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RENESAS

H8SX Series

Asynchronous SCI

Introduction

As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

This H8SX series Application Note provides information you may be need during software and hardware design. This is a basic edition that provides operation examples that each use a single H8SX series on-chip peripheral function.

Although the operation of each program, circuit, and other aspects covered by this application note has been checked, make sure that you conduct your own operation checks before actually using the H8SX series.

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1. Overview

This system asynchronously transmits and receives single-byte data between the H8SX series and H8/38024, as shown in Figure 1. The transfer format is 9600 bps, 8-bit data, 1 stop bit, no parity. RTS and CTS are used for communication.

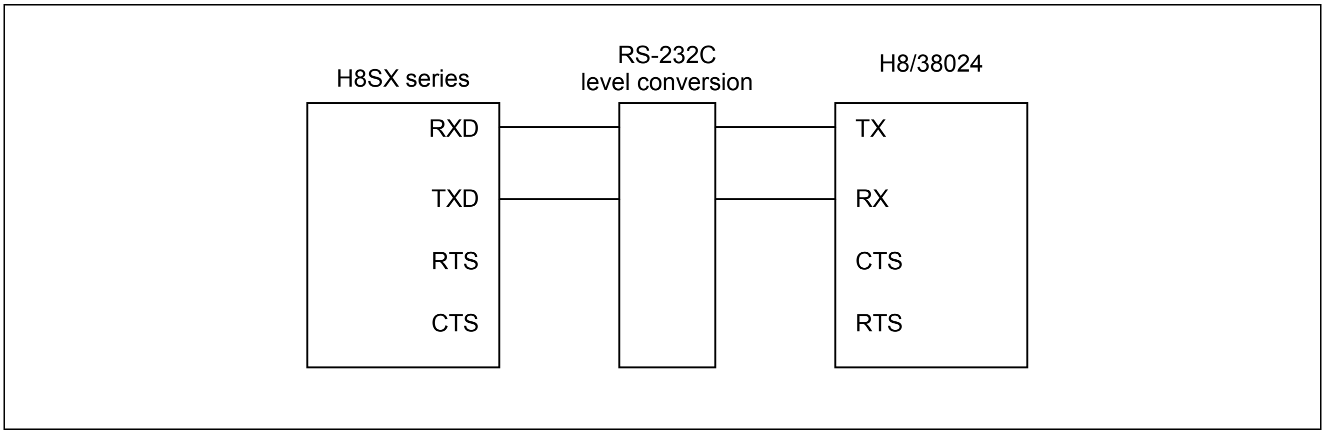


Figure 1 Block Diagram of the Asynchronous SCI Using the H8SX Series

2. Configuration

In this sample task, SCI0 is used to transmit and receive data. Port 3 is used for the communication control pins (RTS and CTS). Figure 2 is a block diagram of the SCI transmission used in this sample task.

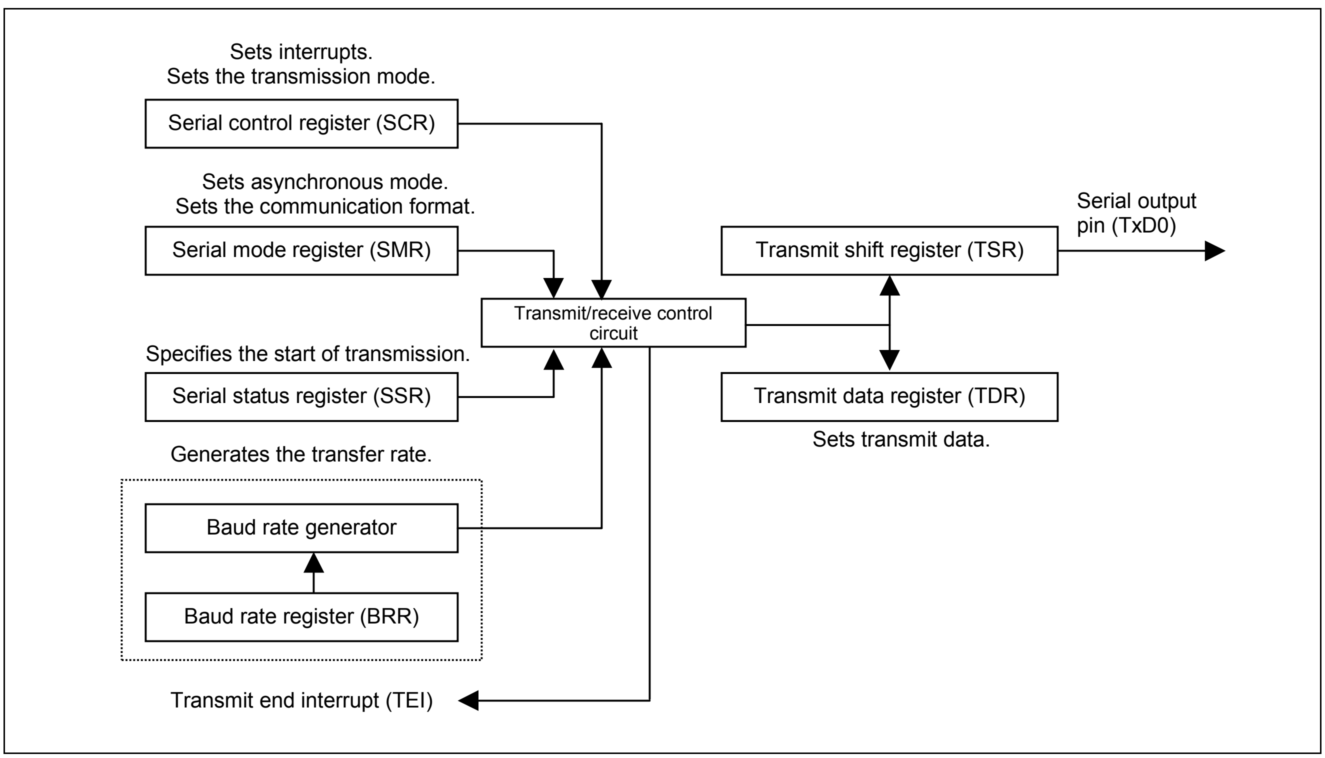


Figure 2 Block Diagram of SCI Transmission

Figure 3 is a block diagram of the SCI reception used in this sample task. The following SCI functions receive data from the H8/38024.

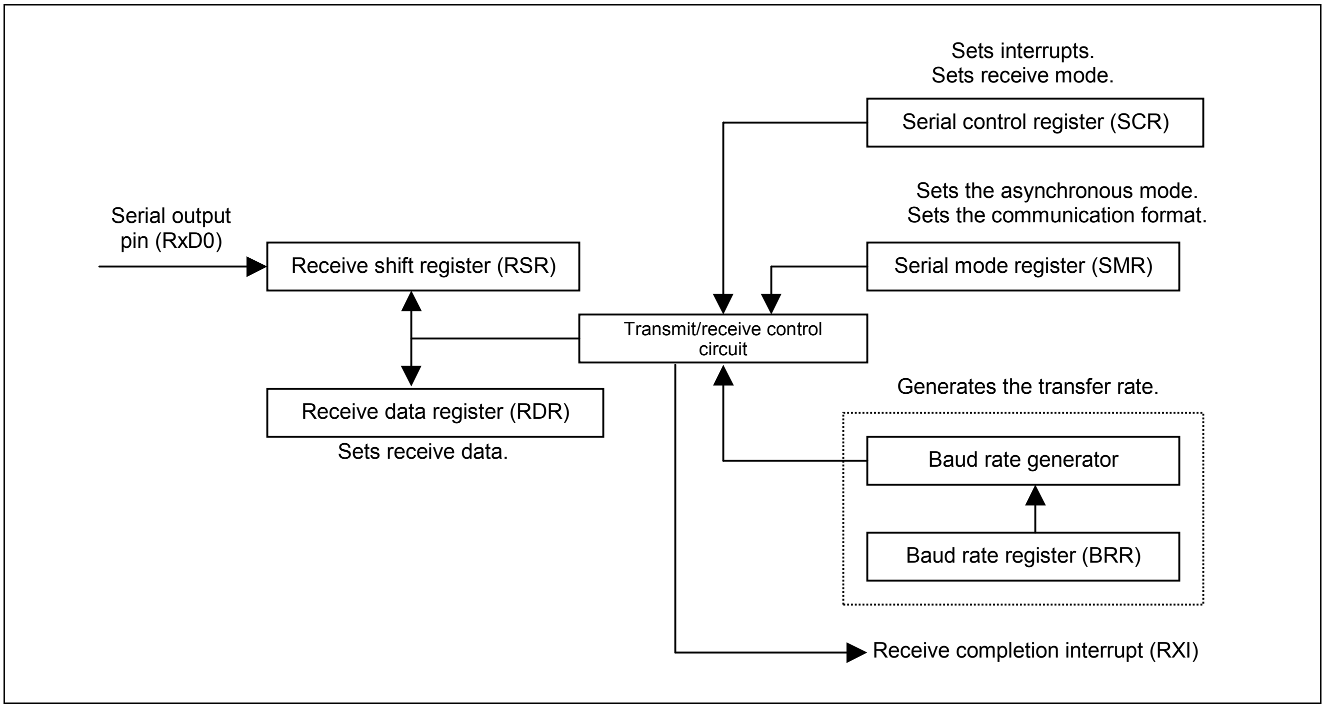


Figure 3 Block Diagram of SCI Reception

Table 1 Function Allocation of H8SX Series

SCI function	Function
RXD	Receives data from the H8/38024.
TXD	Transmits data to the H8/38024.
SMR	Places the SCI in asynchronous mode.
SCR	Enables transmit/receive interrupts and places the SCI in transmit/receive mode.
SSR	Specifies the start of transmission using the TDRE bit.
RDR	Sets the data received from the H8/38024.
TDR	Sets the data to be transmitted to the H8/38024.
BRR	Sets the transfer rate.

Figure 4 shows the description of operation of this sample task. This task performs hardware and software processing based on the timing shown in Figure 4 to interface with the H8/38024.

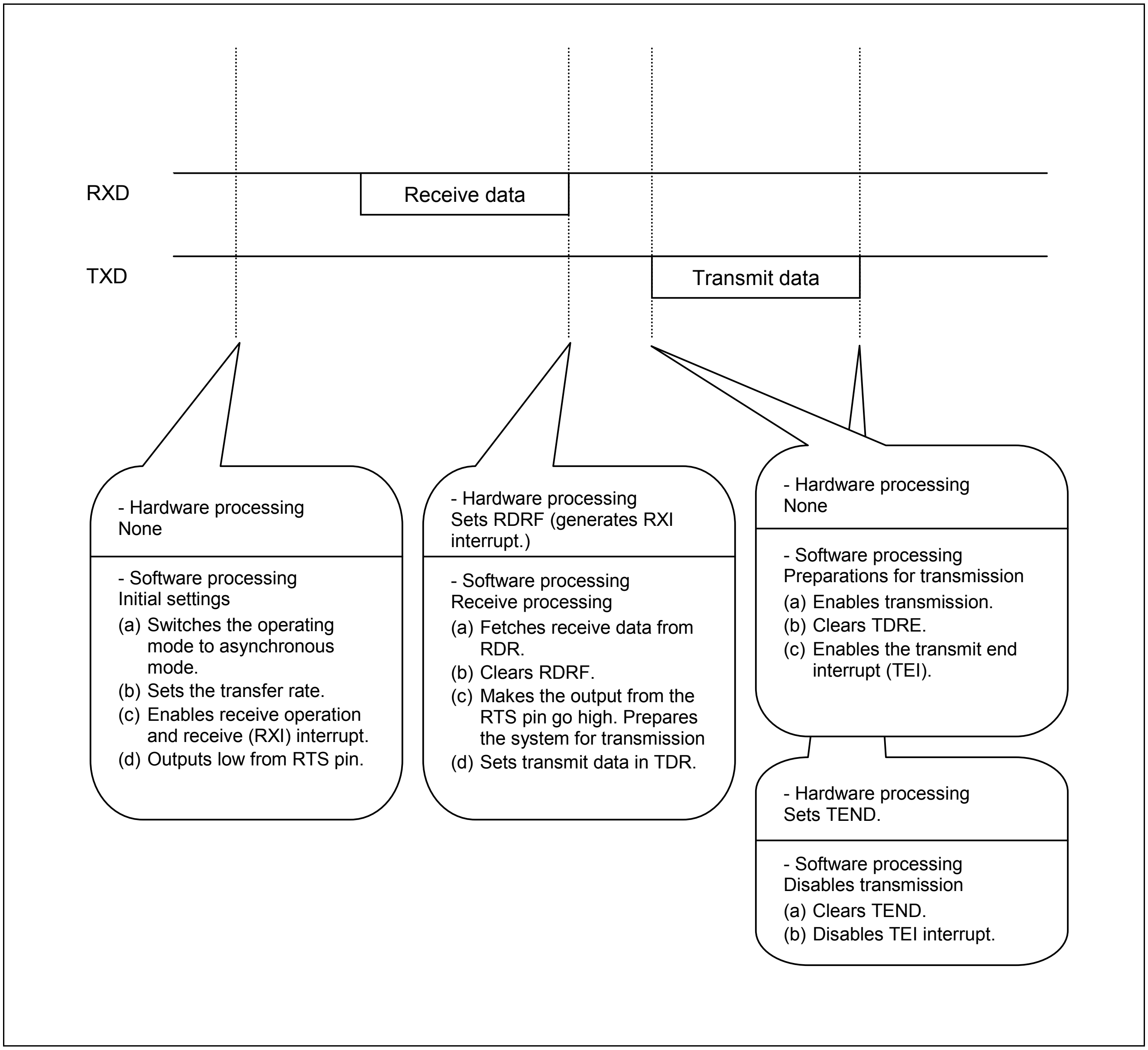


Figure 4 Description of Operation of Asynchronous SCI

3. Sample Program

3.1 Function

This sample program performs communication in the asynchronous mode (synchronous communication in byte units). The communication format is 9600 bps, 8-bit data, 1 stop bit, no parity. This program also controls RTS and CTS by software to enable half-duplex communication.

This sample program receives data from the H8/38024 and then transmits the received data. This program generates an interrupt upon the completion of data reception, fetches the data, and then transmits that data to the H8/38024. Upon the completion of transmission, it generates a transmit end interrupt and then terminates the processing.

3.2 Function Specifications

```
void sci_comm(void);
```

Argument	Description
None	Sets data received from the console.

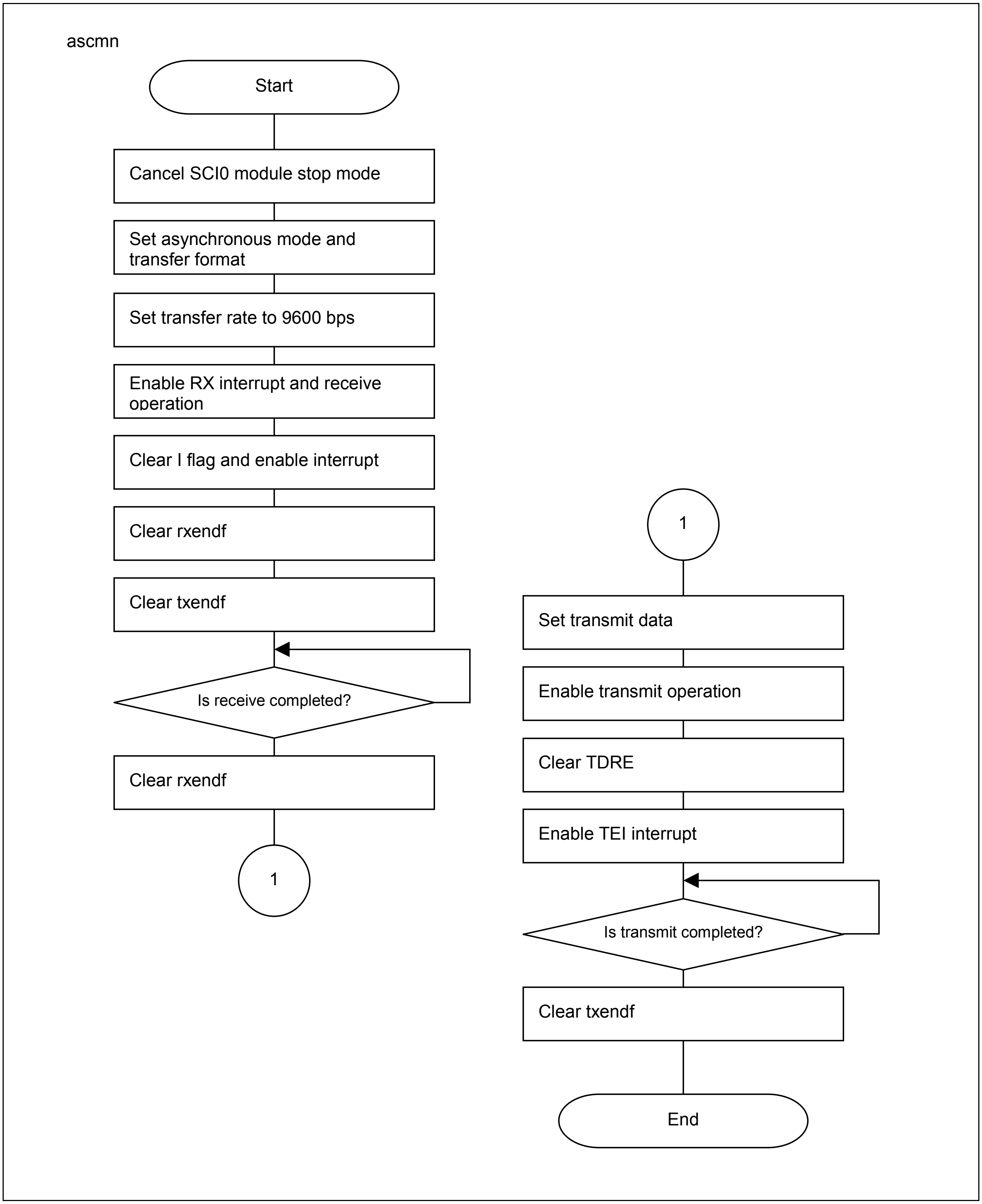
Return value	Description
None	—

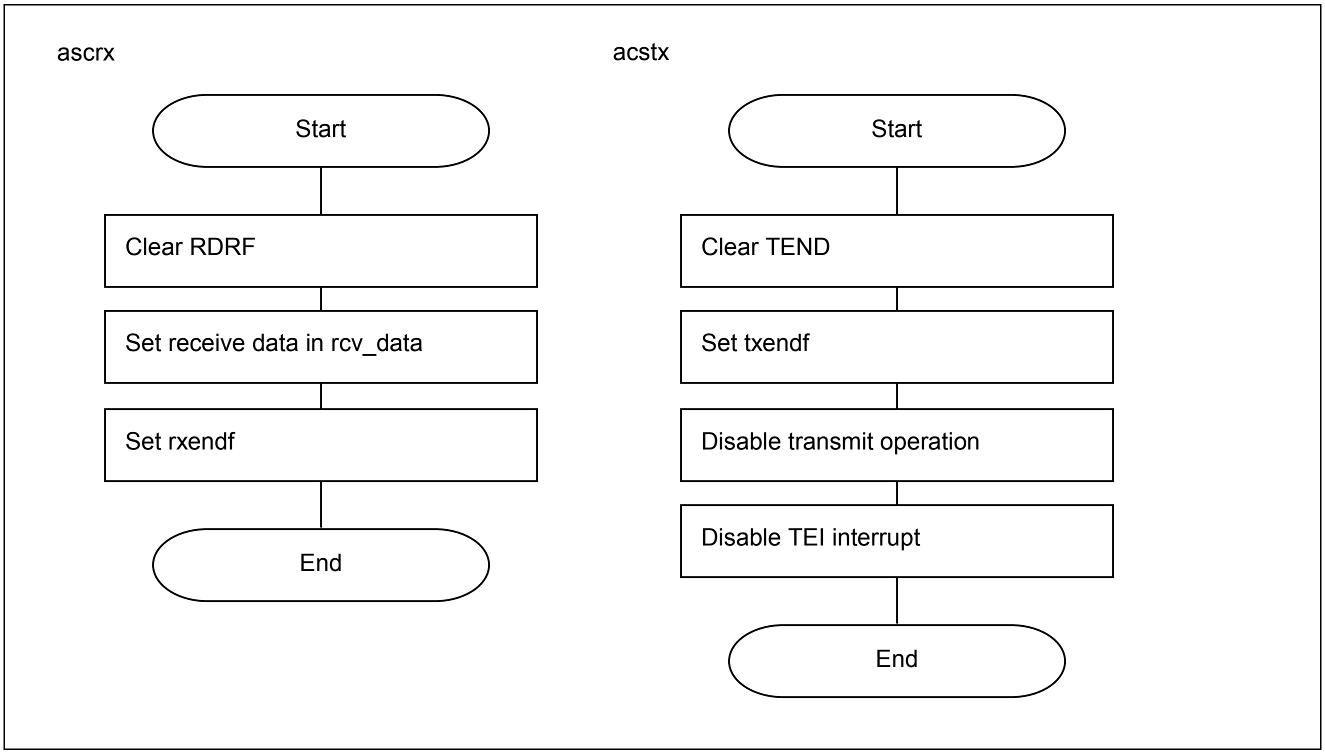
Example)

```
extern void  sci_comm( void );
void  main09( void )                 // Main routine
{
   sci_comm();                       // Asynchronous communication

   while(1) ;
}
```

3.3 Flowchart




ascrx
Start
Clear RDRF
Set receive data in rcv_data
Set rxendf
End
acstx
Start
Clear TEND
Set txendf
Disable transmit operation
Disable TEI interrupt
End

3.4 Program Listing

```
/****************************************************************/
/* Include File                                                 */
/****************************************************************/
#include <machine.h>
#include "iodefine.h"

/****************************************************************/
/* Function Prototype                                           */
/****************************************************************/
void sci_comm(void);

/****************************************************************/
/* RAM Allocation                                               */
/****************************************************************/
static unsigned char rcv_data;  // Receive Data From Console
static volatile unsigned char rxendf;     // Receive End Flag
static volatile unsigned char txendf;     // Trans End Flag
/****************************************************************/
/* Function Definition(Main Program)                            */
/****************************************************************/
void sci_comm(void)
{
   P_MSTPCRB.BIT.MSTPB8 = 0;    // disable module stop mode

   P_P2.ICR.BIT.B1 = 1;
   P_SCI0.SMR.BYTE = 0x00;      // Initialize SMR
   P_SCI0.BRR      = 0x26;      // Set 9600bps
   P_SCI0.SCR.BYTE = 0x50;      // Enable Interrupt
   rxendf = 0;                  // Receive End Flag Initial
   txendf = 0;                  // Trans End Flag Initial
   set_imask_ccr(0);            // Enable Interrupt

   while(rxendf==0);            // Loop For Data Receive
   rxendf = 0;                  // Receive End Flag Clear

   P_SCI0.TDR = rcv_data;       // Set Trans Data

   P_SCI0.SCR.BIT.TE   = 1;     // Enable Trans
   P_SCI0.SSR.BIT.TDRE = 0;     // Data Empty Clear
   P_SCI0.SCR.BIT.TEIE = 1;     // Trans End Interrupt Enable
   while(txendf==0);            // Loop For Data Trans
   txendf = 0;                  // Trans End Flag Clear
}
/****************************************************************/
/* Function Definition(Interrupt Handler)                       */
/****************************************************************/
#pragma interrupt (inthdr_scirx)
void inthdr_scirx (void)         // Receive Interrupt Handler
{
   P_SCI0.SSR.BIT.RDRF = 0;     // RDR Full Clear
   rcv_data       = P_SCI0.RDR; // Get Receive Data(1Byte)
   rxendf              = 1;     // Set Receive End Flag
```

```
}
#pragma interrupt (inthdr_scitx)
void inthdr_scitx (void)         // Transmit Interrupt Handler
{
   P_SCI0.SSR.BIT.TDRE = 0;     // Data Empty Clear
   txendf              = 1;     // Set Trans End Flag
   P_SCI0.SCR.BIT.TE   = 0;     // Trans Disable
   P_SCI0.SCR.BIT.TEIE = 0;     // Trans End Interrupt disable
}
```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sept.19.03	—	First edition issued

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