ISL7457SRH

Extending the TID Capability

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The ISL7457SRH is specified for 10krads(Si) minimum TID in SMD 5962-08230 when continuously biased as shown in Figure 1.

In many cases a 10krad(Si) TID rating is not adequate to meet mission requirements, so a method to extend the TID capability is desired. Figure 2 shows a radiation exposure circuit that biases the ISL7457SRH only 20% of the time. For the other 80% of the time, the ISL7457SRH is unbiased. Devices irradiated in this manner have demonstrated acceptable post-rad parametric limits after 50krad(Si) TID, as indicated in the Electrical Specification tables of this application note. Please note, however, that the post-50krad electrical specifications shown herein are not specified in or guaranteed by SMD 5962-08230.

Imaging Applications

Some camera CCD driver applications do not require 100% availability. In these situations, the ISL7457SRH can be left unbiased until there is a need to image. When imaging is required, the ISL7457SRH can be quickly biased by simply closing a switch. As long as the duty-cycle of the application does not exceed 20%, the TID capability can be extended up to 50krad(Si).

Conclusions

A simple method to extend the TID capability of the ISL7457SRH to 50krad(Si) has been described. This method can be applied to any space-based system that uses the device as long as 20% availability is acceptable.

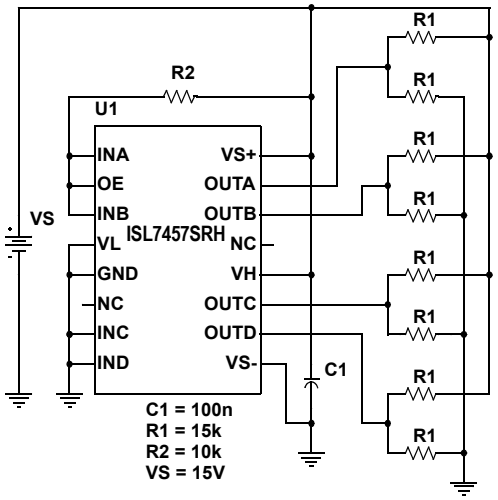

FIGURE 1. RAD EXPOSURE CIRCUIT (BIAS DUTY CYCLE = 100%)

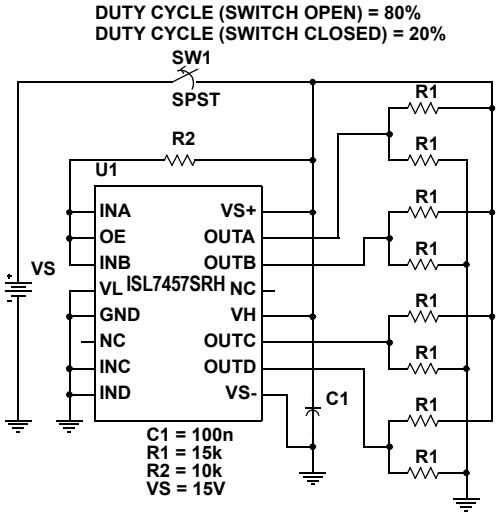

FIGURE 2. RAD EXPOSURE CIRCUIT (BIAS DUTY CYCLE = 20%)

Electrical Specifications $V_S+ = V_H = 5V \pm 10\%$, $V_S- = V_L = 0V$, $OE = V_S+$, $T_A = +25°C$, Post 50krad(Si) unless otherwise specified. Refer to Figure 2 for radiation exposure circuit biasing.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT						
V_{IH}	Logic “1” Input Voltage		2			V
I_{IH}	Logic “1” Input Current	INx = V_S+	-10		10	µA
V_{IL}	Logic “0” Input Voltage				0.6	V
I_{IL}	Logic “0” Input Current	INx = 0V	-10		10	µA
OUTPUT						
R_{OH}	ON Resistance V_H to OUTx	INx = V_S+, I_{OUTx} = -100mA			12	Ω
R_{OL}	ON Resistance V_L to OUTx	INx = 0V, I_{OUTx} = +100mA			7	Ω
I_{LEAK+}	Positive Output Leakage Current	INx = V_S+, OE = 0V, OUTx = V_S+			300	µA
I_{LEAK-}	Negative Output Leakage Current	INx = V_S+, OE = 0V, OUTx = V_S-	-50			µA
POWER SUPPLY						
I_{S+}	V_S+ Supply Current	INx = 0V and V_S+			5	mA
I_{S-}	V_S- Supply Current	INx = 0V and V_S+	-5			mA
I_H	V_H Supply Current	INx = 0V and V_S+			650	µA
I_L	V_L Supply Current	INx = 0V and V_S+	-650			µA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	INx = 0V to 4.5V step, C_L = 1nF			40	ns
t_F	Fall Time	INx = 4.5V to 0V step, C_L = 1nF			26	ns
$t_{RF\Delta}$	t_R, t_F Mismatch	C_L = 1nF			5	ns
t_D+	Turn-On Delay Time	INx = 0V to 4.5V step, C_L = 1nF			30	ns
t_D-	Turn-Off Delay Time	INx = 4.5V to 0V step, C_L = 1nF			40	ns
t_{DD}	t_D+, t_D- Mismatch	C_L = 1nF			12	ns
t_{ENABLE}	Enable Delay Time	INx = V_S+, OE = 0V to 4.5V step, R_L = 1kΩ			35	ns
$t_{DISABLE}$	Disable Delay Time	INX = V_S+, OE = 4.5V to 0V step, R_L = 1kΩ			50	ns

Electrical Specifications $V_S+ = V_H = 15V \pm 10\%$, $V_S- = V_L = 0V$, $OE = V_S+$, $T_A = +25°C$, Post 50krad(Si) unless otherwise specified. Refer to Figure 2 for radiation exposure circuit biasing.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT						
V_{IH}	Logic “1” Input Voltage		2			V
I_{IH}	Logic “1” Input Current	INx = V_S+	-10		10	µA
V_{IL}	Logic “0” Input Voltage				0.6	V
I_{IL}	Logic “0” Input Current	INx = 0V	-10		10	µA
OUTPUT						
R_{OH}	ON Resistance V_H to OUTx	INx = V_S+, I_{OUTx} = -100mA			5	Ω
R_{OL}	ON Resistance V_L to OUTx	INx = 0V, I_{OUTx} = +100mA			5	Ω
I_{LEAK+}	Positive Output Leakage Current	INx = V_S+, OE = 0V, OUTx = V_S+			300	µA
I_{LEAK-}	Negative Output Leakage Current	INx = V_S+, OE = 0V, OUTx = V_S-	-50			µA
POWER SUPPLY						
I_{S+}	V_S+ Supply Current	INx = 0V and V_S+			5	mA
I_{S-}	V_S- Supply Current	INx = 0V and V_S+	-5			mA
I_H	V_H Supply Current	INx = 0V and V_S+			750	µA
I_L	V_L Supply Current	INx = 0V and V_S+	-750			µA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	INx = 0V to 5V step, C_L = 1nF			20	ns
t_F	Fall Time	INx = 5V to 0V step, C_L = 1nF			20	ns
$t_{RF\Delta}$	t_R, t_F Mismatch	C_L = 1nF			3	ns
t_D+	Turn-On Delay Time	INx = 0V to 5V step, C_L = 1nF			20	ns
t_D-	Turn-Off Delay Time	INx = 5V to 0V step, C_L = 1nF			20	ns
t_{DD}	t_D+, t_D- Mismatch	C_L = 1nF			5	ns
t_{ENABLE}	Enable Delay Time	INx = V_S+, OE = 0V to 5V step, R_L = 1kΩ			25	ns
$t_{DISABLE}$	Disable Delay Time	INx = V_S+, OE = 5V to 0V step, R_L = 1kΩ			65	ns

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