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# H8S/2400 Series

## A/D Conversion in Scan Mode

### Introduction

This application note describes an example of A/D conversion of analog inputs on four channels in scan mode, with the results stored in on-chip RAM.

Scan mode enables consecutive A/D conversion of analog inputs on four channels in response to a single initiating trigger.

### Target Device

H8S/2472, H8S/2463, H8S/2462 Group

### Preface

This application note was prepared using the H8S/2472, H8S/2463, H8S/2462 Group, one of the devices on which operation has been confirmed, as the basis.

This program can be used with other H8S/2400 Series MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

### Contents

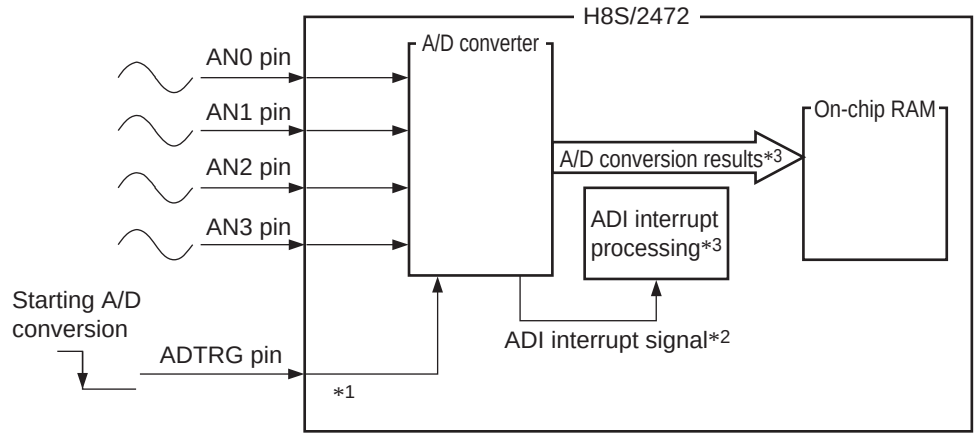
## 1. Specifications

In this application note, the A/D converter is set to scan mode, and performs conversion accordingly.

A/D conversion is initiated by the signal on the $\overline{\text{ADTRG}}$ pin, and is performed for the analog inputs on four channels. The results are stored in on-chip RAM.

Figure 1 is an overview of the operations, and the list below covers the specifications of the operations in detail.

- Set the A/D converter for converting four channels (signals on pins AN0 to AN3) in scan mode.
- A/D conversion is started by the falling edge of the $\overline{\text{ADTRG}}$ signal.
- Set the conversion time to 160 states (5.0 μs when ϕ = 32 MHz).
- The processing routing for the ADI interrupt stops the A/D conversion that was initiated by the $\overline{\text{ADTRG}}$ signal and stores the results of conversion in on-chip RAM.




Notes: *1 A/D conversion is initiated by the falling edge of the $\overline{\text{ADTRG}}$ signal.
*2 An ADI interrupt is generated at the end of A/D conversion for the four channels.
*3 The results are stored in the on-chip RAM from within the ADI interrupt processing routine.

**Figure 1 Overview**

## 2. Conditions for Application

**Table 1 Conditions for Application**

| Item | Contents |
|---|---|
| Operating frequency | Input clock: 8 MHz<br>System clock (ϕ): 32 MHz (8 MHz multiplied by 4) |
| Operating voltage | 3.3 V |
| Operating mode | Mode 2 ($\overline{MD2}$ = 1, MD1 = 1) |
| Integrated development environment | High-performance Embedded Workshop Version 4.05.00.059 |
| Evaluation board | Renesas Technology<br>R0K402472D000BR |
| C/C++ compiler | Renesas Technology<br>H8S,H8/300 C/C++ Compiler (V.6.02.01.000) |
| Compile options | -cpu=2600A:24 -optimize=1 -regparam=3<br>-speed=register,shift,struct,expression |
| Optimizing linkage editor | Renesas Technology<br>Optimizing Linkage Editor (V.9.04.01.000) |
| Linker options | -start= PResetPRG,PIntPRG/01000, P,C$DSEC,C$BSEC,D/01400,<br>B,R/0FF0800, S/0FF9600 |

# 3. Description of Modules Used

## 3.1 A/D Converter

The A/D converter operates by successive approximation with 10-bit resolution. It has two operating modes: single mode and scan mode. When changing the operating mode or analog input channel, to prevent incorrect operation, first clear the ADST bit to 0 in A/D control/status register (ADCSR) to halt A/D conversion. The ADST bit can be set to 1 at the same time as the operating mode or analog input channel is changed.

## 3.2 Scan Mode

In scan mode, A/D conversion is performed sequentially on the specified channels (four channels or eight channel maximum). Operations are as follows.

1. When the ADST bit in ADCSR is set to 1 by software or by the input of trigger signal, A/D conversion starts from the first channel of the selected channel. Consecutive A/D conversion of either four channels maximum (SCANE and SCANS = B'10) or eight channels maximum (SCANE and SCANS = B'11) can be selected. In the case of consecutive A/D conversion on four channels, the operation starts from AN0 when CH2 = B'0, and starts from AN4 when CH2 = B'1. In the case of consecutive A/D conversion on eight channels, the operation starts from AN0.
2. When A/D conversion for each channel is completed, the result is sequentially transferred to the A/D data register corresponding to each channel.
3. When conversion of all the selected channels is completed, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt is requested after A/D conversion ends. Conversion of the first channel in the group starts again.
4. The ADST bit is not automatically cleared to 0 and steps 2 to 3 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops and the A/D converter enters the idle state. After that, when the ADST bit is set to 1, the operation starts from the first channel again.

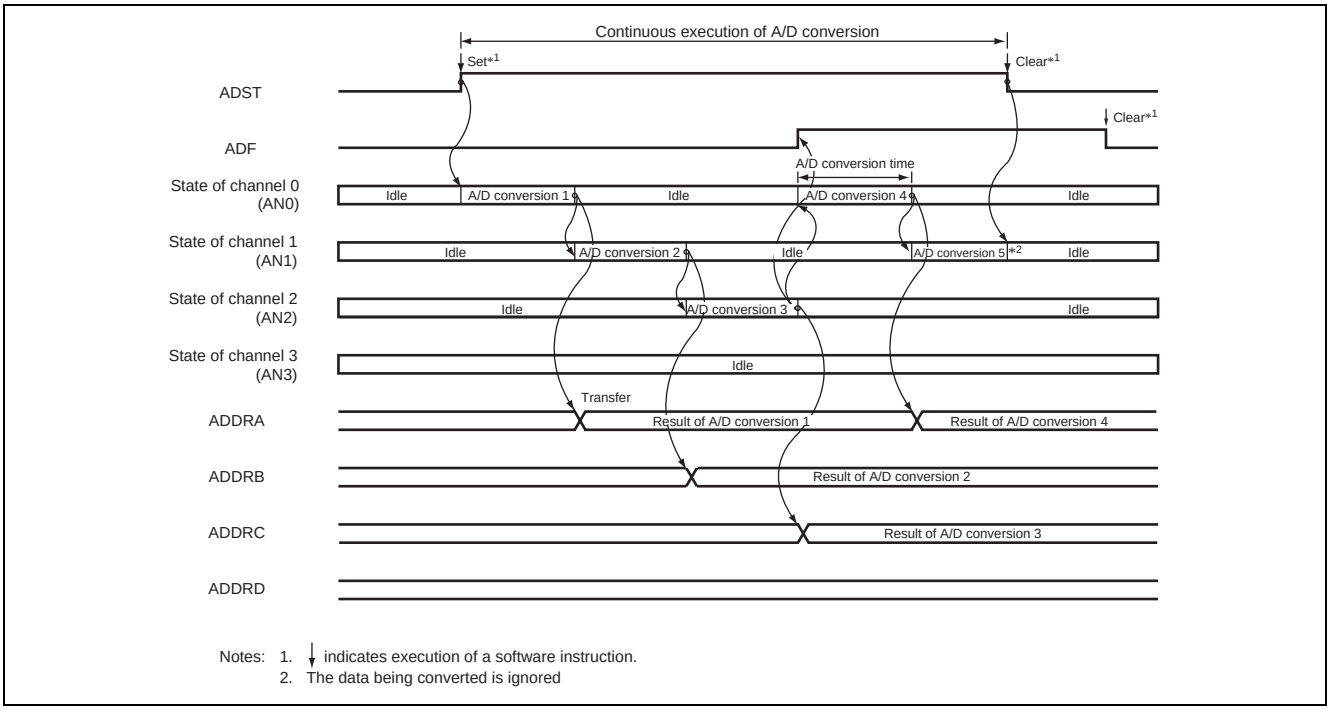



**Figure 2 Example of A/D Converter Operation (When Channels AN0 to AN2 are Selected in Scan Mode)**

## 3.3 Input Sampling and A/D Conversion Time

The A/D converter has a built-in sample-and-hold circuit. The A/D converter samples the analog input when the A/D conversion start delay time ($t_D$) has passed after the ADST bit in ADCSR is set to 1, then starts A/D conversion. Figure 3 shows the A/D conversion timing. Tables 2 shows the A/D conversion time.

As indicated in figure 3, the A/D conversion time ($t_{CONV}$) includes $t_D$ and the input sampling time ($t_{SPL}$). The length of $t_D$ varies depending on the timing of the write access to ADCSR. The total conversion time therefore varies within the ranges indicated in table 2.

In scan mode, the values given in table 2 apply to the first conversion time. The values given in table 3 apply to the second and subsequent conversions. In either case, bits CKS1 and CKS0 in A/D control register (ADCR) should be set so that the conversion time is within the ranges indicated by the A/D conversion characteristics (Figure 4).

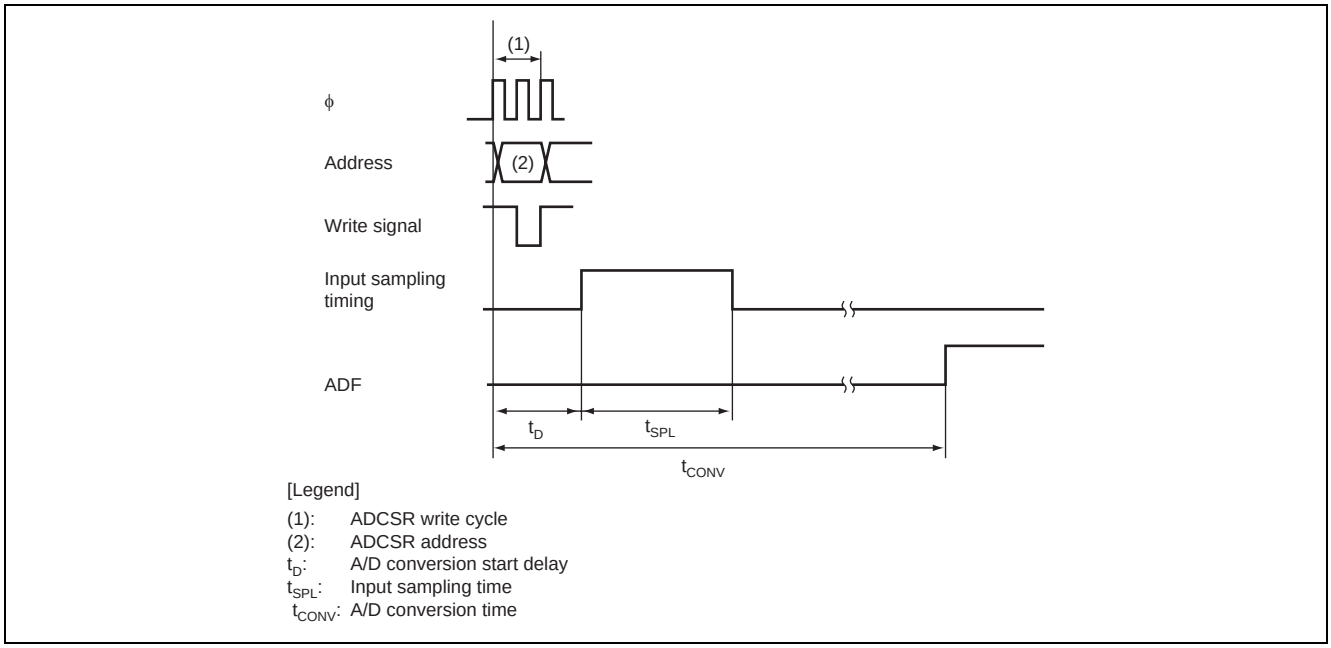



**Figure 3 A/D Conversion Timing**

**Table 2 A/D Conversion Characteristics (Single Mode)**

| | | CKS1 = 0 | | | CKS1 = 1 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | CKS0 = 1 | | | CKS0 = 0 | | | CKS0 = 1 | | |
| **Item** | **Symbol** | **min** | **typ** | **max** | **min** | **typ** | **max** | **min** | **typ** | **max** |
| A/D conversion start delay time | $t_D$ | (6) | — | (9) | (10) | — | (17) | (18) | — | (33) |
| Input sampling time | $t_{SPL}$ | — | 30 | — | — | 60 | — | — | 120 | — |
| A/D conversion time | $t_{CONV}$ | 77 | — | 80 | 153 | — | 160 | 305 | — | 320 |

Note: Values in the table are the number of states.

**Table 3 A/D Conversion Characteristics (Scan Mode)**

| CKS1 | CKS0 | Conversion Time (Number of States) |
|---|---|---|
| 0 | 0 | Setting prohibited |
| 0 | 1 | 80 (Fixed) |
| 1 | 0 | 160 (Fixed) |
| 1 | 1 | 320 (Fixed) |

**Table 4 A/D Conversion Characteristics (AN7 to AN0 Input: 80/160-State Conversion)**

Condition A: VCC = 3.0 V to 3.6 V, AVCC = 3.0 V to 3.6 V, AVref = 3.0 V to AVCC, VSS = AVSS = 0 V, ϕ = 20 MHz

Condition B: VCC = 3.0 V to 3.6 V, AVCC = 3.0 V to 3.6 V, AVref = 3.0 V to AVCC, VSS = AVSS = 0 V, ϕ = 20 MHz to 34 MHz

| | Condition A | | | Condition B | | | |
|---|---|---|---|---|---|---|---|
| **Item** | **min** | **typ** | **max** | **min** | **typ** | **max** | **Unit** |
| Resolution | 10 | 10 | 10 | 10 | 10 | 10 | Bits |
| Conversion time | — | — | 4.0*[1] | — | — | 4.7*[2] | µs |
| Analog input capacitance | — | — | 20 | — | — | 20 | pF |
| Permissible signalsource impedance | — | — | 5 | — | — | 5 | kΩ |
| Nonlinearity error | — | — | ±7.0 | — | — | ±7.0 | LSB |
| Offset error | — | — | ±7.5 | — | — | ±7.5 | |
| Full-scale error | — | — | ±7.5 | — | — | ±7.5 | |
| Quantization error | — | — | ±0.5 | — | — | ±0.5 | |
| Absolute accuracy | — | — | ±8.0 | — | — | ±8.0 | |

Notes: *1 Value when using the maximum operating frequency in single mode of 80 states.
*2 Value when using the maximum operating frequency in single mode of 160 states.

## 3.4 Timing of External Trigger Input

A/D conversion can also be started by an externally input trigger signal. Setting the TRGS1, TRGS0 and EXTRGS bits in ADCR to B'101 selects the signal on the $\overline{\text{ADTRG}}$ pin as an external trigger. The ADST bit in ADCSR is set to 1 on the falling edge of $\overline{\text{ADTRG}}$, initiating A/D conversion. Other operations are the same as those in the case where the ADST bit is set to 1 by software, regardless of whether the converter is in single mode or scan mode. The timing of this operation is shown in figure 4.

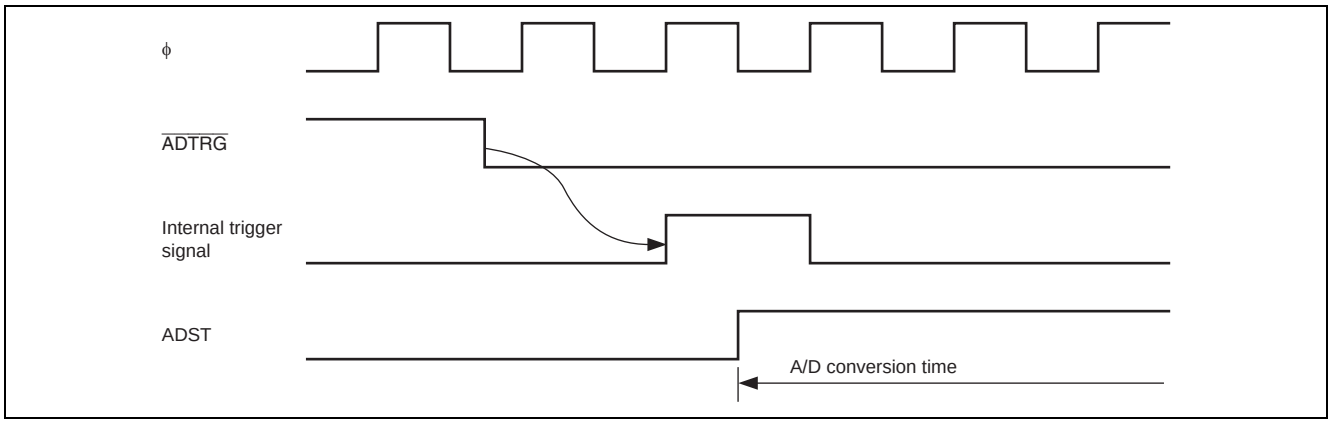



**Figure 4 Timing of External Trigger Input**

# 4. Description of Operation

## 4.1 Description of Operation

Figure 5 shows the operation described in this application note.

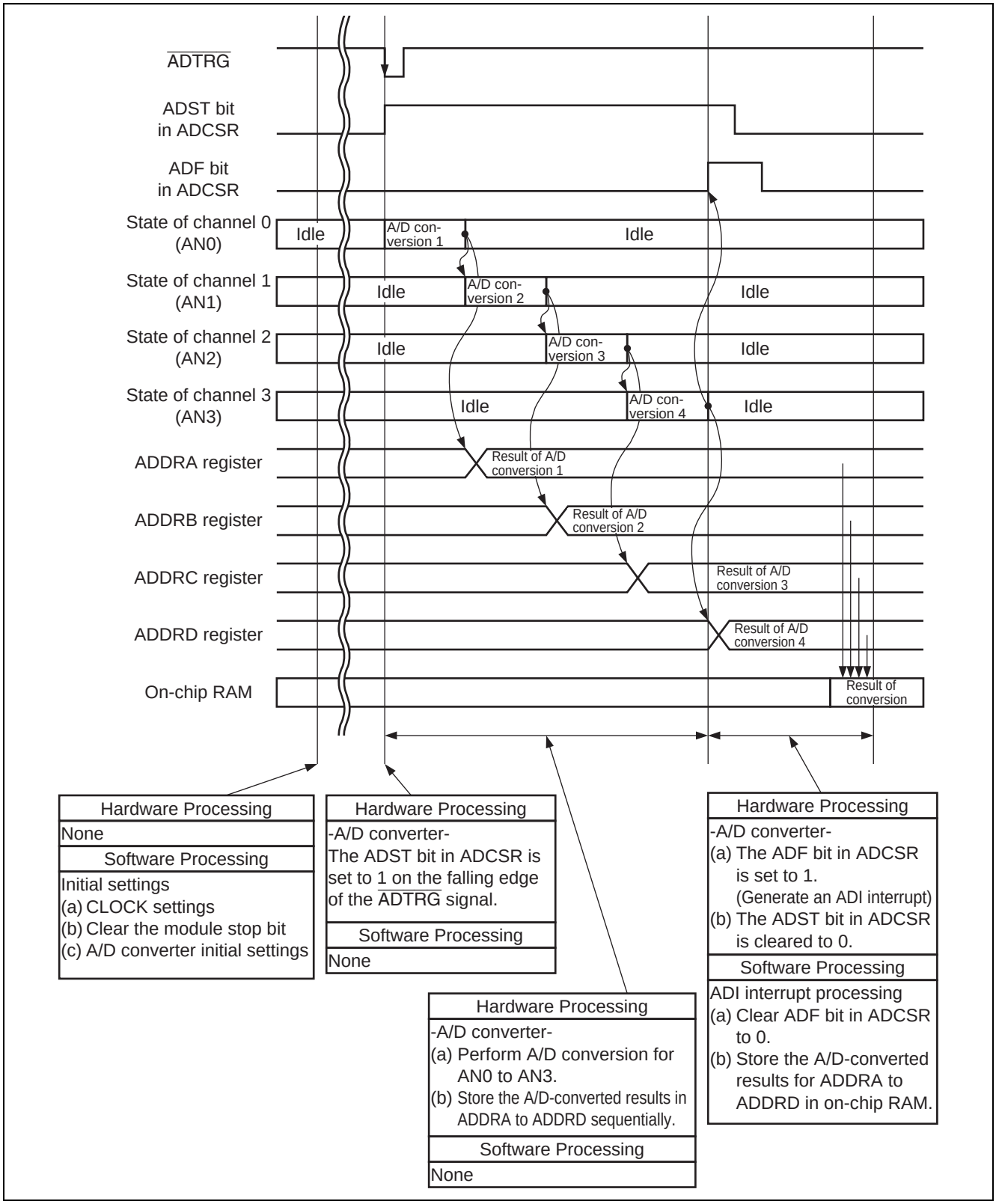



**Figure 5 Operation**

## 4.2 A/D Conversion Time

A/D conversion time is specified as 4.7 μs (max.) when ϕ = 32 MHz, as shown in table 4, A/D Conversion Characteristics (AN7 to AN0 Input: 80/160-State Conversion).

The optimal number of states (clock cycles) for A/D conversion is obtained by using the following formula.

$$\text{A/D conversion time [states]} = \text{A/D conversion time [μs]} \times \text{Operating frequency [MHz]}$$
$$= 4.7\ \mu\text{F} \times 32\ \text{MHz} = 150.4\ \text{states}$$

Due to the following relation

$$80\ \text{states} < 150.4\ \text{states} < 160\ \text{states}$$

conversion takes 160 states.

Since ϕ = 32 MHz, the A/D conversion time is

$$\text{A/D conversion time [μs]} = \frac{\text{A/D conversion time [states]}}{\text{Operating frequency [MHz]}} = \frac{160\ \text{[states]}}{32\ \text{[MHz]}} = 5.0\ \mu\text{s}$$

# 5. Description of Software

## 5.1 RAM Variables

**Table 5 List of RAM Variables**

| Type | Variable Name | Description | Used by Functions |
|---|---|---|---|
| unsigned short | scn[4] | Store the A/D-converted results for ADDRA to ADDRD | main, INT_ADI |
| unsigned char | adiend | End of ADI interrupt determination flag<br>0: A/D conversion is in progress<br>1: A/D conversion interrupt processing has ended | main, INT_ADI |

## 5.2 List of Functions

**Table 6 List of Functions**

| Function Name | Descriptions |
|---|---|
| PowerOn_Reset | • Initial settings function<br>Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, calls main function. |
| main | • Main function<br>Calls init function. Determine ADI interrupt processing end. |
| init | • I/O register initialization function<br>Sets clock mode, module stop mode, and A/D converter. |
| INT_ADI | • ADI interrupt processing<br>Disables the A/D conversion that was initiated by the $\overline{\text{ADTRG}}$ signal, and stores the results of A/D-conversion for the four channels. |

## 5.3 Functions

### 5.3.1 PowerON_Reset Function

(1) Functional overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then PowerON_Reset function calls the main function.

(2) Arguments

None

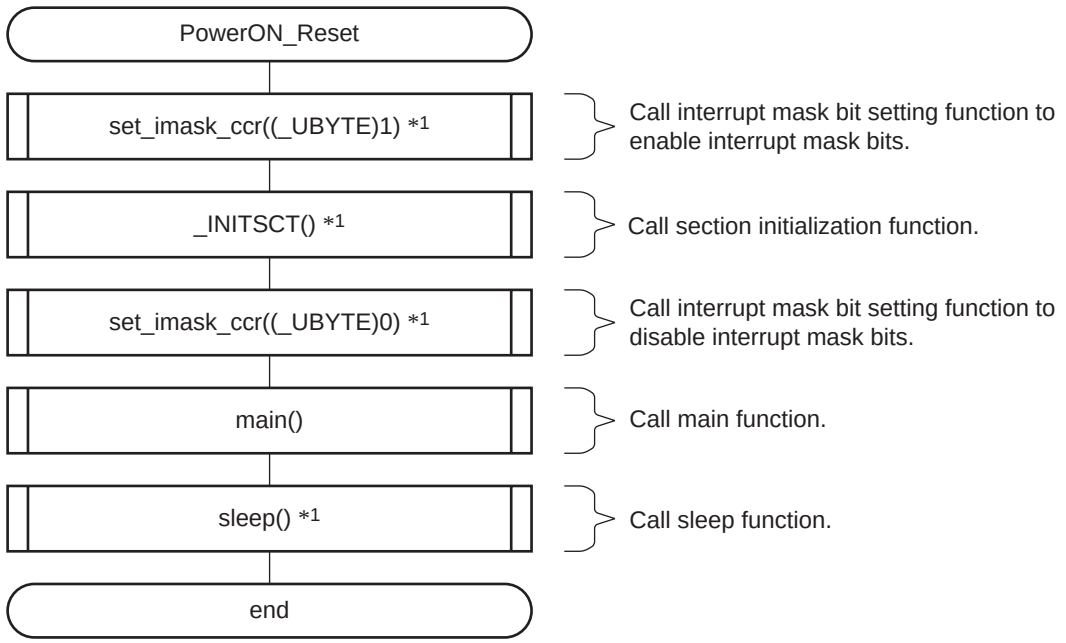
(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart




Note: *1 • set_imask_ccr function: Intrinsic function
• _INITSCT function: Standard library function
• sleep function: Intrinsic function
For details, please refer to the *Development Environment Manual* in the "6. Documents for Reference".

**Figure 6 Flowchart (PowerON_Reset)**

### 5.3.2 main Function

(1) Functional overview

The main function calls the init function and detects the end of the ADI interrupt processing.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below.

Note that the setting values shown are those used in this application note and differ from the initial values.

- Mode Control Register (MDCR) Number of bits: 8 Address: H'FFFFC5

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 7 | EXPE | 0 | R/W | Extended Mode Enable<br>Specifies extended mode.<br>0: Single-chip mode |
| 2 | MDS2 | —* | R | Mode Select 2 and 1 |
| 1 | MDS1 | —* | R | These bits indicate the input levels at mode pins ($\overline{MD2}$ and MD1) (the current operating mode). Bits MDS2 and MDS1 correspond to $\overline{MD2}$ and MD1, respectively. MDS2 and MDS1 are read-only bits and they cannot be written to. The mode pin ($\overline{MD2}$ and MD1) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset. |

Note: * The initial values are determined by the settings of the $\overline{MD2}$ and MD1 pins.

(5) Flowchart

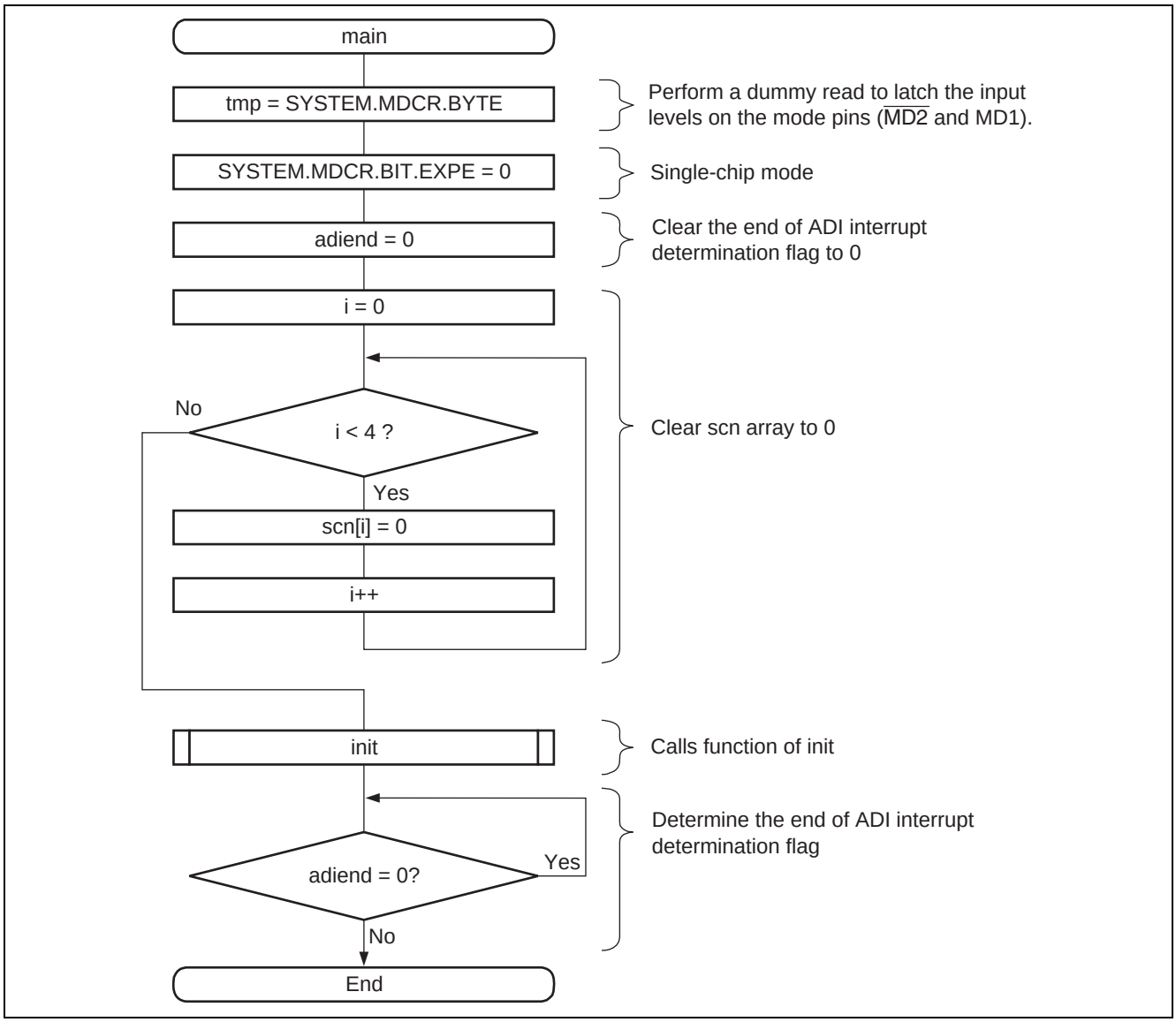



**Figure 7 Flowchart**

### 5.3.3 init Function

(1) Functional overview

The init function sets the clock mode, module stop mode, and A/D converter.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below.

Note that the setting values shown are those used in this application note and differ from the initial values.

- A/D Control/Status Register (ADCSR) Number of bits: 8 Address: H'FFFEB0

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 7 | ADF | 0 | R/(W)* | A/D End Flag<br>A status flag that indicates the end of A/D conversion. This flag indicates that the results of A/D conversion are stored in the A/D data registers.<br>[Setting conditions]<br>• When A/D conversion ends in single mode<br>When A/D conversion ends on all channels specified in scan mode<br>[Clearing conditions]<br>• When 0 is written after reading ADF = 1<br>• When DTC starts by an ADI interrupt and ADDR is read |
| 6 | ADIE | 1 | R/W | A/D Interrupt Enable<br>Enables ADI interrupt by ADF when this bit is set to 1 |
| 5 | ADST | 0 | R/W | A/D Start<br>Clearing this bit to 0 stops A/D conversion and enters the idle state. Setting this bit to 1 starts A/D conversion. In single mode, this bit is cleared to 0 automatically when conversion on the specified channel ends. In scan mode, conversion continues sequentially on the specified channels until this bit is cleared to 0 by software, a reset, or a transition to the hardware standby mode. |
| 2 | CH2 | 0 | R/W | Channel Select 2 to 0<br>Select analog input channels together with the SCANE bit and the SCANS bit of ADCR.<br>When SCANE = 1 and SCANS = 0<br>011: AN0 to AN3 |
| 1 | CH1 | 1 | R/W | |
| 0 | CH0 | 1 | R/W | |

Note: * Only 0 can be written to clear the flag.

- A/D Control Register (ADCR) Number of bits: 8 Address: H'FFFEB1

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 7 | TRGS1 | 1 | R/W | Timer Trigger Select 1 and 0, Extended Trigger Select |
| 6 | TRGS0 | 0 | R/W | Enable starting of A/D conversion by a trigger signal. |
| 0 | EXTRGS | 1 | R/W | 101: Enables starting by the $\overline{\text{ADTRG}}$ pin input. |
| 5 | SCANE | 1 | R/W | Scan Mode |
| 4 | SCANS | 0 | R/W | Select the operation mode of A/D conversion<br>10: Scan mode (consecutive A/D conversion of channels 1 to 4) |
| 3 | CKS1 | 1 | R/W | Clock Select 1 and 0 |
| 2 | CKS0 | 0 | R/W | Set the A/D conversion time. Setting should be made while the conversion is stopped (ADST = 0).<br>10: Conversion time = 160 states (max) |
| 1 | ADSTCLR | 1 | R/W | A/D Start Clear<br>Sets automatic clearing of the ADST bit in scan mode.<br>1: ADST is automatically cleared when A/D conversion for all the selected channels has been completed in scan mode. |

- Interrupt Control Registers B (ICRB) Number of bits: 8 Address: H'FFFEE9

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 7 | ICRB7 | 0 | R/W | Interrupt Control Level<br>0: Corresponding interrupt source (A/D converter) is interrupt control level 0 (no priority) |

- Standby Control Register (SBYCR) Number of bits: 8 Address: H'FFFF84

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 2 | SCK2 | 0 | R/W | System Clock Select 2 to 0 |
| 1 | SCK1 | 0 | R/W | Select a clock for the bus master in high-speed mode or medium-speed mode. |
| 0 | SCK0 | 0 | R/W | 000: High-speed mode |

- Low-Power Control Register (LPWRCR) Number of bits: 8 Address: H'FFFF85

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 4 | EXCLE | 0 | R/W | Subclock Input Enable<br>Enables/disables subclock input from the EXCL pin.<br>0: Disables subclock input from the EXCL pin |

- Module Stop Control Registers H (MSTPCRH) Number of bits: 8 Address: H'FFFF86

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 6 | MSTP14 | 0 | R/W | Data transfer controller (DTC) |
| 5 | MSTP13 | 1 | R/W | 16-bit free-running timer (FRT) |
| 4 | MSTP12 | 1 | R/W | 8-bit timers (TMR_0, TMR_1) |
| 3 | MSTP11 | 1 | R/W | 14-bit PWM timer (PWMX) |
| 1 | MSTP9 | 0 | R/W | A/D converter |
| 0 | MSTP8 | 1 | R/W | 8-bit timers (TMR_X, TMR_Y) |

- Port 8 Data Direction Register (P8DDR) Number of bits: 8 Address: H'FFFFBD

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 7 | P87DDR | 0 | W | If port 8 pins are specified for use as the general I/O port, the corresponding pins function as output port when the P8DDR bits are set to 1, and as input port when cleared to 0.<br>Since this register is allocated to the same address as PBPIN, states of the port 8 pins are when this register is read. |
| 6 | P86DDR | 1 | W | |
| 5 | P85DDR | 1 | W | |
| 4 | P84DDR | 1 | W | |
| 3 | P83DDR | 1 | W | |
| 2 | P82DDR | 1 | W | |
| 1 | P81DDR | 1 | W | |
| 0 | P80DDR | 1 | W | |

- System Control Register (SYSCR) Number of bits: 8 Address: H'FFFFC4

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 5 | INTM1 | 0 | R | These bits select the control mode of the interrupt controller.<br>00: Interrupt control mode 0 |
| 4 | INTM0 | 0 | R/W | |

(5) Flowchart

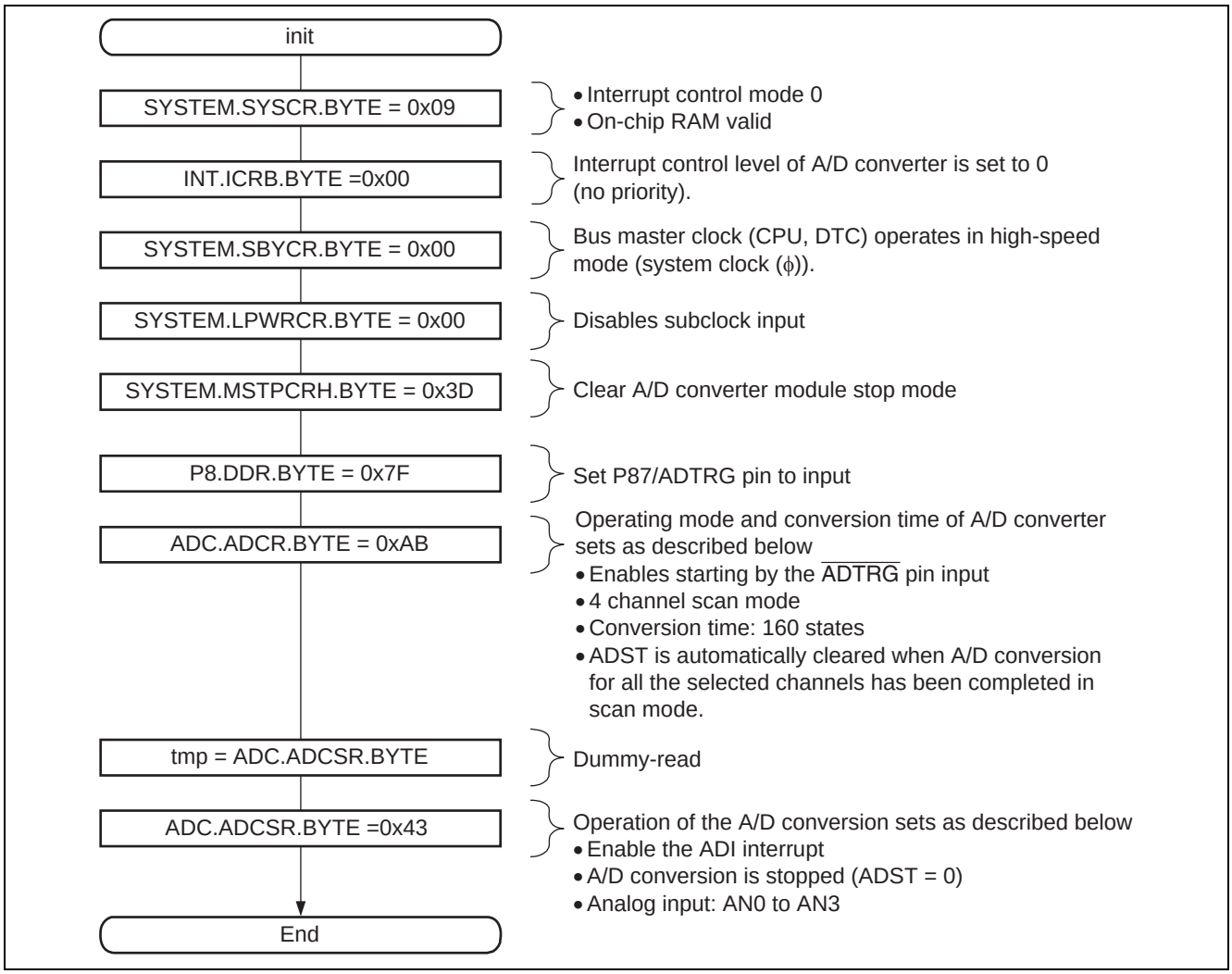



**Figure 8 Flowchart**

### 5.3.4 INT_ADI Function

(1) Functional overview

Disables the A/D conversion that was initiated by the $\overline{\text{ADTRG}}$ signal, and stores the results of A/D-conversion for the four channels.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below.

Note that the setting values shown are those used in this application note and differ from the initial values.

- A/D Data Registers A to D (ADDRA to ADDRD) Number of bits: 16 Address: H'FFFEA0 to H'FFFEA6

  The ADDR are eight 16-bit read-only registers, ADDRA to ADDRH, which store the results of A/D conversion. The ADDR registers, which store a conversion result for each channel, are shown in table 7.

  The converted 10-bit data is stored to bits 15 to 6. The lower 6-bit data is always read as 0. The data bus between the CPU and the A/D converter is 16-bit width and can be read directly from the CPU. The ADDR must always be accessed in 16-bit unit. They cannot be accessed in 8-bit unit.

  The results of A/D conversion are stored in each registers, when the ADF flag is set to 1.

**Table 7 Analog Input Channels and Corresponding ADDR Registers**

| Analog Input Channel | A/D Data Register to Store A/D Conversion Results |
|---|---|
| AN0 | ADDRA |
| AN1 | ADDRB |
| AN2 | ADDRC |
| AN3 | ADDRD |

- A/D Control/Status Register (ADCSR) Number of bits: 8 Address: H'FFFEB0

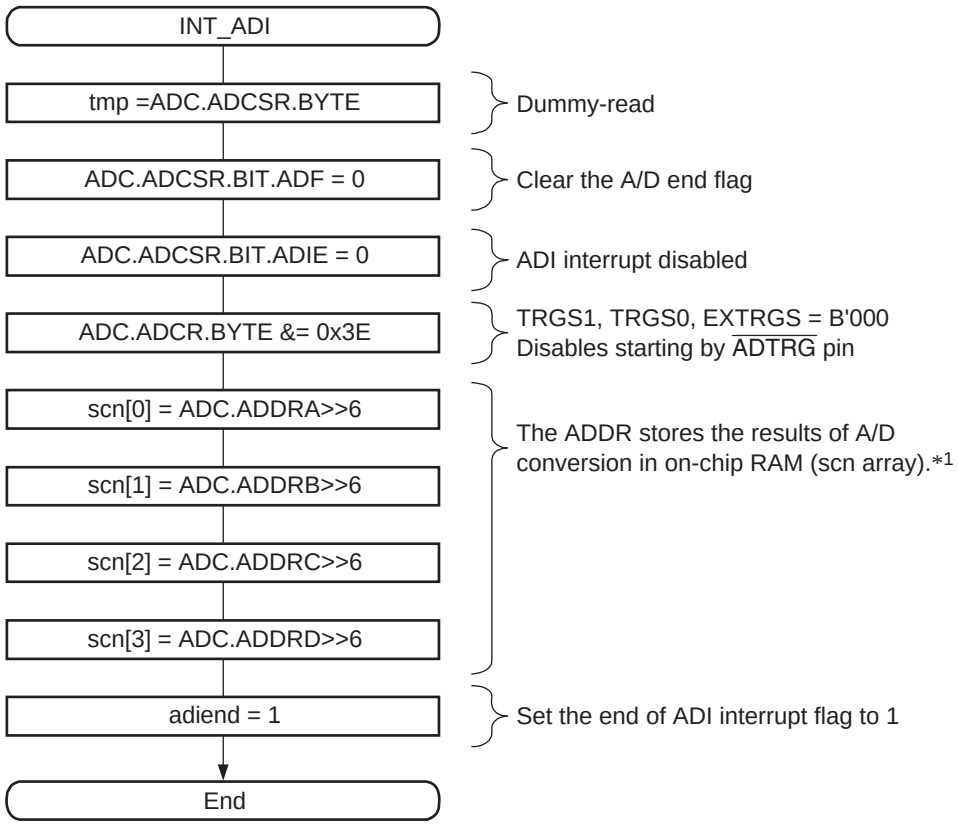
| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 7 | ADF | 0 | R/(W)* | A/D End Flag<br>A status flag that indicates the end of A/D conversion.<br>This flag indicates that the results of A/D conversion are stored in the A/D data registers.<br>[Setting conditions]<br>• When A/D conversion ends in single mode<br>When A/D conversion ends on all channels specified in scan mode<br>[Clearing conditions]<br>• When 0 is written after reading ADF = 1<br>• When DTC starts by an ADI interrupt and ADDR is read |
| 6 | ADIE | 0 | R/W | A/D Interrupt Enable<br>Enables ADI interrupt by ADF when this bit is set to 1 |

Note: * Only 0 can be written to clear the flag.

- A/D Control Register (ADCR) Number of bits: 8 Address: H'FFFEB1

| Bit | Bit Name | Setting | R/W | Descriptions |
|---|---|---|---|---|
| 7 | TRGS1 | 0 | R/W | Timer Trigger Select 1 and 0, Extended Trigger Select |
| 6 | TRGS0 | 0 | R/W | Enable starting of A/D conversion by a trigger signal. |
| 0 | EXTRGS | 0 | R/W | These bits should be set while A/D conversion is stopped (ADST = 0).<br>000: Disables starting by trigger signals. |

(5) Flowchart




Note: *1 The results of A/D conversion are stored in the upper 10 bits of ADDRA to ADDRD. In this application note, ADDRA to ADDRD are shifted six bits to the right and stored in on-chip RAM (scn array).

**Figure 9 Flowchart**

## 6. Reference Documents

- Hardware Manual
  H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual (REJ09B0403)
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package Ver.7.00 User's Manual (REJ10J2039)
  (The latest version can be downloaded from the Renesas Technology Web site.)
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