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## H8/300L SLP 系列

### 振荡稳定时间的设定 (H8/3867)

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#### 要点

说明关于时钟稳定前 CPU 和外围功能的待机时间（振荡稳定时间）的指定方法。

#### 动作确认器件

H8/3867

#### 目录

1. 设定方法 .....	2
2. 流程图 .....	5
3. 程序清单 .....	6

## 1. 设定方法

在通过特定的中断解除待机模式、时钟模式并转移到激活模式的情况下，指定时钟稳定前的 CPU 和外围功能的待机时间。必须根据工作频率指定长于振荡稳定时间的待机时间。

### 1.1 待机时间的设定

通过设定系统控制寄存器 1 (SYSCR1) 的待机定时器选择 2~0 (STS2~STS0)，进行待机时间的设定。

### 1.2 STS2~STS0 的说明

SYSCR1 的 STS2~STS0 的说明如表 1 所示。

表 1 STS2~STS0 的说明

SYSCR1			说明
位 6	位 5	位 4	
STS2	STS1	STS0	
0	0	0	待机时间 = 8,192 个状态 (初始状态)
0	0	1	待机时间 = 16,384 个状态
0	1	0	待机时间 = 32,768 个状态
0	1	1	待机时间 = 65,536 个状态
1	0	0	待机时间 = 131,072 个状态
1	0	1	待机时间 = 2 个状态 (外部时钟输入模式)
1	1	0	待机时间 = 8 个状态
1	1	1	待机时间 = 16 个状态

【注】在输入外部时钟的情况下，必须在进行模式转移前将待机定时器选择设定为外部时钟输入模式。另外，在不使用外部时钟的情况下，不要设定为外部时钟输入模式。

### 1.3 晶体振荡时的工作频率和振荡稳定时间

对于晶体振荡时的工作频率和 STS2~STS0 设定值的待机时间如表 2 所示。设定 STS2~STS0，使待机时间长于振荡稳定时间。

表 2 晶体振荡时的工作频率和振荡稳定时间

(单位: ms)

STS2	STS1	STS0	待机时间	2MHz	1MHz	0.5MHz
0	0	0	8,192 个状态	4.1	8.2	16.4
0	0	1	16,384 个状态	8.2	16.4	32.8
0	1	0	32,768 个状态	16.4	32.8	65.5
0	1	1	65,536 个状态	32.8	65.5	131.1
1	0	0	131,072 个状态	65.5	131.1	262.1
1	0	1	2 个状态 (禁止使用)	0.001	0.002	0.004
1	1	0	8 个状态	0.004	0.008	0.016
1	1	1	16 个状态	0.008	0.016	0.032

### 1.4 外部时钟的情况

建议使用 STS2="1"、STS1="0"、STS0="1" 的设定。也能使用其他的设定，但是对于 STS2="1"、STS1="0"、STS0="1" 以外的设定，有可能在待机时间结束之前开始运行。

## 1.5 振荡稳定时间

振荡稳定时间的 AC 特性如表 3 所示。

表 3 振荡稳定时间的 AC 特性

项目	符号	适用管脚	测量条件	标准值			单位	参照图
				min,	typ.	max		
振荡稳定时间	$t_{rc}$	OSC <sub>1</sub> , OSC <sub>2</sub>	图 1 的情况, $V_{CC} = 2.2 \sim 2.5V$	—	20	45	us	图 1* <sup>1</sup>
			图 1 的情况, $V_{CC} = 2.2 \sim 2.5V$		0.1	8	ms	图 1
			上述以外	—	—	50	ms	
振荡稳定时间	$t_{rc}$	X <sub>1</sub> , X <sub>2</sub>	—	—	2.0	s	—	

(包含  $V_{CC}=1.8 \sim 5.5V$ 、 $AV_{CC}=1.8 \sim 5.5V$ 、 $V_{SS}=AV_{SS}=0.0V$ 、 $T_a=-20 \sim +75^\circ C$ 、子激活模式)

【注】\*1 不使用内部电源降压电路

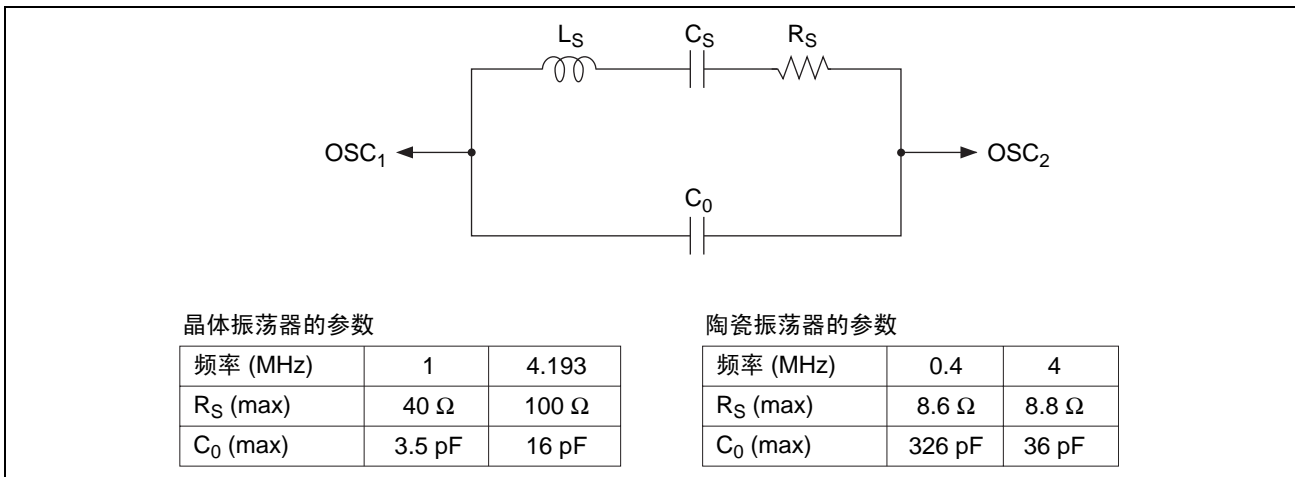


图 1 振荡器的等效电路

## 1.6 振荡稳定时间的设定例

### (1) 功能

从激活（高速）模式转移到时钟模式，在等待 250ms 后通过定时器 A 中断解除时钟模式，转移到激活（高速）模式。从时钟模式转移到激活（高速）模式时，将时钟稳定前的 CPU 和外围功能的待机时间设定为 8 个状态。

### (2) 注意事项

本设定例子中，在通过定时器 A 中断解除时钟模式时，禁止定时器 A 中断处理中的定时器 A 中断请求。所以，在从激活（高速）模式转移向时钟模式、然后通过定时器 A 中断解除时钟模式并且转移到激活（高速）模式时结束。

### (3) 时钟模式

#### (a) 向时钟模式的转移

在激活模式、子激活模式中，当系统控制寄存器 1 (SYSCR1) 的软件待机 (SSBY) 为 "1"，并且定时器模式寄存器 A (TMA) 的内部时钟选择 3 (TMA3) 为 "1" 时，如果执行 SLEEP 指令就转移到时钟模式。在时钟模式中，定时器 A、定时器 F、定时器 G、异步事件计数器和 LCD（可选择运行/停止）以外的内部外围功能停止运行。只要供给规定的电压，就保持 CPU 和一部分内部外围功能的内部寄存器、内部 RAM 的内容，并且 I/O 端口保持转移前的状态。

#### (b) 时钟模式的解除

通过中断 (IRQ<sub>0</sub>、WKP<sub>7</sub>~WKP<sub>0</sub>、定时器 A、定时器 F、定时器 G) 和  $\overline{\text{RES}}$  管脚输入进行时钟模式的解除。

通过中断进行解除时，如果发生中断就解除时钟模式。通过 SYSCR1 的低速 ON 标志 (LSON) 和系统控制寄存器 2 (SYSCR2) 的中速 ON 标志 (MSON) 的组合，在 LSON="0" 并且 MSON="0" 时，转移到激活（高速）模式；在 LSON="0" 并且 MSON="1" 时，转移到激活（中速）模式；在 LSON="1" 时，转移到子激活模式。转移到激活模式时，在经过由 SYSCR1 的 STS2~STS0 设定的时间后给整个 LSI 提供稳定的时钟，开始中断异常处理。而且，在 CCR 的 I 位为 "1" 或者根据中断允许寄存器禁止接受相应中断的情况下，不解除时钟模式。

通过  $\overline{\text{RES}}$  管脚进行解除时，如果将  $\overline{\text{RES}}$  管脚设定为 "Low" 电平，系统时钟就开始振荡。如果在经过振荡稳定时间后将  $\overline{\text{RES}}$  管脚设定为 "High" 电平，CPU 就开始复位异常处理。而且，在系统时钟开始振荡的同时给整个 LSI 提供系统时钟。 $\overline{\text{RES}}$  管脚必须保持 "Low" 电平状态，直到系统时钟的振荡稳定为止。

## 2. 流程图



### 3. 程序清单

```

;*****
;*   H8/3867 Application Note
;*
;*   'Oscillator Settling Time -8 States'
;*
;*   Function : Oscillator Settling Time
;*
;*   External Clock : 6MHz
;*   Internal Clock : 3MHz
;*   Sub Clock      : 32.768kHz
;*****
;
;       .cpu          3001
;
;*****
;*   Symbol Definition
;*****
;
TMA     .equ          h'ffb0    ;Timer Mode Register A
SYSCR1  .equ          h'fff0    ;System Control Register 1
SYSCR2  .equ          h'fff1    ;System Control Register 2
IENR1   .equ          h'fff3    ;Interrupt Enable Register 1
IRR1    .equ          h'fff6    ;Interrupt Request Register 1
;
;*****
;*   Vector Address
;*****
;
;       .org          h'0000
;       .data.w      MAIN      ;No.0 Reset Interrupt(H'0000-H'0001)
;
;       .org          h'0008
;       .data.w      MAIN      ;No.4 _IRQ0 Interrupt(H'0008-H'0009)
;       .data.w      MAIN      ;No.5 _IRQ1 Interrupt(H'000A-H'000B)
;       .data.w      MAIN      ;No.6 _IRQ2 Interrupt(H'000C-H'000D)
;       .data.w      MAIN      ;No.7 _IRQ3 Interrupt(H'000E-H'000F)
;       .data.w      MAIN      ;No.8 _IRQ4 Interrupt(H'0010-H'0011)
;       .data.w      MAIN      ;No.9 _WKP0-_WKP7 Interrupt(H'0012-H'0013)
;
;       .org          h'0016
;       .data.w      TAINT     ;No.11 Timer A Interrupt(H'0016-H'0017)
;       .data.w      MAIN      ;No.12 AEC Interrupt(H'0018-H'0019)
;       .data.w      MAIN      ;No.13 Timer C Interrupt(H'001A-H'001B)
;       .data.w      MAIN      ;No.14 Timer FL Interrupt(H'001C-H'001D)
;       .data.w      MAIN      ;No.15 Timer FH Interrupt(H'001E-H'001F)
;       .data.w      MAIN      ;No.16 Timer G Interrupt(H'0020-H'0021)
;       .data.w      MAIN      ;No.17 SCI31 Interrupt(H'0022-H'0023)
;       .data.w      MAIN      ;No.18 SCI32 Interrupt(H'0024-H'0025)
;       .data.w      MAIN      ;No.19 A/D Converter Interrupt(H'0026-H'0028)
;       .data.w      MAIN      ;No.20 Direct Transfer Interrupt(H'0028-H'0029)
;
;*****
;*   MAIN : Main Routine
;*****
;

```



```

        .org      h'1000
;
MAIN:    .equ      $
        mov.w     #h'ff80,sp          ;Initialize Stack Pointer
        orc      #h'80,ccr          ;Interrupt Disable
;
        mov.b     #h'e7,r01 ;Initialize System Control Regsiter
        mov.b     r01,@SYSCR1
        mov.b     #h'f0,r01
        mov.b     r01,@SYSCR2
;
        bclr     #7,@IRR1
        mov.b     #h'80,r01
        mov.b     r01,@IENR1
;
        mov.b     #h'ff,r01
        mov.b     r01,@TMA
        mov.b     #h'1a,r01
        mov.b     r01,@TMA
;
        andc     #h'7f,ccr
;
        sleep
;
        nop
;
EXIT:    bra      EXIT
;
;*****
;*      TMAINT : Timer A Interrupt Routine
;*****
;
TAINT:   .equ      $
        bclr     #7,@IRR1
;
        mov.b     #h'00,r01
        mov.b     r01,@IENR1
;
        rte
;
        .end

```

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