8A3xxxx

Using an External Trigger for Loading/Latching ToD

Abstract

This document explains in detail the required steps to use the 8A3xxxx CLKs or GPIOs for loading/latching Time of Day (ToD). Both register locations and Timing Commander screenshots are shown. Contact Renesas support for clarifications, errors, or feedback regarding this document.

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1. Overview

The 8A3xxxx supports up to four independent ToD accumulators (DPLL0~3). There are several ways to load/latch each ToD accumulator, including using CLKs or GPIOs. When using CLKs/GPIOs for ToD loading/latching signals, actual values are pre-written or post-read from registers through a serial port. Any of the 8A3xxxx GPIOs can be used (configurable) and any of the CLKs can be used.

There is a read or write inaccuracy when using CLKs/GPIOs. This is because of the different clock domains used for sampling the CLK/GPIO and for loading/latching the ToD accumulator value. The two main contributors are the internal System clock (200MHz) and the ToD accumulator's FoD (Fractional Output Divider) clock (500MHz – 1GHz).

- **CLKn as a trigger:** uncertainty of a *compensated ToD value from ToD accumulator is ±(2 x FoD clock period)
- **GPIOn as a trigger:** uncertainty of a *compensated ToD value from ToD accumulator is ±(2 x FoD clock period) + (1 x system clock period)

*compensated is (ToD_value + 2ns) for a write (load) trigger and (ToD_value - 2ns) for a read (latch) trigger

1.1 FoD Configuration

The ToDs are incremented by the associated DPLL0~3's FoD. DPLL0/1 support a FoD frequency of 500MHz to 1GHz and DPLL2/3 support a FoD frequency of 500MHz to 750MHz when working with the ToD accumulators[1]. Configuration of the DPLLs and FoDs is done using the 8A3xxxx TCP and Timing Commander. The ToDs are timed from the FoD clock, but they work separately. One operation does not affect the other. Any value can be stored (write) or latched (read) from a ToD without affecting DPLL functionality. Figure 1 shows where the DPLL configuration and the TOD configuration exist in the GUI.

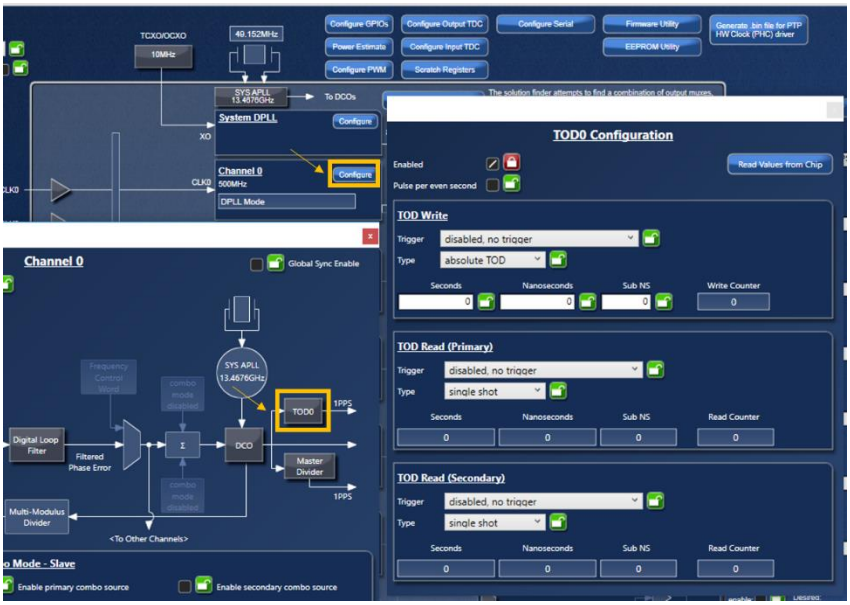

Figure 1. DPLL and TOD Configuration Locations in GUI

[1] All DPLLs support a FoD frequency of 500MHz to 1GHz when the TOD accumulators are not used.

2. ToD and GPIO/CLK Configuration

After the configuration of the FoD, you need to program the ToD of the DPLL and associated GPIO, assuming a GPIO is used as the trigger. Below is an example for DPLL1 ToD1 accumulator using GPIO3 as a load/trigger (highlighted numbers can be interchanged with applicable DPLL0~3 and/or GPIO0~15). Register names and how to modify them are shown, followed by Timing Commander screenshots performing the same function.

If a CLK is used as the trigger, Steps 1 through 3 can be skipped.

2.1 ToD Write

1. Write a 1 to GPIO_3.GPIO_OUT_CTRL_0.GPIO_FUNCTION_EN[0]. Enables GPIO3.
2. Write a 1010 to GPIO_3.GPIO_OUT_CTRL_0.GPIO_FUNCTION[7:4]. Selects ToD trigger input.
3. Write a 1 to GPIO_3.GPIO_TOD_TRIG.TOD_TRIG_1[1]. Selects ToD of DPLL1 to be triggered by GPIO3.

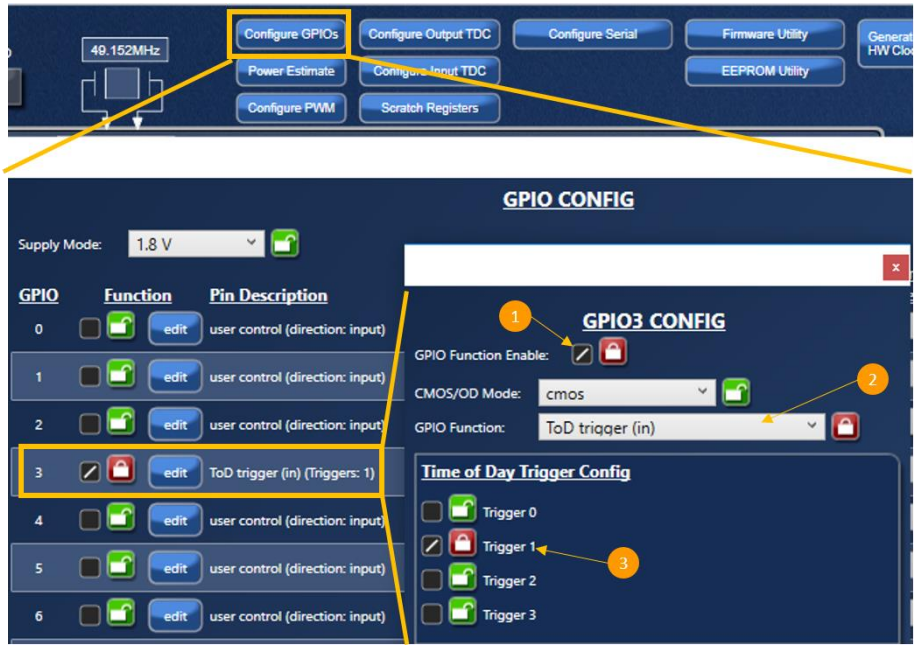

Figure 2. GPIO Configurations

4. Write a 1 to TOD_1.TOD_CFG.TOD_ENABLE[0]. Enables the TOD1 accumulator.
5. Writing to TOD_WRITE_1.TOD_WRITE_CMD.TOD_WRITE_SELECTION[3:0]:
   a. Write a 0110 to TOD_WRITE_1.TOD_WRITE_CMD.TOD_WRITE_SELECTION[3:0]. Selects the GPIO as the trigger.
   b. Write a 0010 to TOD_WRITE_1.TOD_WRITE_CMD.TOD_WRITE_SELECTION[3:0]. Selects the CLK as the trigger. CLK0 is chosen by default. To change the CLK input, write to TOD1_WRITE_REF_INDEX[3:0].
6. Write the 88-bit ToD value into TOD_WRITE_1.TOD_WRITE.SECONDS[87:40].NS[39:8].SUBNS[7:0]. Enters the Time of Day.

7. Rising Edge Occurrence:
   a. Cause a rising edge to occur on GPIO3. Value is written internally, and trigger select goes back to reset state.
   b. Cause a rising edge to occur on CLK0. Value is written internally, and trigger select goes back to reset state.
8. Read the ToD Write Counter at TOD_WRITE_1.TOD_WRITE_COUNTER.WRITE_COUNTER[7:0]. This counter increments to indicate completion.

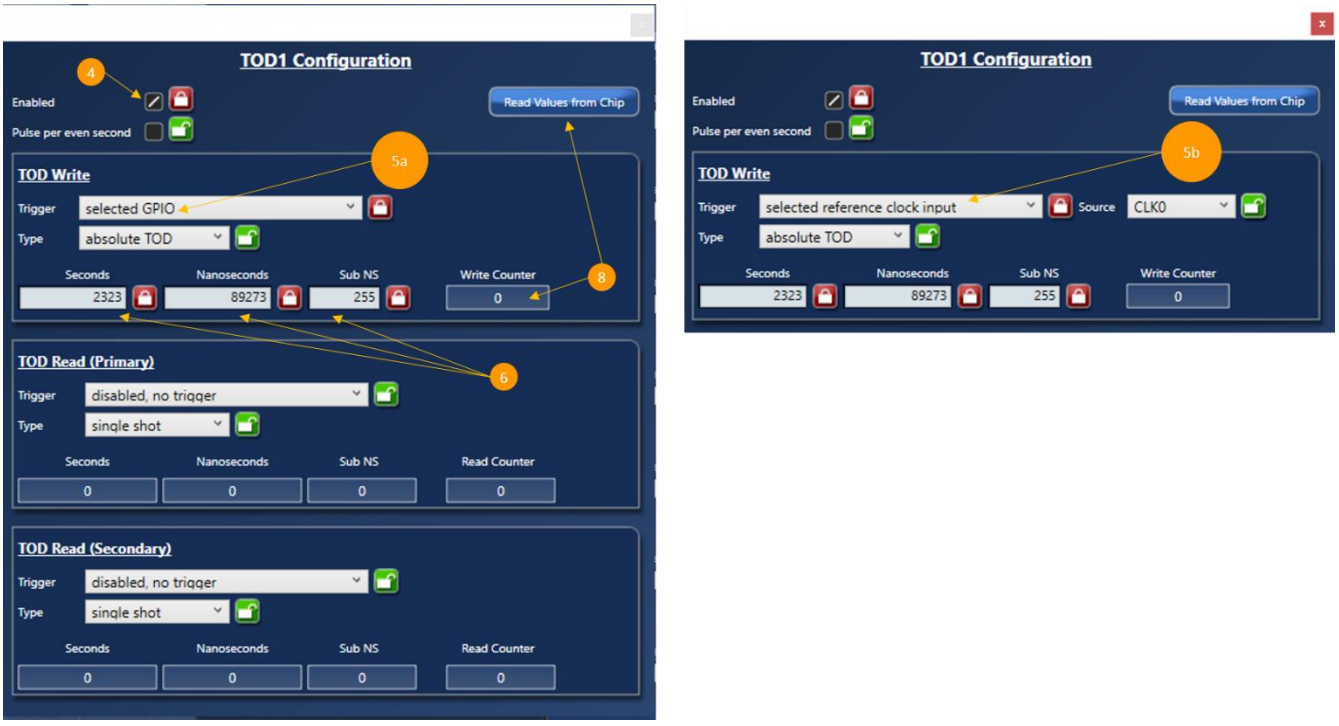

Figure 3. TOD1 Configuration - Write

2.2 ToD Read

9. Writing to TOD_READ_PRIMARY_1.TOD_READ_PRIMARY_CMD.TOD_READ_TRIGGER[3:0]
   a. Write a 0111 to TOD_READ_PRIMARY_1.TOD_READ_PRIMARY_CMD.TOD_READ_TRIGGER[3:0]. Selects the GPIO as the trigger. Keep the TOD_READ_PRIMARY_1.TOD_READ_PRIMARY_CMD.TOD_READ_TRIGGER_MODE[4] to single shot. The other option is continuous, which means you do not need to retrigger the next time.
   b. Write a 0011 to TOD_READ_PRIMARY_1.TOD_READ_PRIMARY_CMD.TOD_READ_TRIGGER[3:0]. Selects the CLK0 as the trigger. CLK0 is chosen by default. To change the CLK input, write to TOD1_READ_PRIMARY_REF_INDEX.
10. Ensure Steps 1-3 are still active. This step is skipped when using CLKx as a trigger.
11. Rising Edge Occurrence:
   a. Cause a rising edge to occur on GPIO3. The 88-bit TOD value is transferred to TOD_READ_PRIMARY_1.TOD_READ_PRIMARY and the trigger select goes back to reset state.
   b. Cause a rising edge to occur on CLK0. The 88-bit TOD value is transferred to TOD_READ_PRIMARY_1.TOD_READ_PRIMARY and the trigger select goes back to reset state.

12. Read the ToD Read Counter at TOD_READ_PRIMARY_1.TOD_READ_PRIMARY_COUNTER.READ_COUNTER[7:0]. This counter increments to indicate completion.

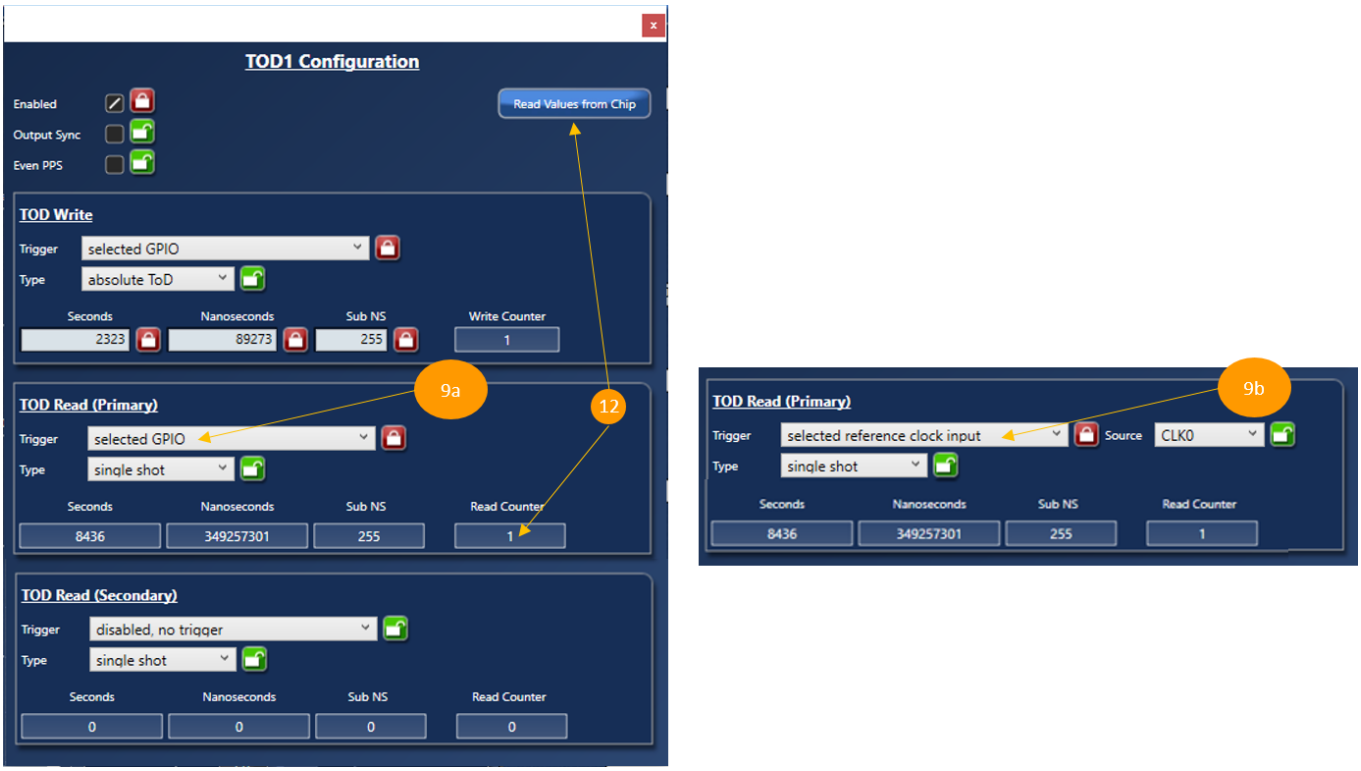

Figure 4. TOD1 Configuration - Read

3. Fixed Delays in ToD Loading (Write)/Latching (Read)

As previously mentioned there is an uncertainty of 1 x system clock period (200MHz) from the GPIO edge until the ToD value is loaded (written) or latched (read). If a CLK is used as the trigger, the system clock period uncertainty is not present. In addition, there is a fixed delay that may be applied for pre- or post-compensation of the ToD value, which is (ToD_value + 2ns) for a write (load) trigger and (ToD_value - 2ns) for a read (latch) trigger.

4. Revision History

Revision Date	Description of Change
Oct.27.20	Initial release

5. References

8A3xxxx Family Programming Guide v4.7

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