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Using the Reference Layout

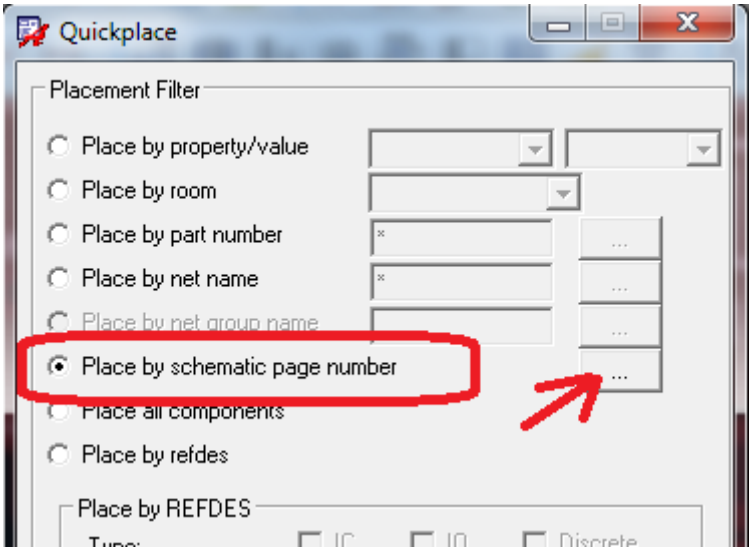
The P9025AC-R-EVK reference layout is a simplified two-layer design optimized for high-performance, small-size, and ease-of-use. Its purpose is to minimize design-in effort and risk by providing a proven solution that can be imported into an existing system design. When circumstances permit, it is highly recommended to copy the reference layout. This will accelerate design time to market at final product level.

Importing the Reference Layout

The P9025AC-R-EVK reference design was created using Cadence PCB design software. This software has been used to generate layout modules which can be rapidly deployed onto PCB designs using Cadence OrCAD CIS and Cadence Allegro PCB Editor. The P9025AC-R-EVK Allegro layout module is labeled P9025AC-R-EVK.mdd and can be downloaded at www.idt.com/P9025AC-R-EVK. It will load into an existing or new PCB design file by following these instructions:

1. Use or copy the P9025AC-R-EVK schematic file (.dsn) and export the netlist to a PCB file.
2. Move the file P9025AC-R-EVK.mdd to the same directory as the PCB design file.
3. Import the netlist into the PCB file (.brd).
4. Open the PCB design file (.brd) and click on the menu Place→Quickplace…
    a. Select Place by Page Number and select the page the P9025AC circuitry resides on.

Figure 1. Cadence Quickplace Option Box used for Placing the IDT Layout Module by Page Number



    b. Click Place. Click Ok.
5. Select the parts that were placed from the schematic that matches the schematic used from the P9025AC-R-EVK.
    a. In the Find Filter, select Symbols, then left click and drag to highlight all of the components that were just placed.
    b. Right click on any of the highlighted parts and select “Place Replicate Apply→Browse…”
    c. Select the P9025AC-R-EVK.mdd file and select Ok.
    d. Components should be matched. If unmatched, manually identify and match component reference designators based on schematic location.
6. Enter the coordinates (x,y location) in the command window where the P9025AC circuit should be located at, or left click where the P9025AC should be placed.

Connecting a Load

The reference board layout has been designed such that the DC output is easily accessible when being imported on to a system board. Traces should be connected directly to the OUT and GND vias on the top or bottom layer, and routed to the load. Wide, low-impedance traces are recommended to minimize the DC voltage drop on its way to and from the load. To reduce ripple voltages or improve transient performance, increase the capacitance on Vrect and OUT nodes.

Connecting Inputs / Outputs

All input and outputs on the reference board have been placed near the edges of the reference layout such that they can be easily connected to other parts of the system board. After placing the module in the specific design, use the labeled vias as connection points for new traces on either the top or bottom layer.

Manufacturing Notes

PCB should be made with a minimum of 1oz copper foil weight per square foot or heavier. For better thermal performance, 2oz copper thickness is recommended.

Additional Resources

All support files and collateral for the P9025AC-R-EVK reference board can be found at http://www.idt.com/P9025AC-R-EVK. Files include: schematics, layout files, datasheets, user guides, etc.

Custom Layout Guidelines

The P9025AC wireless power receiver is an integrated device consisting of multiple high-power blocks along with noise sensitive circuits; all controlled by a state-machine. When designing the printed circuit board (PCB), there are multiple considerations and often some trade-offs associated with managing the critical current paths. In order to optimize the design, components should be placed based on circuit function to guarantee best performance when the schematic is implemented into a PCB design. Furthermore, the thermal management of the application is important to the product's performance and should be optimized during PCB design. By following the guidelines set forth in this document, efficient operation will be obtained for each circuit function.

At the time that the layout is started, the following guidance should be used to place the most critical parts in order of priority. There are three main categories of circuitry: Power Circuits, Sensitive Circuits, and Non-Sensitive Circuits.

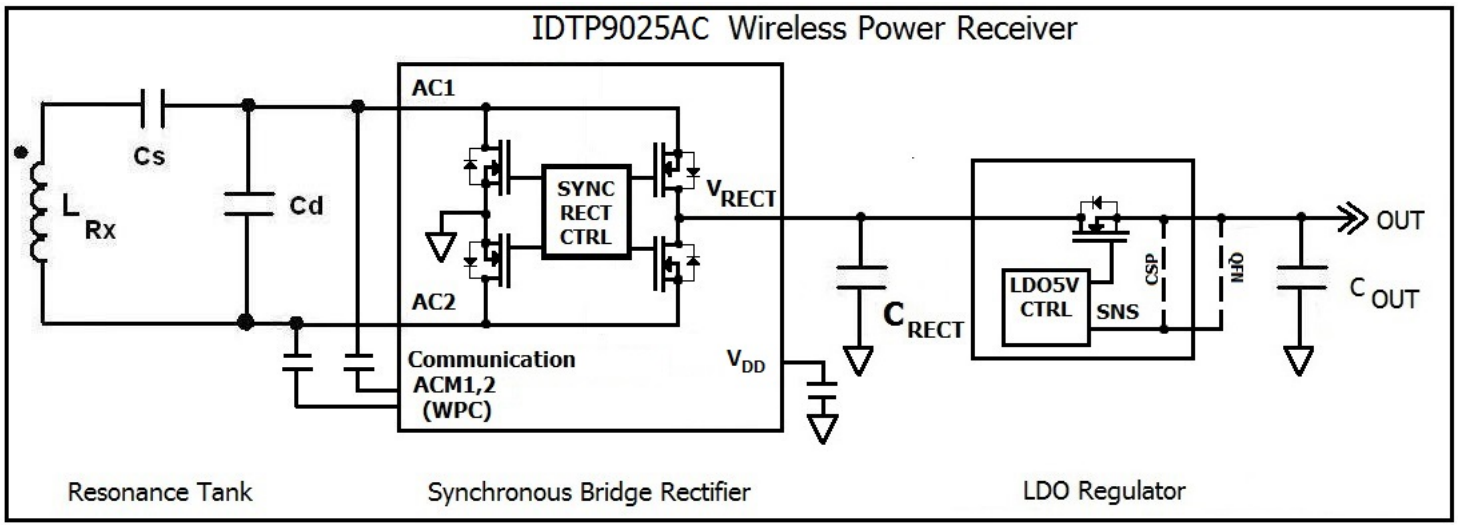
Layout Priority Checklist

1. Route the power connections wide (50-200mils or wider as space allows) and on the same side of the PCB as the P9025AC (Vrect, AC1, AC2, OUT, LC node, and GND).
2. Use the next closest layer to the P9025AC device as a solid GND plane.
3. Avoid unnecessary layer transitions of the power connections (Vrect, AC1, AC2, OUT, LC node, and GND). Use 6 – 8 vias for any layer transition.
4. Attempt to place the P9025AC as close as possible to the center of the board.
5. Connect as much copper as possible to the EPAD (use direct connection). Use multiple GND planes to connect to EPAD for multi-layer PCBs. Have a solid, continuous GND plane surrounding the EPAD on as many sides as possible.
6. Try to avoid running traces in parallel with the EPAD on the bottom or inner layers to promote heat dissipation.
7. Follow the placement and routing suggestions outlined in the remainder of this document.
8. Use low ESR resonance capacitors (Cs) to decrease losses in the LC and AC1 current path. IDT recommends using components with less than 300mΩ of ESR at 100kHz operating frequency.

Power Circuits

The main power circuits of the P9025AC device are the resonance tank, the synchronous bridge rectifier and the LDO linear regulator. A Secondary power circuit is the VDD regulator.

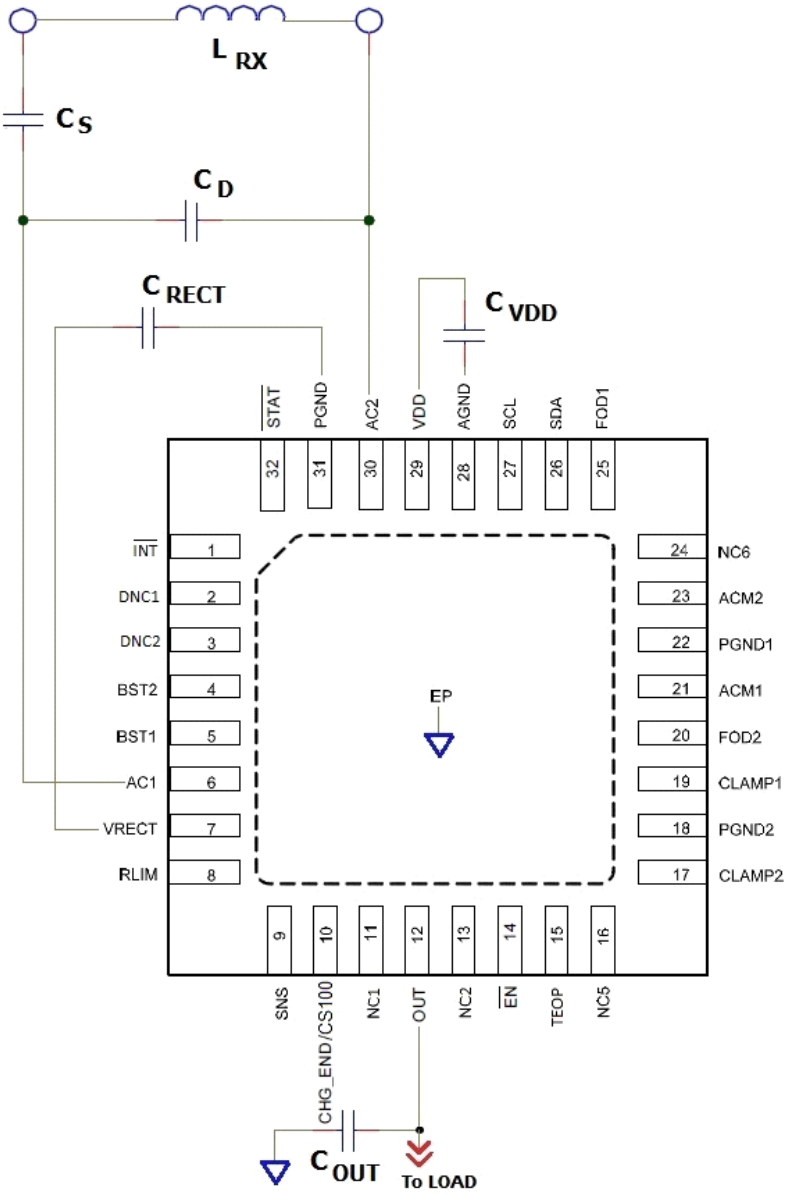
Figure 2. P9025AC Power Blocks



As soon as the final shape of the PCB has been determined (based on system constraints), the connection points for the receiver coil (L_{RX}) should be determined. Next, the P9025AC should be placed as close to the center of the PCB as possible. The orientation of the device should be determined based on the ability to route connections and place the necessary components in the following order of priority: Rectifier capacitors (C_{RECT}), Bootstrap capacitors: BST1, BST2, Resonance Capacitors (C_S, C_d), VDD capacitor, OUT capacitors (C_{OUT}), and these capacitors should be placed with equal precedence (Clamp1, Clamp2, ACM1, ACM2

The main power current path is considered the connection from the RX coil to AC2, the Cs capacitors to AC1, GND, V_{RECT}, and OUT connections. The optimal P9025AC orientation relative to the receiver coil (L_{RX}) and output connector physical locations are presented in Figure 3.

Figure 3. P9025AC QFN (VFQFPN) Package. Recommended orientation based on Rx coil location and generic placement guide for some critical components (Note, not all necessary connections are shown in this figure, refer to the P9025AC datasheet Typical Application Drawing for a complete diagram of recommended connections). Trace widths not to scale. All GND pins should be connected to GND.



VFQPFN Package Layouts

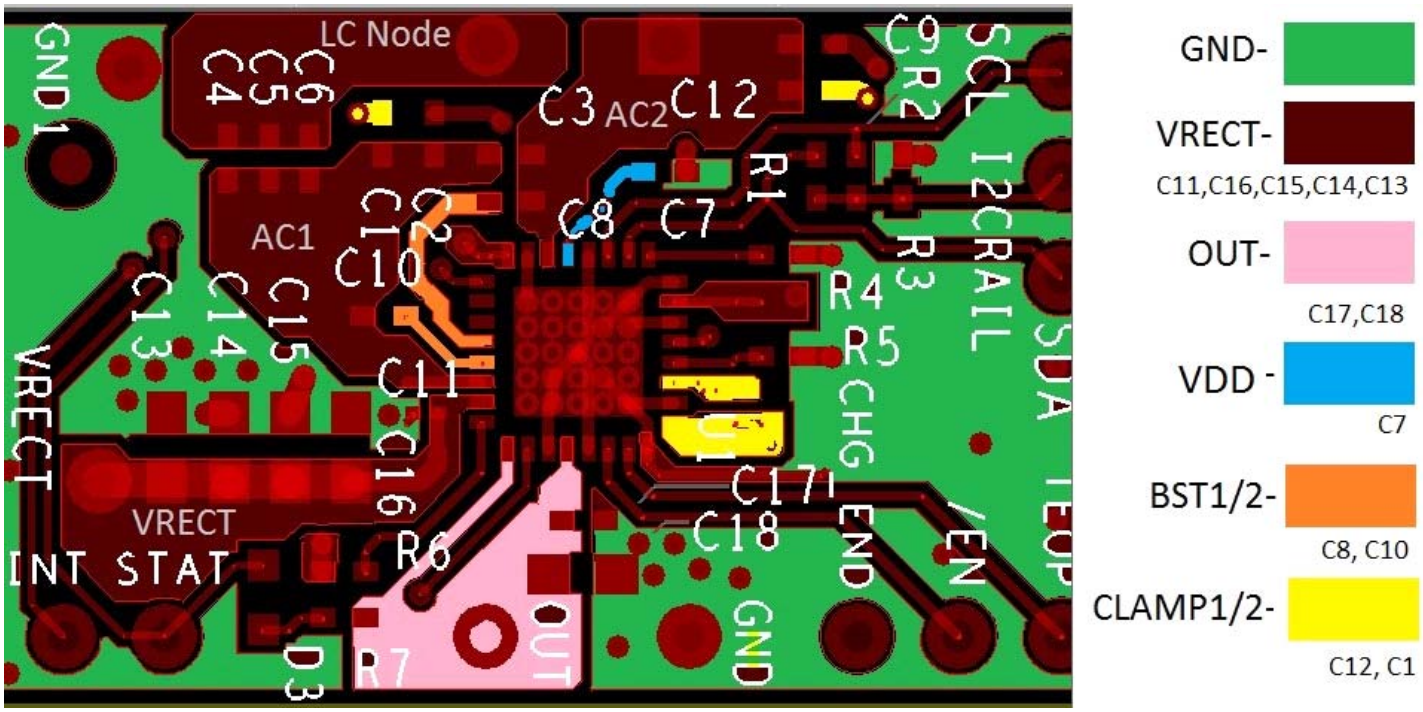
The QFN PCB designs are easily accomplished using 2-layers. Components should be placed in the following order (while leaving adequate room to route AC1, AC2, VRECT):

1. VRECT capacitors
2. OUT
3. VDD
4. BST1 / BST2

5. Cs
6. Cd
7. Clamp1 / 2
8. ACM1 / 2
9. RLIM and FOD resistors

The following layout images should be used to guide PCB designs. For convenience, the QFN schematic that corresponds to the QFN layout images is at the bottom of this application note. The VRECT capacitors should be placed first. The bridge rectifier output is physically located from PGND pin 31 to VRECT pin 7; therefore the VRECT capacitors are ideally placed such that they are oriented with the GND side facing pin 31 (PGND with current flowing from VRECT capacitors through the EPAD to the PGND (pin 31)) and the VRECT side routed on the P9025AC side of the PCB. OUT capacitors should be located as close as possible to the P9025AC with a wide (30-200 mils or wider as space permits) connection to the VRECT capacitor GND and EPAD. The VDD capacitor needs to be placed as close as possible to the IC, along with the BST capacitors. The EPAD should have an array of vias (10-12mil diameter hole spaced evenly) and be directly connected to heat spreading GND plane(s).

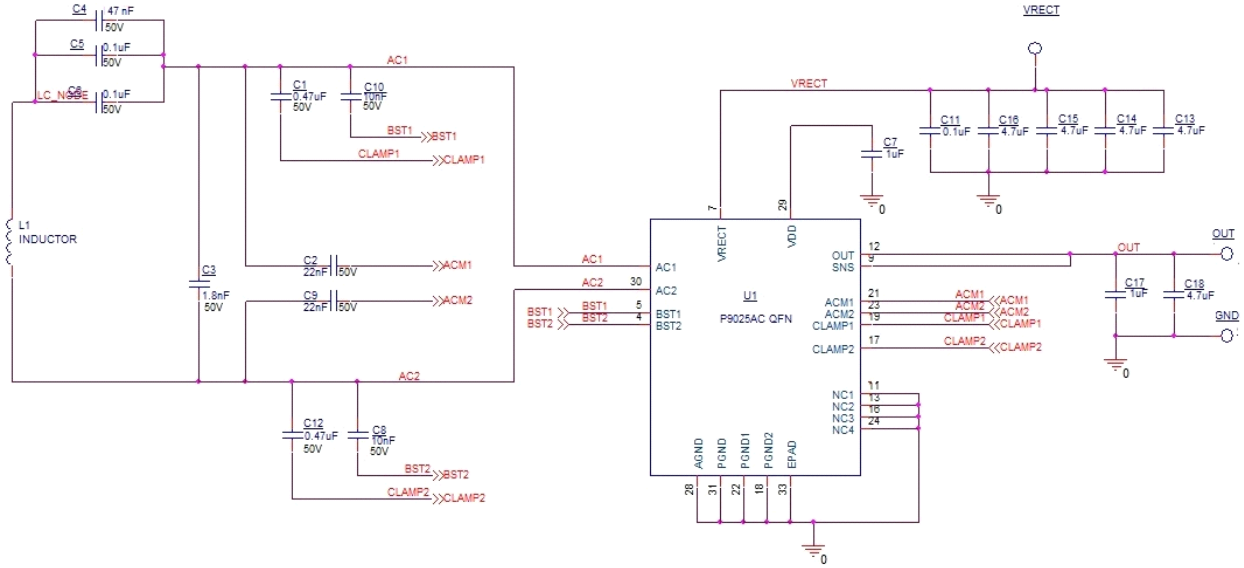
Figure 4. P9025AC QFN IC Side Layout Recommendations



VRECT and OUT Capacitors

The first components to place should be the VRECT output capacitors due to the high current charging at the power transfer operating frequency. The power transfer switching results in dV/dt voltage steps high enough for consideration as noise generating signals at the AC1 and AC2 nodes and high current surges during normal operation. The ideal placement of the VRECT capacitors is to have them straddling the VRECT pin (pin 7) and the PGND pin (pin 31). Below is a section from the P9025AC-R-EVK schematic portraying the Power Circuits (Figure 5), and this figure will be used for reference.

Figure 5. P9025AC Power Section, QFN EVK Board Schematic (Note, not all pins are shown in this figure, refer to the P9025AC datasheet Pin Description for the complete list of pins and recommended connections)

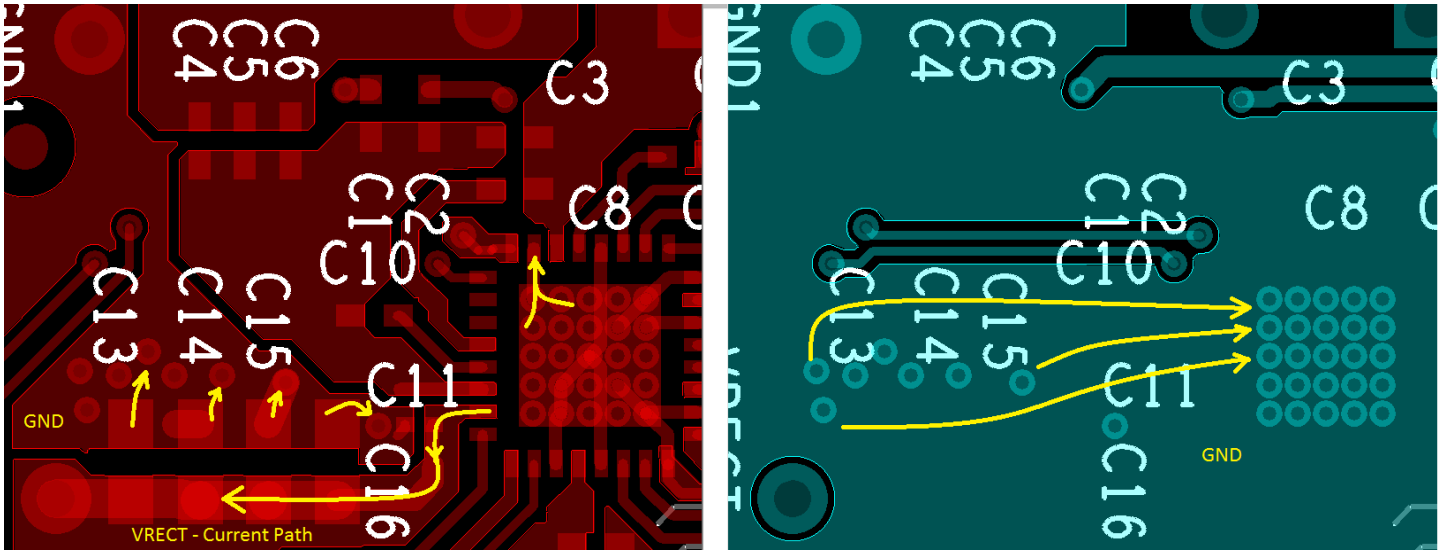


In the following layout image (Figure 6), the placement of the VRECT capacitors (C11, C16, C15, C14, C15) will be detailed. The small 0201 0.1uF capacitor is placed first and closest, followed by the larger bulk capacitors. It is important to keep the area of the current loop that conducts the AC current from the synchronous bridge rectifier to the VRECT capacitors and GND (PGND) to a minimum – helping to keep ripple voltages and GND bounce minimized.

In the reference layout, the GND current traverses from the VRECT capacitor GND plates to a solid GND plane by using eight vias and returns to the PGND (pin 31) through the EPAD thermal vias. VRECT capacitors should be close to the P9025AC. If the design is space-constrained, capacitors C13 and C14 may be located slightly farther from the P9025AC as long as the other capacitors from VRECT to GND are adjacent to the IC. In these cases, the capacitors may be rotated relative to the rest of the VRECT capacitors or placed farther away as long as they are within 30 mm (1.2") of the P9025AC device.

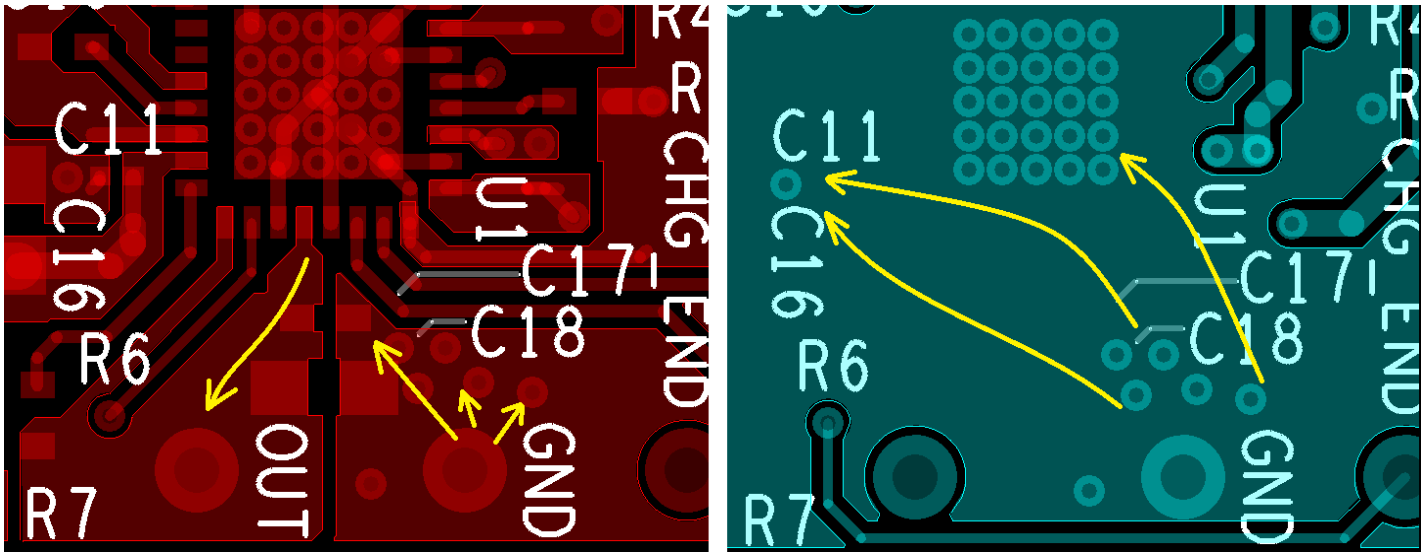
The copper planes should be as wide as possible for the connections for VRECT from the IC to the capacitors and back to GND (50 – 200 mils or wider as space permits). The reason for the number of capacitors is to maintain a minimum of 10uF of effective capacitance when 5 to 7 V of DC bias is applied across the VRECT capacitors (see DC-bias characteristics of selected capacitors).

Figure 6. P9025AC Physical Layout from QFN EVK PCB (top and bottom layers), VRECT Capacitor Placement and Current Path



Next, the OUT capacitors C17 and C18 should be placed very close to the P9025AC for optimal performance. The traces connecting these capacitors should be wide (50 – 200 mils as space permits). There should be many GND vias (at least 5) for the layer transition; again the loop area is minimized to improve the voltage accuracy and reduce ripple. The OUT current GND return needs to have direct connections to the VRECT capacitor GND and the EPAD so the output current can return to the source (VRECT GND).

Figure 7. P9025AC Physical Layout from QFN EVK PCB (top and bottom layers), OUT Capacitor Placement and Current Path



Effort should be made to keep the bottom layer (or additional internal layers) free from unnecessary connections or routing in the vicinity of the P9025AC. Since it is impractical to not have connections on additional layers, it is recommended to have them escape from the P9025AC in straight lines so that the continuous connections can be kept as solid as possible.

The outer layers of the PCB will be the most effective at transferring heat from the board to the ambient air or other objects. But, it should be realized that spreading the heat into internal layers is also effective at lowering the operating temperature, since the thermal resistance of the PCB's FR-4 material has fairly small resistance to heat flow along the z-axis because the board is thin.

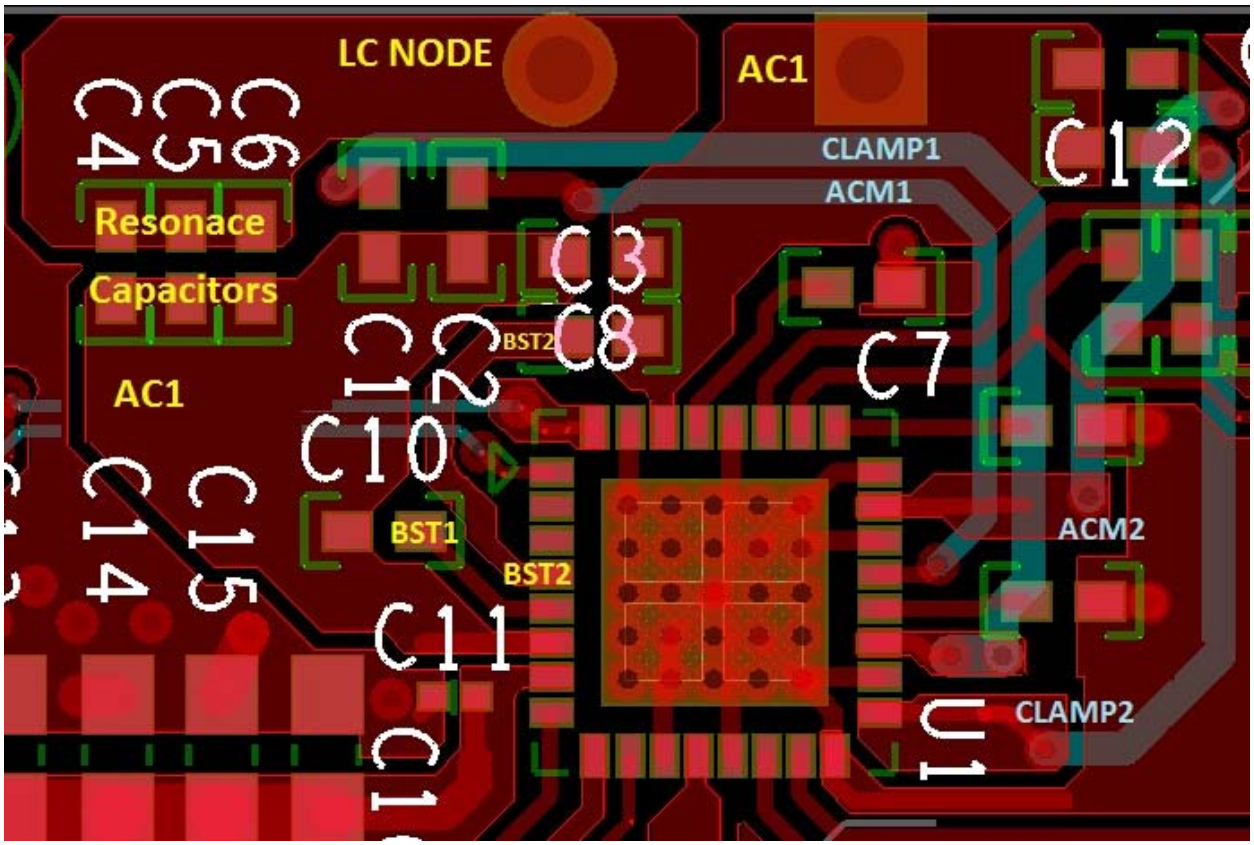
Internal layers are able to effectively spread heat horizontally when they are not interrupted by traces and through-holes. The heat on the internal layers will spread to outer layers for dispersion to the ambient environment in direct proportion to the temperature gradient and area of the PCB.

An ideal layout will result in the entire PCB being close to the same temperature. To achieve this, all board layers should have planes that are fairly continuous and in direct contact with heat-generating nodes (such as P9025AC vias-in-pad). The required nodes to which heat-spreading planes should be connected are PGND, VRECT, AC1, AC2, and OUT. The other connections will spread heat due to natural thermodynamics, but the listed nodes contact the primary heat sources of the P9025AC.

BST, CLAMP, ACM, Resonance Capacitors

Next the VDD, BST1 & BST2, Clamp1 & Clamp2, resonance (Cs), parallel (Cd) capacitors and the communication components will be addressed.

Figure 8. P9025AC EVK Resonance, BST1/2, CLAMP1/2, ACM1/2 Placement and Routing



In Figure 8, the key points of emphasis are the large surface areas connected to the P9025AC pins. Components should be placed in a manner that allows adequate room for the VRECT, OUT, AC1, and AC2 nets to be routed with copper planes that are as wide as possible (50 – 200 mils as space permits). When using internal layers to route these nets, it is advised that they remain as wide as possible and use multiple vias (5 or more) for each and every layer transition.

The next components recommended for placement are the BST1 (C10) and BST2 (C8) capacitors. These should be placed near the respective P9025AC pins and in series to the AC1 and AC2 nets. Connections involving the BST capacitors should be completed using 0.3 to 0.5 mm (12 – 20 mil) wide traces and two vias are recommended for layer transitions as space permits. This is important because these capacitors provide the power for the high-side synchronous rectifier FET gate drive signals. Low impedance routing will allow the FETs to be turned on at the optimal time for most efficient operation.

Next, the CLAMP1 (C1) and CLAMP2 (C12) capacitors should be placed. These connections should be routed at 15 – 30 mils wide as space permits and not be more than 10 mm from the P9025AC device.

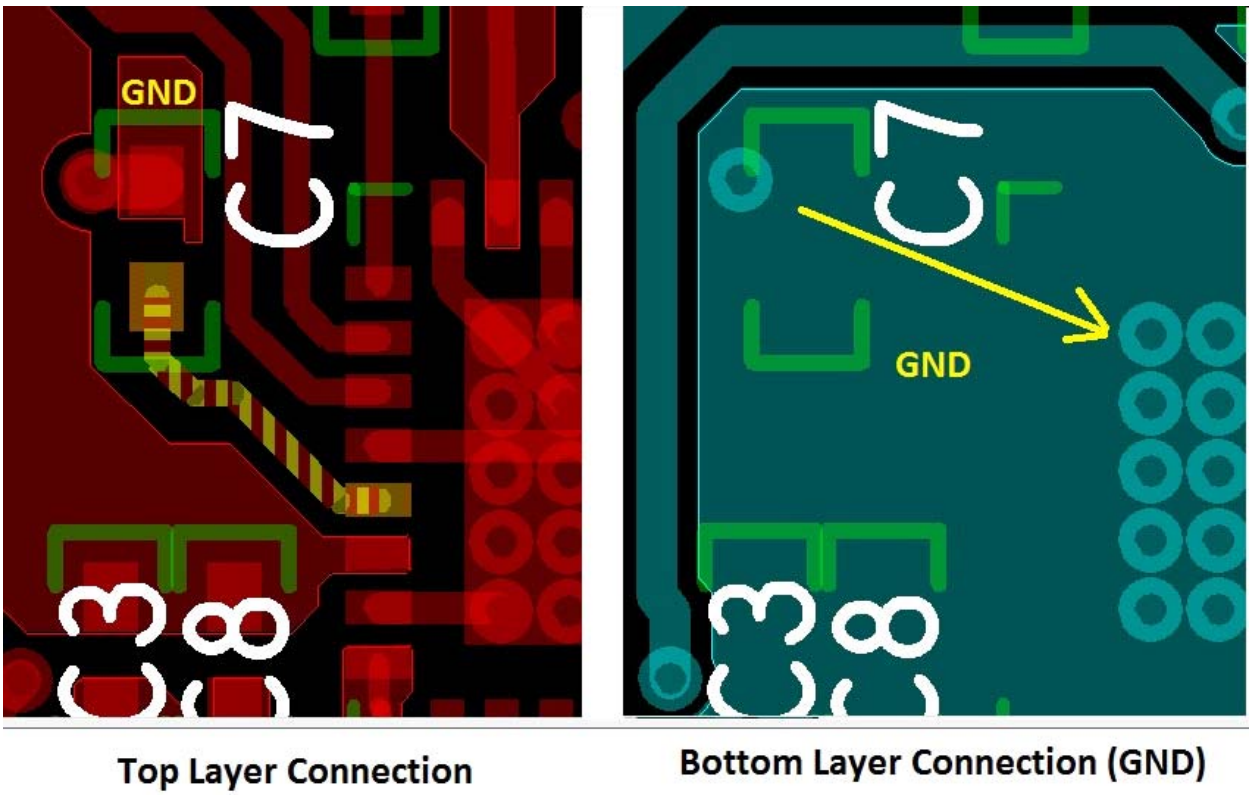
Next, the ACM1 (C2) and ACM2 (C9) capacitors (WPC capacitive communication generating signals) are placed conveniently close to the respective pins and AC1 and AC2 connections. These may be routed at widths of 0.3 to 0.5mm (12 – 20 mils) as space permits.

The Cd (C3) capacitor is recommended for placement next and should be located at a convenient location across the AC rectifier inputs between the P9025AC and the Rx coil. The Cs (C4, C5, C6) resonance capacitors should be placed in series with the P9025AC and the Rx coil. For best performance the connections to these capacitors should be at least 2.5 mm wide (100 mils) and should be considered for use as electrical and thermal conductors (similar to AC2). If this width is not possible, multiple parallel connections on various PCB layers should be considered. Any layer transitions should utilize 4 – 6 vias at each transition. The AC1 and AC2 traces will carry all of the load current from the Rx coil to the synchronous rectifier and must be routed accordingly.

VDD Capacitor

The VDD capacitor is used to stabilize a voltage supply used internally to the P9025AC and must be located close to the P9025AC. Optimal placement is directly across VDD pin 28 and AGND pin 29. To make room for routing, the VDD GND return may be routed on the bottom or inner layer GND planes directly to the EPAD, and then to the AGND pin. The VDD capacitor should be at least 1uF, but it is recommended that there is an effective capacitance of 3uF at 5 VDC for best performance across all load conditions. Short component-side connections to the respective pins are recommended for best performance.

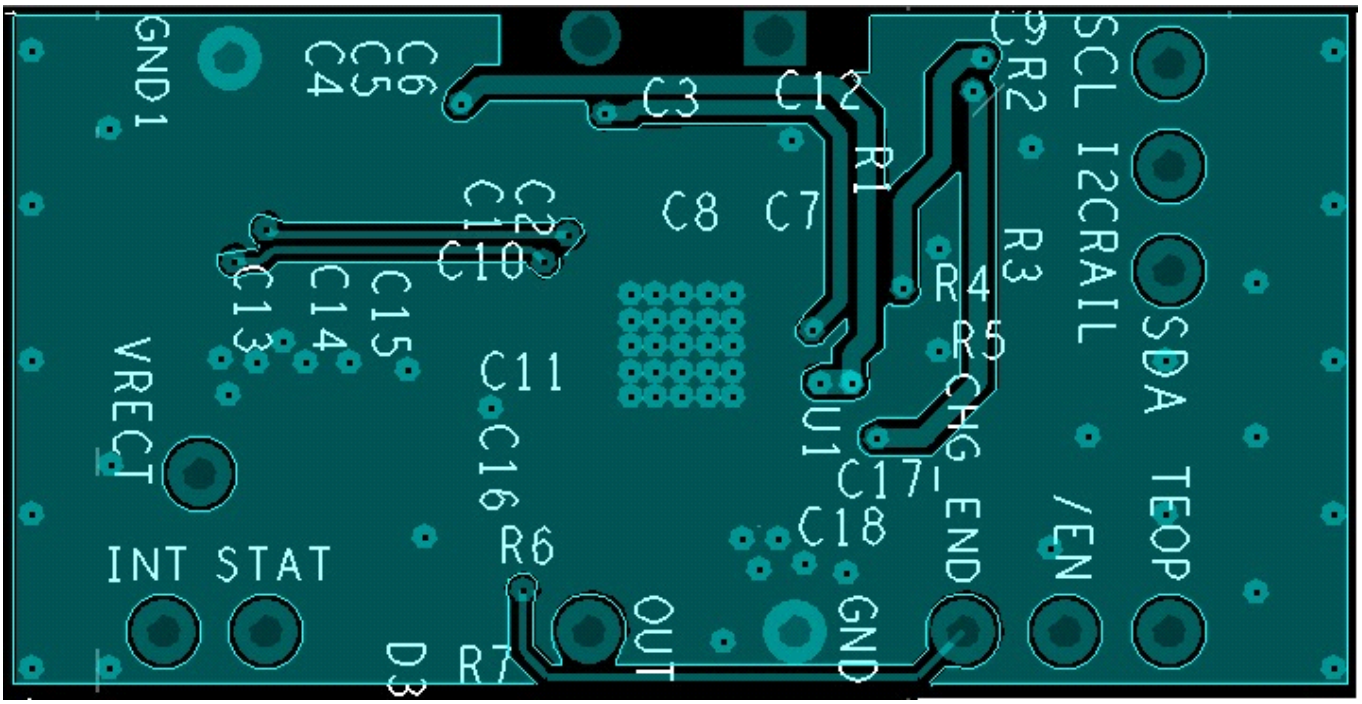
Figure 9. P9025AC VDD Capacitor Routing



EPAD GND Connection

Thermal vias contacting the EPAD offer excellent heat transfer paths to spread the heat developed within the IC to the surrounding copper area of the PCB allowing the P9025AC to operate at a lower temperature. For best performance, the GND plane should be on the bottom layer of the PCB while being free from obstructions in the form of too many vias or traces. Multi-layer designs should use a redundant parallel GND plane on the first adjacent layer to the component side as well as the bottom layer of the PCB (see Figure 10).

Figure 10. P9025AC QFN Bottom Layer layout



Observe the bottom layer of the layout: traces need to be located as far as possible from the EPAD in order to promote heat flow paths to maintain low operating temperatures.

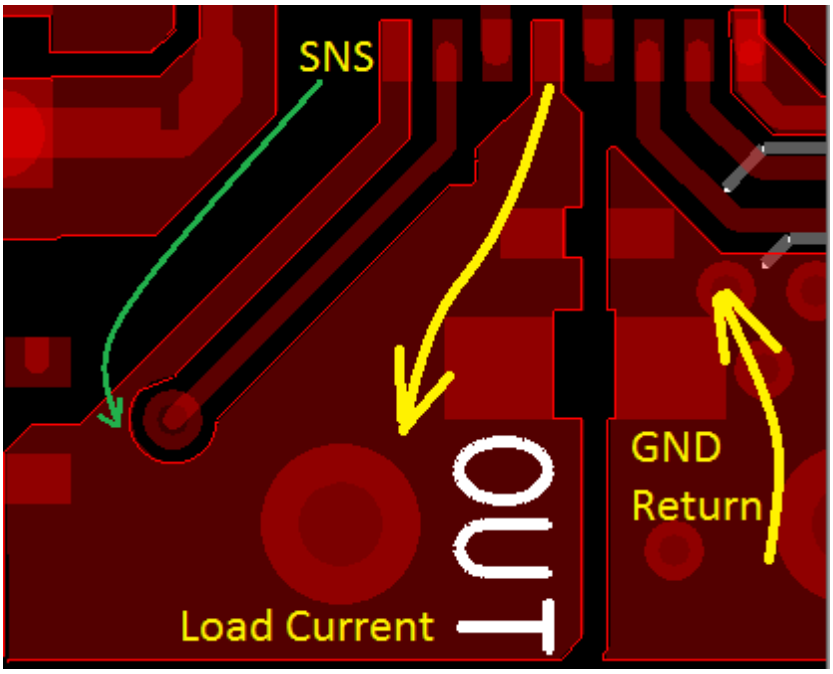
The EPAD should be directly connected to a solid, continuous GND plane. All of the PGND and AGND pins of the device (and E-PAD) should be in full contact with the GND plane. For improved thermal performance in boards with more than two layers, it is recommended to use multiple ground planes. Connections to these planes should be direct and not thermally relieved. Additional thermal performance improvements can be made by connecting large copper planes to the power pins and component-side connections of the P9025AC device.

Sensitive Circuits

The sensitive circuits refer to noise sensitive circuits that should be referenced to GND in the ‘Quiet’ GND area and they include the Rlim (R83) resistor and the FOD resistors (R64 and R66). For additional FOD related functions and programming methods, consult the datasheet and Application Note AN-814A for detailed instructions and AN-889 for simplified FOD tuning methods.

An additional noise sensitive signal is the SNS signal. This should be routed away from the noise areas (Rectifier and resonance) and make a single Kelvin type connection as close as possible to the point of load, or at the connector used to carry the output power to the rest of the application circuitry. The P9025AC will adjust the OUT voltage to compensate for conduction voltage drops up to the point that SNS is merged with the OUT pin. This should take place on the same PCB that the P9025AC is attached to and should occur within a 50 mm (2") of the P9025AC.

Figure 11. SNS Kelvin Sense Connection to OUT (do not share connection with main current path)



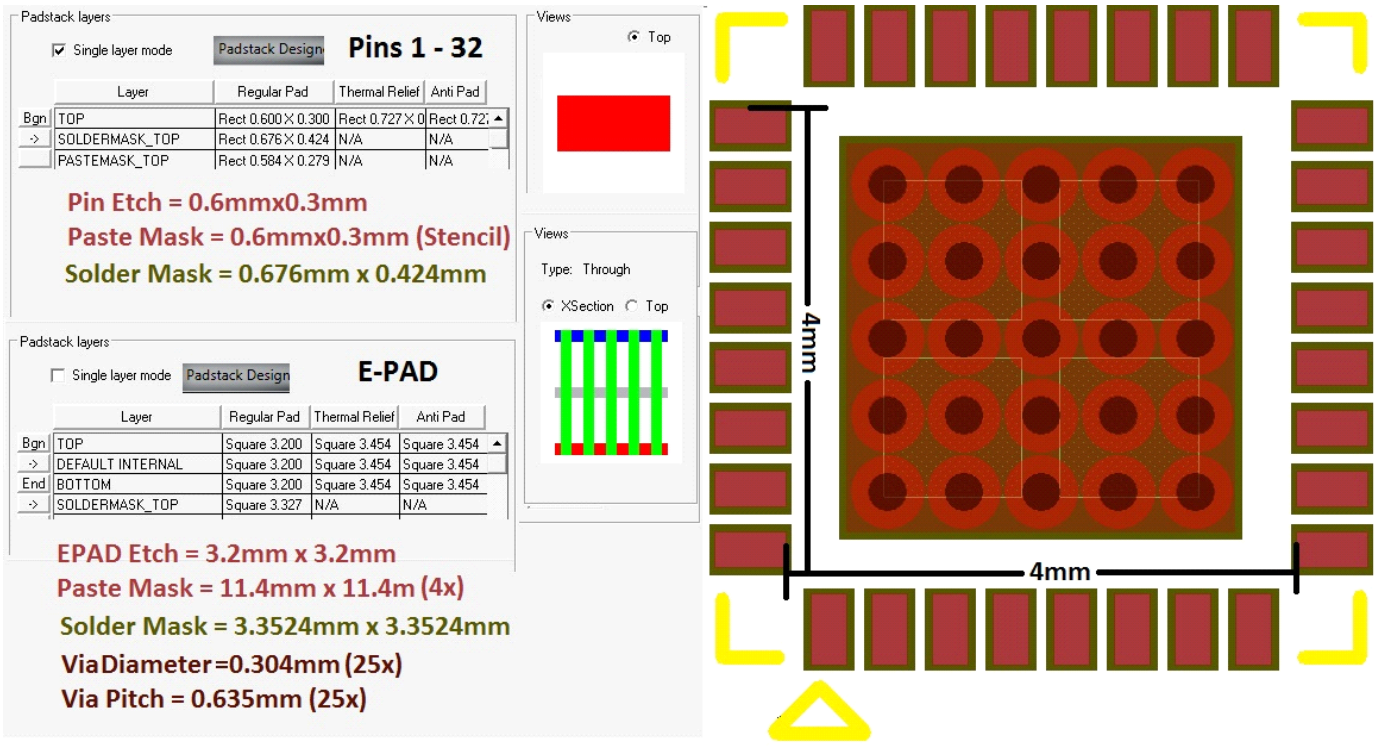
Non-Sensitive Circuits

The remaining components and pins that have not been mentioned are regarded as non-sensitive circuits and the placement and routing of these nodes is not considered critical to performance or functionality. They simply need to be present and properly connected. They should be connected last, and should try to accommodate the needs of the other circuits when a trade-off needs to be made. In most cases, 0.127 mm (5 – 8 mils) wide traces and any method of connectivity will suffice to complete the circuit.

PCB Footprint Design

The P9025AC package is a 0.5 mm pitch VFQFPN device and the PCB footprint is an important factor in production assembly yields (see Figure 12). Improper footprint design can lead to solder shorts or open circuits. Poor PCB footprint design can also cause the performance to be degraded by limiting the robustness and diameter of the pin to board connections. In order to minimize these risks, it is recommended that the PCB pin pads EPAD be designed using the following guidance. Non-solder mask defined pins are recommended and solder paste should be applied with stencil openings identically matched to the component pins as defined in the datasheet. Stencil thickness should be approximately 4 mils.

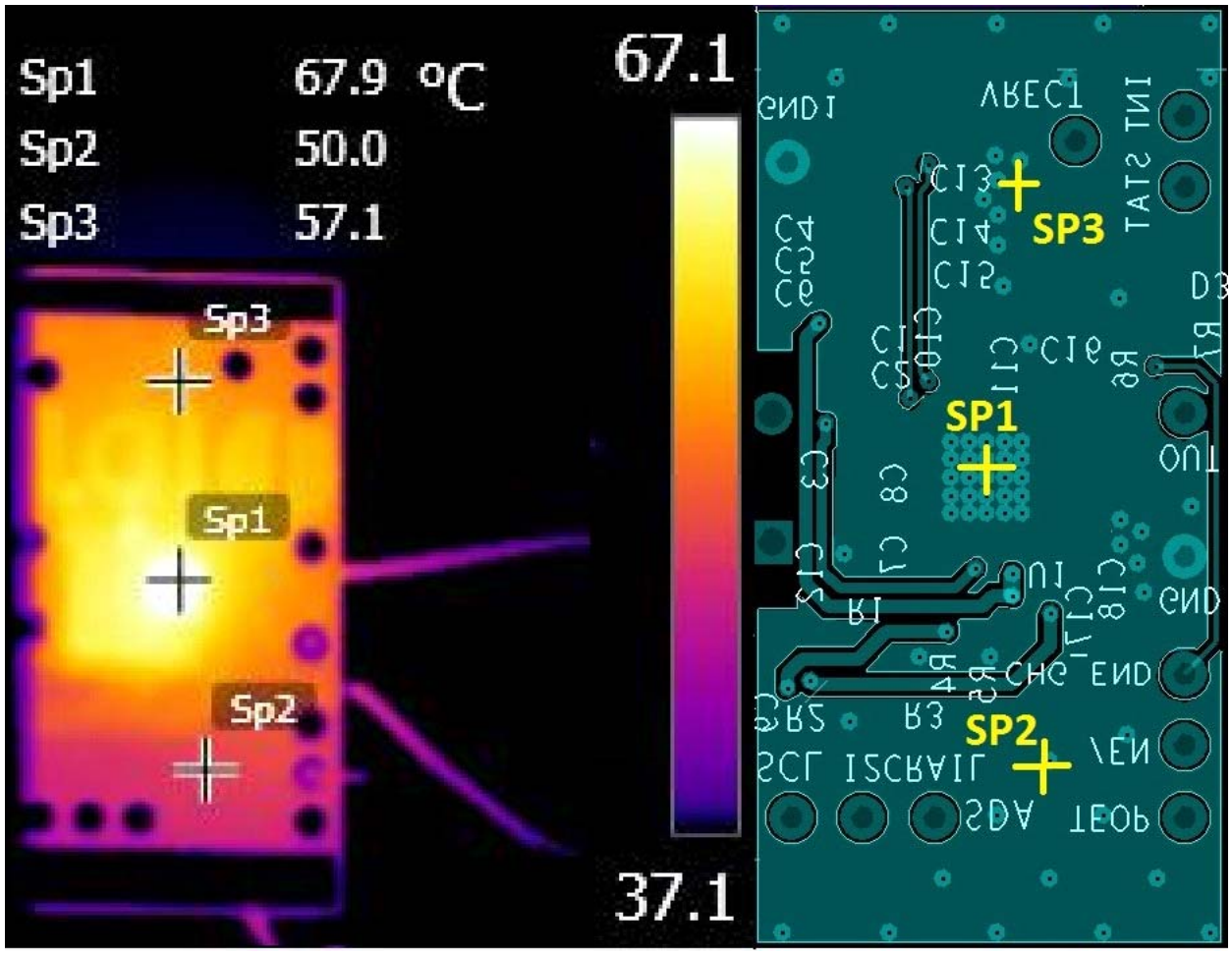
Figure 12. P9025AC QFN Footprint Design Guideline



Thermal Layout Overview

The heat management of the P9025AC design is critical to performance, and from the thermal perspective, it is recommended to route the main power connections as directly as possible to the device. This allows for optimal electrical and thermal performance. The main power connections are VRECT, AC1, AC2, OUT, the Rx coil node (LC node), and GND. These connections should be routed on the same side of the PCB as the P9025AC for maximum thermal benefit (excluding GND which should be on the closest internal layer and the outer layer opposite to the P9025AC). These traces should avoid multiple layer changes in order to reduce voltage drops and thermal resistance induced by thin via walls. If these traces need to transfer layers, it should be accomplished using multiple vias that have enough spacing such that they do not block the current path leading up to the via. The following thermal images (Figure 13, Figure 14, and Figure 15) show the heat flow on the back-side of the PCB.

Figure 13. P9025AC QFN Bottom Layer layout Temperatures (Ambient Temperature = 23.7°C)



Notice the temperature gradient is not even; SP3 is 57°C (direct connection to EPAD vias, only two traces obstructing heat and they are in straight lines). SP2 has necessary traces blocking the heat path and is only 50°C. To help reduce the temperature of the IC, heat must be given a path to follow for it to dissipate (such as wide copper planes).

Figure 14. P9025AC QFN Bottom Layer Heat Flow Paths

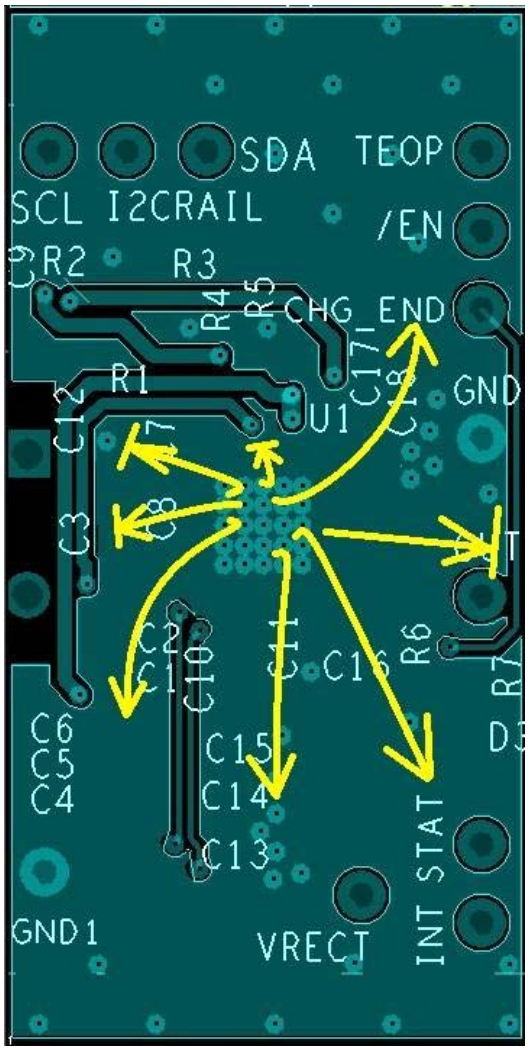
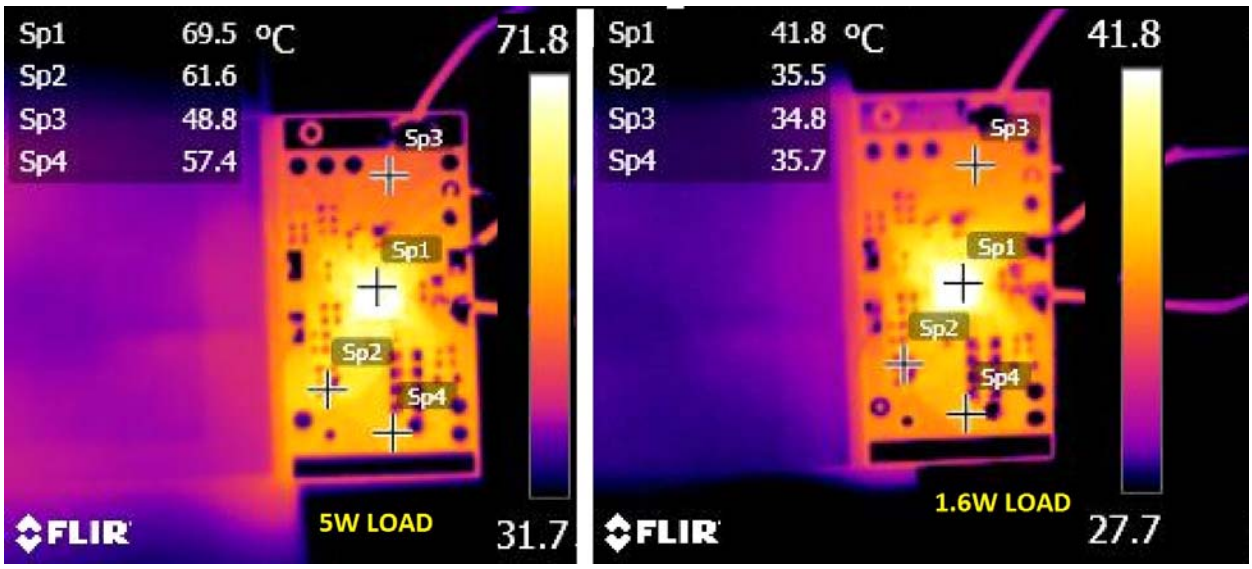


Figure 14 shows the thermal images of the P9025AC CSP DEMO PCB. Notice that the top of the package is measured to be 69.5°C (temperature rise of 46.8°C on 33 x 16.7 mm reference board design) when delivering 5 W in an ambient temperature of 23.7°C and 41.6°C when delivering 1.6 W.

Figure 15. P9025AC DEMO PCB Component Layer Thermal Image, 5W and 1.6W load (1.3" x 0.66")



The most effective way to transfer heat evenly across the PCB is to make the first layer beneath the component side of the board as solid of a GND plane as possible and to have large surfaces on the component side contacting the P9025AC. This reference board PCB is 1.6 mm thick, and the temperature on bottom is only 0.8°C higher than the package surface. This indicates that the heat developed on the component side of the PCB is transferred to the bottom of the board (or inner layers) effectively with the 25 thermal vias. Since effective thermal management is the sum of all heat flow paths, every opportunity for heat dissipation should be used.

Additionally, increasing the copper foil weight of the PCB allows the heat flow from the device to increase. Therefore, it is recommended to use 2-oz copper foil weight for small PCBs to improve thermal performance (600 mm^2 or smaller and heat sensitive designs). Thinner PCBs also dissipate more heat than thicker PCBs. Furthermore, the size of the PCB and the layer count will impact the operating temperature. To reduce the operating temperature, the PCB size should be increased and/or the layer count should be increased. Since every design is different and the continuity of the heat spreading surfaces cannot be predicted, a rule of thumb for temperature reduction based on additional area cannot be accurately provided. Assuming effective heat spreading techniques are implemented an average of 5 to 10°C per 40mm2 (per 0.25in^2) is fairly typical with an upper limit being approached when PCBs are approximately 100 x 100 mm (4" x 4") or larger.

Finally, in Figure 13, notice that the entire PCB is not the same temperature; an obvious heat gradient has developed. This demonstrates that the most effective heat transfer occurs when routing obstruction of the heat flow is minimized.

Audible Noise Suppression

Wireless power receiver solutions have been observed to produce audible noise. If sound is detected, there are several steps that can be taken to reduce or eliminate the noise. The first priority should be identifying the source (i.e. the rectifier capacitors, the Rx coil ferrite, ACM capacitors). Typically, the rectifier capacitors are the components that generate the audible noise.

The reason the noise is present and associated with the rectifier capacitors is due to the WPC and PMA communication signals being generated in the audible frequency range and the use of small form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors contract and expand while providing the communication pulses and this noise is amplified as it flexes the PCB.

The primary solution to this issue is to use low-acoustic noise capacitors. If that's not feasible, higher voltage rated components often have superior piezoelectric properties which can reduce the audible noise.

If swapping out the components is not possible, placing the capacitors on both sides of the PCB (directly above and below each other) can counter the piezoelectric forces applied to the PCB, thus eliminating the noise. Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. Lastly, some have reported success by placing additional lower-capacitance value components in parallel (such as eighteen 1uF capacitors instead of four 4.7uF capacitors) to reduce the mechanical force of the piezoelectric effect per component.

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