Introduction

Time-Slot Interchanger (TSI) products are used widely in Time Division Multiplexer (TDM) switching systems. Typical applications including the following:

- Central office TDM switches, i.e., Class 5 voice switches, Media Gateway, Wireless Services switches
- Digital cross-connects and digital loop carriers
- T1/E1 Add/drop multiplexers
- IP gateways
- PON transmission system
- Multi-service Access platforms
- Wireless base stations

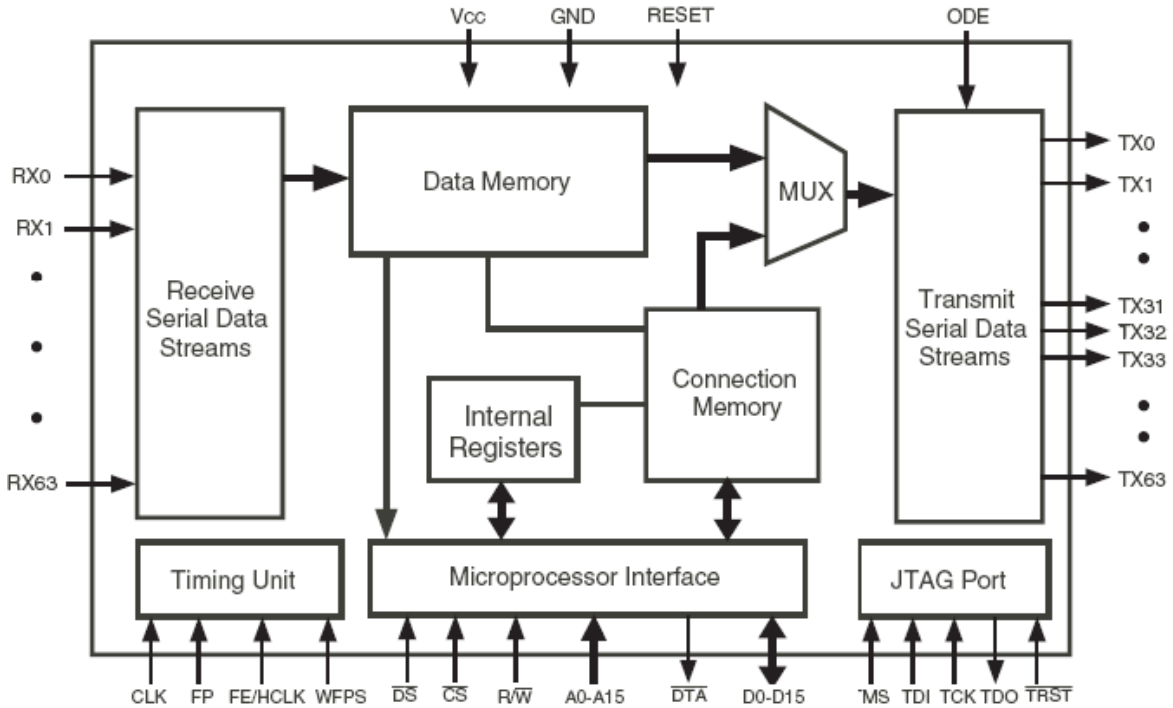
TSI conducts non-blocking switching down to DS0 level. IDT offers TSI products with a switching capacity ranging from 128 x 128 to 32K x 32K. Features also include input frame offset alignment, rate-matching and block programming, etc.

This application note describes in detail some of the basic application considerations for TSI products. These considerations include connection memory configuration, block programming and rate-matching features. These considerations are encountered in most TSI applications. TSI bus interface with H.110 will be discussed in a separate note.

Connection Memory Configurations

Figure 1 is a typical functional block diagram of TSI products. (also refer to References [1])

Figure 1. TSI Functional Block Diagram



There are two memory blocks shown in Figure 1 - Data Memory and Connection Memory. Data Memory is a temporary buffer of all incoming serial streams. It can be read out by processor to access a particular DS0 in any input serial stream. But its contents can not be altered by system processor.

Connection Memory can be read or written by the system processor. In processor mode (MOD[1:0] = 10), system processor can write data into Connection Memory locations to be routed into output serial streams. In other modes in which time-slot switching is enabled to connect any input time-slot to any output time-slot, Connection Memory must be configured accordingly. This is the basic function a TSI device accomplishes. This section introduces in detail how to configure Connection Memory for time-slot switching. An example is given to illustrate the configuration procedures.

Suppose you want to make a connection, using 72V71660, between Time Slot #1 (TS0) of input stream #5 (RX4) and Time Slot #10 of (TS9) of output stream #14 (TX13), and visa versa. That is, switching between (incoming) TS0/RX4 and (outgoing) TS9/TX13. We can also interpret this connection in terms of origin versus destination: Origin = TS0/RS4; Destination = TS9/TX13.

Making a time-slot switching in TSI device is then nothing more than defining the “destination” and the “origin”. Connection Memory block has a 16-bit address and a 16-bit data. The address bits define the Destination; the data bits determine the Origin.

Connection Memory block is selected when address bits A[15:14] = 10. The lower 14 address bits (A[13:0]) are used to select 214 = 16K locations in the block, of which A13~A8 select outgoing serial streams; A7~A0 select time slots in each of these streams. Please refer to Figure 2 for address bits definition. The address of each location in Connection Memory is the Destination. It represents an outgoing time-slot in TX streams

The 16-bit data intended to be written into a Connection Memory location is the origin. It specifies the data source (an incoming time-slot) for this destination (an outgoing time-slot). The data bits definition is shown in Figure 3.

Coming back to the above example, all we need to do is to define the destination in Connection Memory and to determine the origin (data source) for it. We have:

(1) The destination can be translated into an address: TS9/TX13 ⟶ A[15:14] = 10, STA[5:0] = 001101, CH[7:0] = 00001001. The address is: 0x8D09 in hex.

Figure 2. Connection Memory Address Definition

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	Location
1	0	STA5	STA4	STA3	STA2	STA1	STA0	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	R/W	Connection Memory

(2) The origin can be obtained by: TS0/RX4 ⟶ MOD[1:0] = 01 (for constant delay mode), AB[5:0] = 000100, CAB[7:0] = 00000000. Therefore, the origin is: 0x4400

A single write operation on Connection Memory with address = 0x8D09 and data = 0x4400 will make a connection specified in the example

Figure 3. Contents (source) Definition For Connection Memory Locations

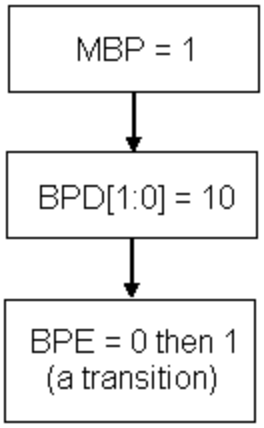
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD1	MOD0	SAB5	SAB4	SAB3	SAB2	SAB1	SAB0	CAB7	CAB6	CAB5	CAB4	CAB3	CAB2	CAB1	CAB0

Bit	Name	Description
15, 14	MOD1-0 (Switching Mode Selection)	MOD1 MOD0 MODE 0 0 Variable Delay mode 0 1 Constant Delay mode 1 0 Processor mode 1 1 Output high-impedance
13-8	SAB5-0 (Source Stream Address Bits)	The binary value is the number of the data stream for the source of the connection.
7-0	CAB7-0 (Source Channel Address Bits)	The binary value is the number of the channel for the source of the connection.

Memory Block Programming

Memory block programming capability is provided to ease the initialization of the entire Connection Memory block. The feature involves 4 control bits in Control register (A[15:14] = 01): MBP (bit 9), BPD[1:0] (bit 8 and 7), BPE (bit 6). The following is a working procedure for activating Memory Block Programming:

Figure 4. Steps to enable Memory Block Programming



Once a zero-to-one transition is created on BPE bit, the entire Connection Memory block will be initialized in 2 frames (2x125µs = 250µs). The initialization process put A[15:14] = BPD[1:0], A[13:0] = 0x0000 in every single locations in Connection Memory block. By completion, the device will reset BPD[1:0] = 00.

To disable the Memory Block Program feature, configure MBP = 0. In this case, the system processor needs to conduct the initialization process by writing into every location of the Connection Memory block.

Rate-Matching

Rate-matching allows the user to configure TSI device in such a way that all input streams operate in the same rate while output streams operate in different rates. This feature apparently enhances the flexibility of device's TDM interfaces.

TSI devices supporting rate-matching (refer to References [2]) can be configured to work in either “regular mode” (input and output streams operate in the same rate) or “Mux/Deux mode” in which rate-matching is possible.

Four control bits (DR[3:0]) in Control Register configure different rate combinations, as shown in the following chart (also refer to References [3]).

Figure 5. Rate-matching Selections by Control Bits DR[3:0]

Switching Mode	Control Bits				Data Rate bits/s		Clock Rate MHz
	DR3	DR2	DR1	DR0	Receive Streams	Transmit Streams	
Mux/Demux	0	1	0	0	2 M on RX0-15	8 M on TX0-3	16
	0	1	0	1	8 M on RX0-3	2 M on TX0-15	16
	0	1	1	0	4 M on RX0-15	8 M on TX0-7	16
	0	1	1	1	8 M on RX0-7	4 M on TX0-15	16
	1	0	0	0	16 M on RX0-1	2 M on TX0-15	16
	1	0	0	1	2 M on RX0-15	16 M on TX0-3	16
	1	0	1	0	16 M on RX0-7	8 M on TX0-15	16
	1	0	1	1	8 M on RX0-15	16 M on TX0-7	16

Note: 16.384MHz clock rate is required when rate-matching is enabled.

References

[1] 72V71660 device datasheet

[2] Rate-matching is supported in the following IDT TSI devices: 72V71623 (2K x 2K), 72V71643 (4K x 4K), 72V73263 (16K x 16K), 72V73273 (32K x 32K)

[3] 72V71643 device datasheet

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