

Introduction

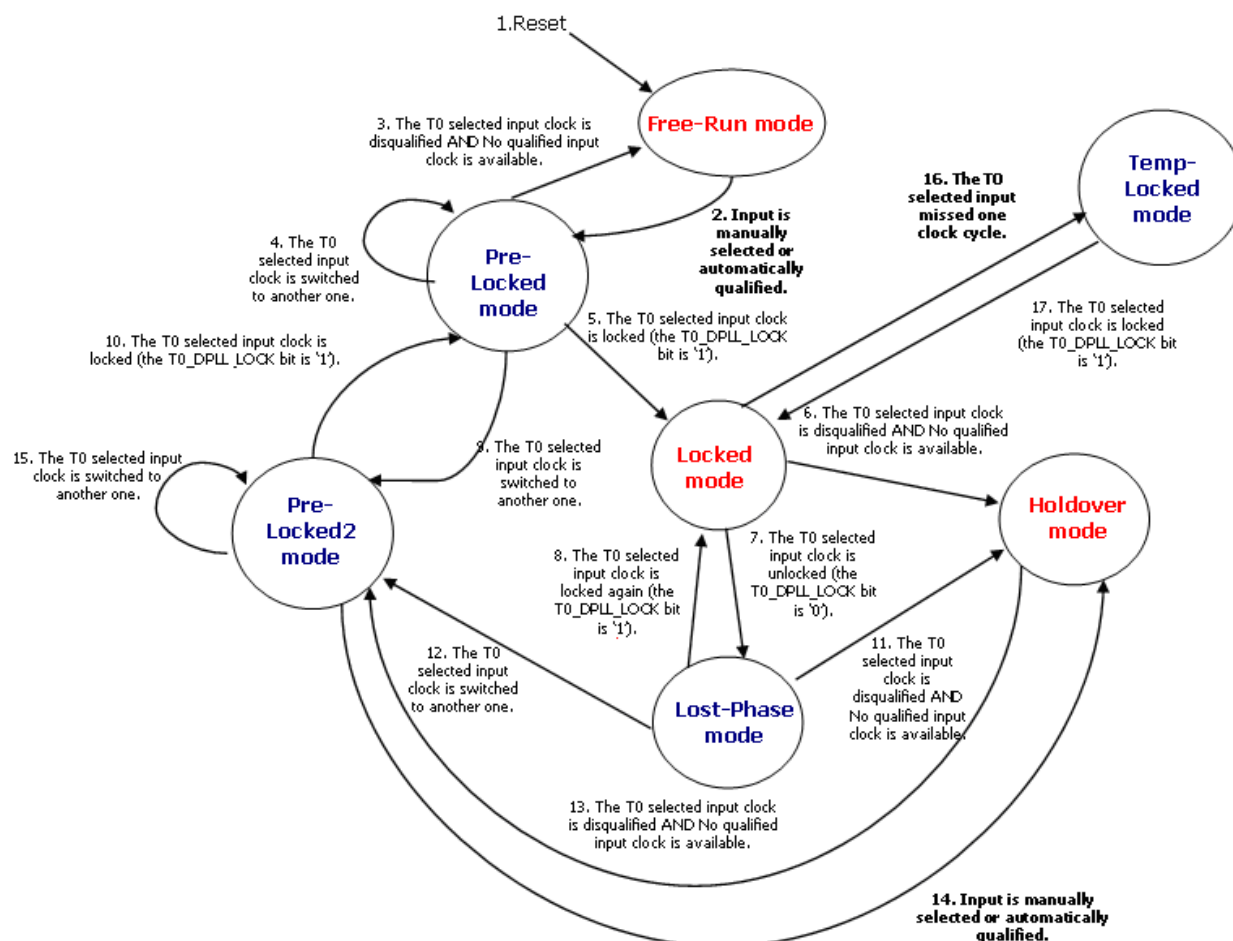
The core functionality of the 82V3255 T0 DPLL consists of two state machines; an input clock qualification machine to assess the suitability of the input signals on all input clock ports to serve as references to the second state machine, the core DPLL that generates the DPLL output clocks. This application note provides the state transition details of the core DPLL state machine, depicted in Figure 1.

Operating States of the T0 DPLL

The T0 DPLL supports three primary operating states (modes) shown in red: Free-Run, Locked and Holdover. Also shown are the four secondary, temporary operating states (modes): Temp-Locked, Pre-Locked, Pre-Locked2 and Lost-Phase. Transitions between these states are caused by changes in either the:

1. Input reference selection made either automatically by the input clock state machine or manually by the user (no clocks available, clocks switched, disqualified or newly qualified).
2. Instantaneous phase of the input reference.
3. Phase relationship between the selected input reference and the DPLL output clock.
4. Output clock frequency ppm error.

Figure 1. 82V3255 Transition Diagram



T0/T4 DPLL Locking Detection Monitors

The changes listed in items 2–4 above are implemented by the following features within the DPLL state machine. Each of these monitors will trigger a loss of lock when an event or monitor threshold is crossed and raise an alarm. DPLL Soft Limit does not trigger loss of lock as noted.

Table 1: DPLL Lock Quality Monitors

| Monitor | DPLL Monitoring Point | Trigger Event | Enable Name (Set bit =1 to enable) |
|-------------------|-----------------------|---|--|
| Fast Loss | Input Reference | Set - Selected input clock misses 2 consecutive clock cycles. Clear - A clock edge occurs. | FAST_LOS_SW |
| Coarse Phase Loss | DPLL phase detector | Set - Phase Detector Error greater than the Coarse Phase Loss Limit. Clear - Phase Detector Error less than the Coarse Phase Loss Limit. | COARSE_PH_LOS_LIMT_EN |
| Fine Phase Loss | DPLL phase detector | Set - Phase Detector Error greater than the Fine Phase Loss Limit. Clear - Phase Detector Error less than the Fine Phase Loss Limit. | FINE_PH_LOS_LIMT_EN |
| DPLL Hard Limit | DPLL output frequency | Set - DPLL ppm greater than the DPLL Hard Limit (ppm) Clear - DPLL ppm less than the DPLL Hard Limit (ppm) | FREQ_LIMT_PH_LOS |
| DPLL Soft Limit | DPLL output frequency | Set - DPLL ppm greater than the DPLL Soft Limit (ppm) Clear - DPLL ppm less than the DPLL Soft Limit (ppm) | NA. Will not trigger Loss of Lock. Only raises T0_DPLL_SOFT_FREQ_ALARM |

Setting the Coarse Phase Loss Limit

The Coarse Phase Loss Limit is dependent on input clock frequency, MULTI_PH_8K_4K_2K_EN bit, WIDE_EN bit and PH_LOS_COARSE_LIMT[3:0]. The options available to set the Coarse Phase Loss Limit are broken down by input clock reference frequency in the following two tables.

Table 2: Input Clock is 2kHz, 4kHz or 8kHz

| MULTI_PH_8K_4K_2K_EN | WIDE_EN | Coarse Phase Limit |
|----------------------|-------------|---|
| 0 | Do not care | ±1 UI |
| 1 | 0 | ±1 UI |
| | 1 | Set by the PH_LOS_COARSE_LIMT[3:0] bits |

Table 3: Input Clock Frequency is other than 2kHz, 4kHz or 8kHz

| WIDE_EN | Coarse Phase Limit |
|---------|---|
| 0 | ±1 UI |
| 1 | Set by the PH_LOS_COARSE_LIMT[3:0] bits |

Setting the Fine Phase Loss Limit

The fine phase limit programmed is by the PH_LOS_FINE_LIMT[2:0] bits in accordance with the following table.

Table 4: Fine Phase Loss Limits

| | |
|-----------------------|--|
| PH_LOS_FINE_LIMT[2:0] | 001: $\pm (45^\circ \sim 90^\circ)$ 010: $\pm (90^\circ \sim 180^\circ)$. (default) 011: $\pm (180^\circ \sim 360^\circ)$ 100: $\pm (20 \text{ ns} \sim 25 \text{ ns})$ 101: $\pm (60 \text{ ns} \sim 65 \text{ ns})$ 110: $\pm (120 \text{ ns} \sim 125 \text{ ns})$ 111: $\pm (950 \text{ ns} \sim 955 \text{ ns})$ |
|-----------------------|--|

Setting DPLL ppm Limits (Hard Limit Exceeding)

The DPLL soft limit is set by the DPLL_FREQ_SOFT_LIMT[6:0] bits. It is calculated as follows:

$$\text{DPLL Soft Limit (ppm)} = \text{DPLL_FREQ_SOFT_LIMT}[6:0] \times 0.724$$

The DPLL hard limit is set by the DPLL_FREQ_HARD_LIMT[15:0] bits. It is calculated as follows:

$$\text{DPLL Hard Limit (ppm)} = \text{DPLL_FREQ_HARD_LIMT}[15:0] \times 0.0014$$

Transient events can occur causing threshold crossing in these monitors but are not observable after the associated alarm has been raised. It is expected that transient conditions that affect the lock status will be caused primarily by the input reference since the DPLL output clock is generated by the OSCI oscillator and bandwidth limited by the DPLL. The input reference however is subject to transmission and customer clock conditioning prior to presentation to the DPLL.

It is recommended that all status information be latched and time stamped when any status changes occurs in the DPLL to assist tracing clock faults through a network.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.