SerDes Configuration for Industrial Temperature (-40°C to 85°C)

Application Note: 825

89Hxx[H|T]xxG2 Family of PCI Express Switches

Introduction

The IDT 89Hxx[H|T]xxG2 family of PCI Express switches offers a unique set of advanced features including switch partitioning. Most applications that leverage the advanced features of this family operate in harsh environmental conditions. These embedded designs using the 89Hxx[[H|T]xxG2 have experienced more sensitivity with respect to SerDes calibration across a wide temperature range than that which can be supported by the default device settings.

The document provides system designers with the necessary information to modify the SerDes calibration parameters to operate across the entire industrial temperature range, -40ºC to 85ºC.

Symptom

The majority of designs will not experience this issue until wide temperature cycle testing is performed. The issue is not observed during normal operation in a lab environment. The sensitivity affecting the SerDes calibration is seen when the device powers up at one of the extreme ends of the supported temperature range specification (for example, -40ºC) and is then rapidly forced to the opposite end of the temperature range. As a result, the Clock and Data Recovery (CDR) circuit may occasionally lose lock at or along the way to the temperature at the opposite extreme, thereby causing loss of a PCIe link.

Solution

The solution is to increase the SerDes calibration margin in order to improve the ability of the CDR to track with wider temperature swings. The tuning can be done using a 3-bit field called INT_STEP inside a SerDes register. This field needs to be changed for each lane of the device.

INT_STEP

The SerDes register to be modified has the default value of 0x0000_006B. The least significant bits, in binary, are: 01101011. The last three underlined bits are the INT_STEP value. The default value of INT_STEP, as can be seen above, is 3 (011b). This value can be changed in the range of 000b to 111b. Setting this value below the default (3) will generally not improve device behavior. Therefore users are encouraged to try the following values.

INT_STEP	Register Value
011b	0x0000_006B (default)
100b	0x0000_006C
101b	0x0000_006D
110b	0x0000_006E

These values can be changed via EEPROM (preferred) or via PCIe in-band accesses or SMBUS accesses.

EEPROM Solution Example

This example is for the 89H32H8G2 – it can be easily modified for any member of the 89Hxx[H|T]xxG2 PCIe switches.

The following EEPROM code modifies the SerDes register that contains the INT_STEP field for Quads 4 and 5. Please ensure that all of the ports being used in the design are modified similarly by replicating the lines of code. This EEPROM code should be added to the very top of the EEPROM so that it takes effect immediately before the SerDes start calibrating upon power on.

The following example changes the default value of INT_STEP to 5 (register value: 0x6D). This should work for most applications. Additional values can be experimented with to determine the optimal setting. The value of INT_STEP = 7 (Register: 0x0000_006F) is not recommended as it appears to reduce the Receiver jitter tolerance.

The registers used in the following code example are explained in Register Definitions.

EEPROM Code

0x0003EA08 0x0000006D; increase ***INT_STEP*** to 5 (default = 3)
0x0003EA00 0x00000004; select SerDes Quad4
0x0003EA04 0x80000103; set OPTYPE to write to address 0x0103 (lane0)
0x0003EA04 0x80000203; set OPTYPE to write to address 0x0203 (lane0)
0x0003EA04 0x80000303; set OPTYPE to write to address 0x0303 (lane0)
0x0003EA04 0x80000403; set OPTYPE to write to address 0x0403 (lane0)
0x0003EA00 0x00000005; select SerDes Quad5
0x0003EA04 0x80000103; set OPTYPE to write to address 0x0103 (lane0)
0x0003EA04 0x80000203; set OPTYPE to write to address 0x0203 (lane0)
0x0003EA04 0x80000303; set OPTYPE to write to address 0x0303 (lane0)
0x0003EA04 0x80000403; set OPTYPE to write to address 0x0403 (lane0)

<…Repeat above pattern to update all SerDes quads…>

PCIe In-band and SMBus Slave Example

This example is for the 89H32H8G2 – it can be easily modified for any member of the 89Hxx[H|T]xxG2 PCIe switches.

There is no Switch Configuration EEPROM available in this usage scenario, so the registers are updated by the local CPU on the board through either the in-band PCI Express link or the SMBus slave interface. The following EEPROM code modifies the SerDes register that contains the INT_STEP field for Quads 2 and 3. Please ensure that all of the ports being used in the design are modified similarly by replicating the lines of code. After the INT_STEP filed has been updated within a port, that port is required to run through a full link retrain. The full link retrain is done by setting the FLRET bit in the PHYLSTATE0 register (for more information about this register, see the relevant 89Hxx[H|T]xxG2 User Manual).

The following example changes the default value of INT_STEP to 5 (register value: 0x6D). This should work for most applications. Additional values can be experimented with to determine the optimal setting. The value of INT_STEP = 7 (Register: 0x0000_006F) is not recommended as it appears to reduce the Receiver jitter tolerance.

The registers used in the following code example are explained in Register Definitions.

The pseudo operation pciwrite is used to indicate some piece of software that writes to the IDT device registers, either in-band or through the SMBUS. IDT can provide such software to users that need it. The operation is simply “pciwrite <config space offset> <value to be written at the offset>.

CPU Code

pciwrite 0x0003EA08 0x0000006D; increase ***INT_STEP*** to 5 (default = 3)
pciwrite 0x0003EA00 0x00000002; select SerDes Quad2
pciwrite 0x0003EA04 0x80000103; set OPTYPE to write to address 0x0103 (lane0)
pciwrite 0x0003EA04 0x80000203; set OPTYPE to write to address 0x0203 (lane1)
pciwrite 0x0003EA04 0x80000303; set OPTYPE to write to address 0x0303 (lane2)
pciwrite 0x0003EA04 0x80000403; set OPTYPE to write to address 0x0403 (lane3)
pciwrite 0x00004540 0x80000000; set FLRET to initiate full link retrain Quad2
pciwrite 0x0003EA00 0x00000003; select Serdes Quad3
pciwrite 0x0003EA04 0x80000103; set OPTYPE to write to address 0x0103 (lane0)
pciwrite 0x0003EA04 0x80000203; set OPTYPE to write to address 0x0203 (lane1)
pciwrite 0x0003EA04 0x80000303; set OPTYPE to write to address 0x0303 (lane2)

pciwrite 0x0003EA04 0x80000403; set OPTYPE to write to address 0x0403 (lane3)

pciwrite 0x00006540 0x80000000; set FLRET to initiate full link retrain Quad3

<…Repeat pattern above to update all SerDes quads…>

Register Definitions

Table 1: Register List

Cfg. Offset	Size	Register Mnemonic	Register
0xA00	DWord	SDGC	SerDes Debug Global Control
0xA04	DWord	SIRCTL	SerDes Internal Register Control
0xA08	DWord	SIDATA	SerDes Internal Register Data

The SerDes Debug Global Control (SDGC - SerDes Debug Global Control) register (Table 2) determines the SerDes Quad that will be affected by the settings in the SIRCTL and SIDATA registers (Table 3 and Table 4).

Table 2: SerDes Debug Global Control (SDGC)

Bit Field	Field Name	Type	Default Value	Description
4:0	SS	RW	0x0 SWSticky	Select. This field is used to select the block (that is, on-chip PLL or SerDes) within the 89Hxx[H|T]xxG2 on which the SIRCTL and SDTBCS registers operate. 0x0 - SerDes Quad 0 0x1 - SerDes Quad 1 0x2 - SerDes Quad 2 0x3 - SerDes Quad 3 0x4 - SerDes Quad 4 0x5 - SerDes Quad 5 0x6 - SerDes Quad 6 0x7 - SerDes Quad 7 0x8 - SerDes Quad 8 0x9 - SerDes Quad 9 0xA - SerDes Quad 10 (Not available in 89H32[H|T]8G2 and 89H48[H|T]12G2) 0xB - SerDes Quad 11 (Not available in 89H32[H|T]8G2 and 89H48[H|T]12G2) 0xC - SerDes Quad 12 (Not available in 89H32[H|T]8G2) 0xD - SerDes Quad 13 (Not available in 89H32[H|T]8G2) 0xE - SerDes Quad 14 (Not available in 89H32[H|T]8G2 and 89H48[H|T]12G2) 0xF - SerDes Quad 15 (Not available in 89H32[H|T]8G2 and 89H48[H|T]12G2) 0x1F - On-chip PLL Others - Reserved Selecting an invalid value produces undefined results.
31:5	Reserved	RO	0x0	Reserved.

SerDes Internal Register Control (SIRCTL) and SerDes Internal Register Data (SIDATA) provide access to the SerDes internal control and status registers. That is, the SIRCTL and SIDATA registers provide a mechanism of indirection by which all internal registers in the selected block can be accessed.

When writing data to an internal register (i.e., the Operation Type (OPTYPE) field in SIRCTL is set to "Write"), the data to be written is the current value of the corresponding SIDATA register. Note that the SIDATA register must be written prior to initiating a write access via the SIRCTL register. The OPDONE bit in the SIDATA register is set once the requested operation completes.

Table 3: SerDes Internal Register Control (SIRCTL)

Bit Field	Field Name	Type	Default Value	Description
15:0	ADDR	RW	0x0 SWSticky	Address For the block selected via the SS field in the SDGC register (that is, SerDes or on-chip PLL), this field is used to select the address of the internal block register to be accessed.
30:16	Reserved	RO	0x0	Reserved
31	OPTYPE	RW	0x0 SWSticky	Operation Type This field selects whether to read or write the internal register selected by the ADDR field in this register. 0x0 - Read 0x1 - Write The corresponding action is initiated whenever any field in this register is written to. The read or write operation is guaranteed to complete within 10 microseconds.

Table 4: SerDes Internal Register Data (SIDATA)

Bit Field	Field Name	Type	Default Value	Description
7:0	DATA	RW	0x0 SWSticky	Data. When the OPTYPE field in the SIRCTL register is set to "read", this field contains the data read from the selected internal register. When the OPTYPE field in the SIRCTL register is set to "write", this field contains the data to be written into the selected internal register. For read operations, the value of this field is valid only when the OPDONE field in this register is set. For write operations, this field must be written prior to initiating an internal register access by writing to the SIRCTL register.
30:8	Reserved	RO	0x0	Reserved
31	OPDONE	RO	0x0 SWSticky	Operation Done. This status bit indicates if the operation selected by the OPTYPE field in the SIRCTL has completed. This bit is automatically cleared by hardware whenever the SIRCTL register is written to.

Conclusion

The IDT 89Hxx[H|T]xxG2 PCIe switches operate across the entire industrial temperature range, -40°C to 85°C. If the default CDR circuit settings are not optimal, the device can improve its CDR tracking margin using the examples outlined in this document. The 89Hxx[H|T]xxG2 switches are the most advanced PCI Express switches and are ideal for embedded applications.

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