## Introduction

High performance clock buffers are widely used in digital consumer and communications applications for distribution of clock signals. A critical parameter for these buffers is additive phase noise that can degrade system performance and reliability. This application note briefly explains the theory behind measuring additive phase noise for IDT clock buffers and summarizes the additive phase jitter results for several widely used IDT clock buffers. Other AC parameters of interest for buffers are input to output propagation delay and output to output skew.

In synchronous systems where timing and performance of the system is dependent on the clock, integrity of the clock signal is important. Designers must optimize board layout, use clean power supplies and follow recommended decoupling and termination schemes for the outputs in order to meet the EMI and timing budgets for their application.

IDT has a large variety of low skew clock distribution devices to meet all your application needs. Figure 1 shows a typical set top box application where an IDT clock buffer is used to distribute 33MHz PCI clocks to multiple PCI slots.
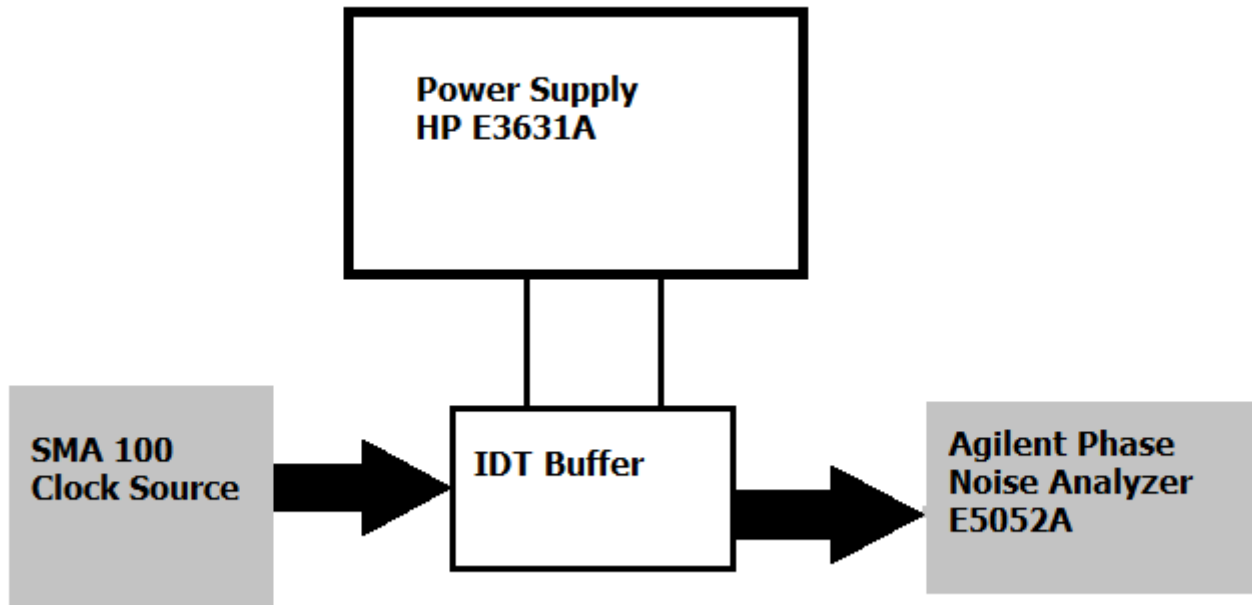
Figure 1. Set Top Box Application Diagram Using an IDT Clock Buffer
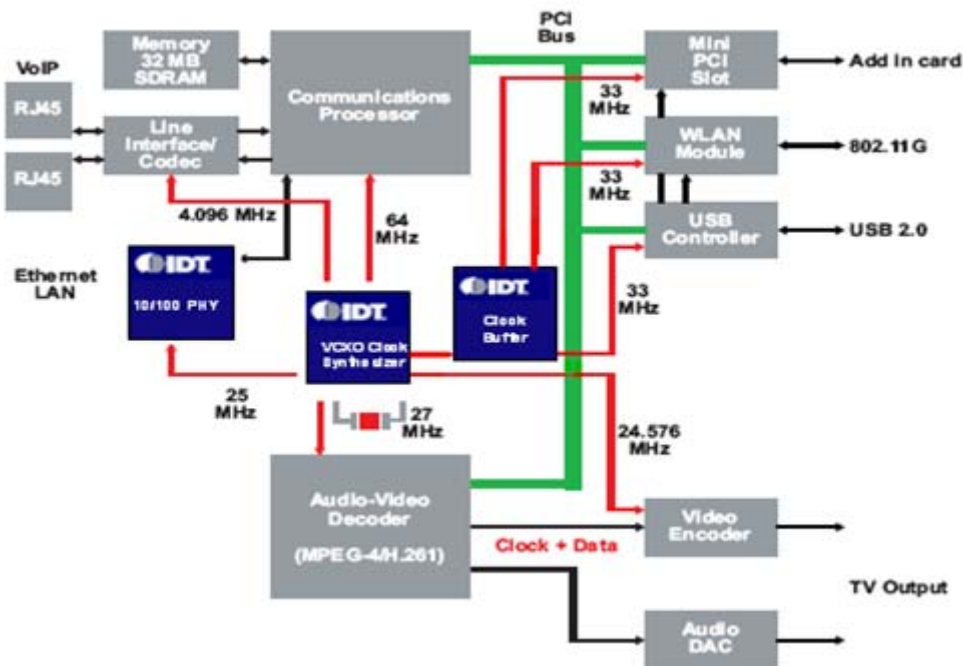
Phase Noise Measurement

The Agilent 5052A Phase Noise analyzer is used to take phase noise plots and the RMS jitter is calculated over an offset range for a center carrier frequency.

Figure 2. Test Setup for Additive Jitter Measurements

Additive Phase Noise

Any component in a signal chain has some amount of noise at its output that is generated internally (not including the contribution due to the external reference noise at the input). It is useful to measure the phase noise at the output of a device in such a way that the phase noise of any external source is canceled out. The phase noise so measured is specified as the additive phase noise of the device. It is the amount of phase noise that the device (clock buffer in our case) adds to the signal chain. IDT clock buffers have ultra low additive phase jitter thereby allowing system designers to distribute multiple copies of a clean clock to other devices on their system. The clock signal integrity is maintained thereby eliminating the need for additional jitter cleaning components. By considering the phase noise contribution due to the buffer alone, it is then possible to foretell the degree to which the buffer impacts the total system phase noise when used in conjunction with components such as oscillators and clock sources, each of which contribute to the phase noise of the total system. In many cases, the phase noise of one element in the chain dominates the system phase noise.

Additive Jitter

Additive jitter is defined as the added amount of jitter to the input signal caused by the device itself and can be calculated as:

**Total Additive Jitter = sq root ((output clock jitter)^2 - (input clock rms jitter)^2)**

It assumes that the noise processes are random and the input noise is not correlated to the output noise. Additive jitter must be measured with a clock source where phase noise is below the noise floor of the buffer itself.

The input clock reference source used for phase jitter measurements is a SMA100A clock generator which is very low phase noise. The measured phase noise of the input clock to the IDT buffers used varies over frequencies. Below are phase noise measurements of frequency equal to 25MHz. The RMS jitter is measurement over the offset range of 12kHz to 20MHz. The average phase noise RMS Jitter measured on the SMA clock source is 80fs. We will use this value for our calculations of additive jitter in this applications note. This value represents the input clock RMS Jitter for the below formula.

Additive Phase Noise Results

Measurements for Additive Phase Noise were taken on five of the most commonly used IDT Clock Buffers at three frequencies: 25MHz, 100MHz and 125MHz. All measurements contained in this report were taken at room temperature and at the nominal voltage.

Figure 3. Phase Noise on ICS553 25MHz Clock Output and 25MHz Input Clock Source
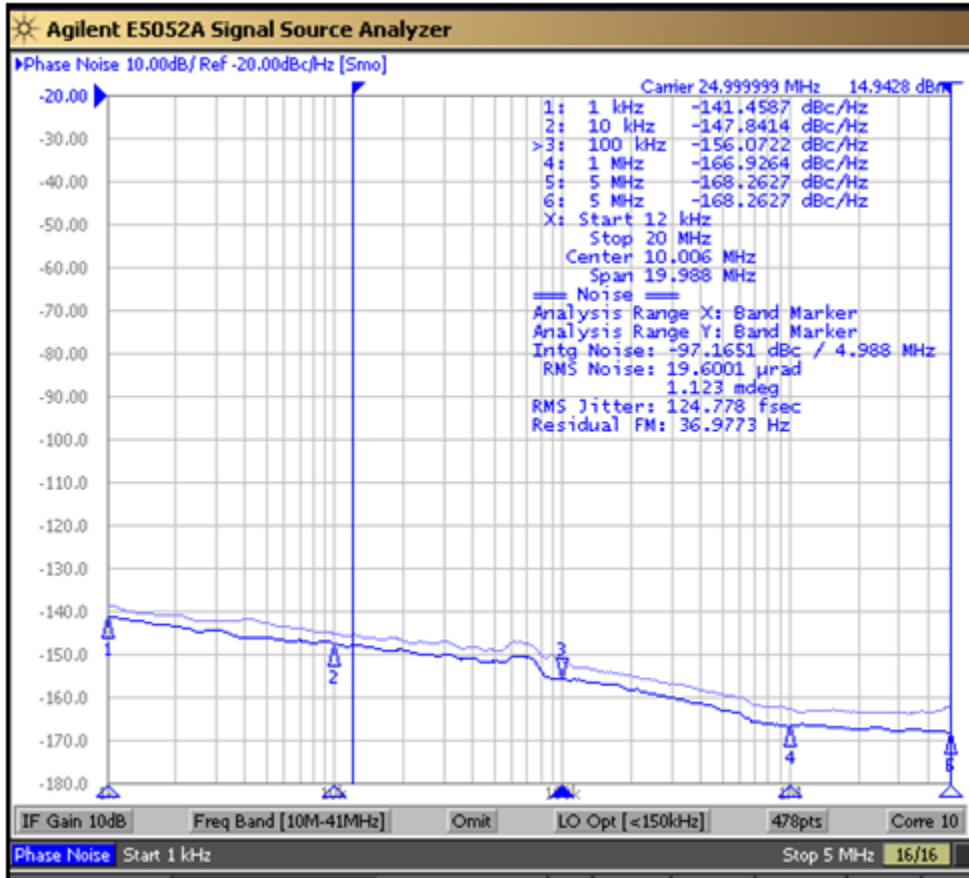
Summary of Additive Jitter Results

The additive phase noise measurement results presented in this application note confirm ultra low additive phase jitter across IDT's family of clock buffers. The additive phase jitter varies minimally over the buffer input frequency range and operating voltage range. All measurement data is in femto seconds (fs).

Table 1. Summary of Additive Jitter on Commonly Used IDT Clock Buffers

MHz	Range	IDT2305NZ	ICS551	ICS553	IDT74FCT3807	IDT5T30533
25	12kHz–20MHz	120.11	101.07	89.87	312.50	404.54
100	12kHz–20MHz	53.23	76.51	48.37	82.53	52.84
125	12kHz–20MHz	69.23	87.11	55.38	267.24	176.09

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