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April 1st, 2010
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RENESAS

Application Note

78K0S/Kx1+

8-Bit Single-Chip Microcontrollers

Flash Memory Programming (Programmer)

μPD78F9200
μPD78F9201
μPD78F9202
μPD78F9210
μPD78F9211
μPD78F9212
μPD78F9221
μPD78F9222
μPD78F9232
μPD78F9234

Document No. U17470EJ4V0AN00 (4th edition)
Date Published September 2006 NS CP(K)

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

[MEMO]

INTRODUCTION

Target Readers

This application note is intended for users who understand the functions of the 78K0S/Kx1+ and who will use this product to design application systems.

Purpose

The purpose of this application note is to help users understand how to develop dedicated flash memory programmers for rewriting the internal flash memory of the 78K0S/Kx1+.

Organization

This manual consists of the following main sections.

- OVERVIEW
- COMMUNICATION PROTOCOL
- SETTING FLASH MEMORY PROGRAMMING MODE
- COMMAND SPECIFICATIONS
- FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers. The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

☐ To learn more about the 78K0S/Kx1+'s hardware functions:

→ See the user's manual of each 78K0S/Kx1+ product.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeral representation:	Binary ..... xxxx or xxxxB
	Decimal xxxx
	Hexadecimal ..... xxxxH

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Device-related documents

Document Name	Document Number
78K0S/KU1+ User's Manual	U18172E
78K0S/KY1+ User's Manual	U16994E
78K0S/KA1+ User's Manual	U16898E
78K0S/KB1+ User's Manual	U17446E
78K/0S Series Instructions User's Manual	U11047E

CONTENTS

CHAPTER 1 OVERVIEW

To rewrite the contents of the internal flash memory of the 78K0S/Kx1+, a dedicated flash memory programmer (hereafter referred to as the “programmer”) is usually used.

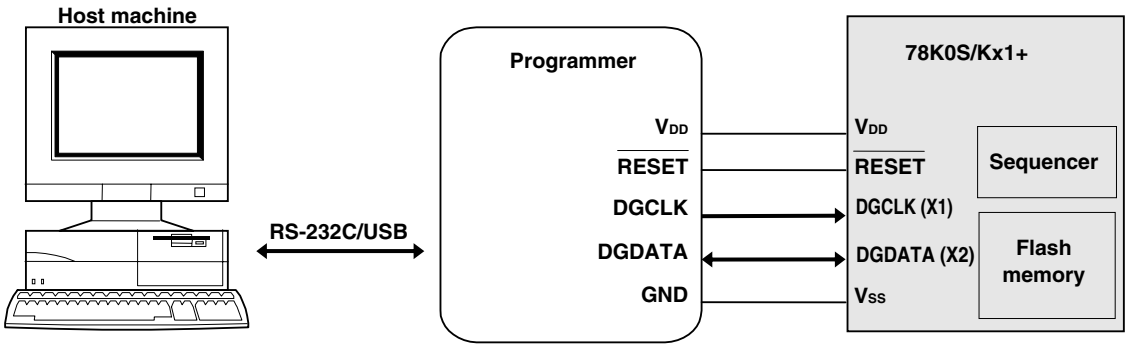
This Application Note explains how to develop a dedicated programmer.

1.1 System Configuration

An example of the system configuration for programming the flash memory is illustrated in Figure 1-1.

This figure illustrates how to program the flash memory under control of a host machine.

Figure 1-1. Programming Environment



Caution Supply V_{DD} starting from 0 V to correctly initialize the device hardware before setting the flash memory programming mode.

Remark The interface communicating commands/data between the programmer and 78K0S/Kx1+ is a single-wired UART using the DGDATA pin.

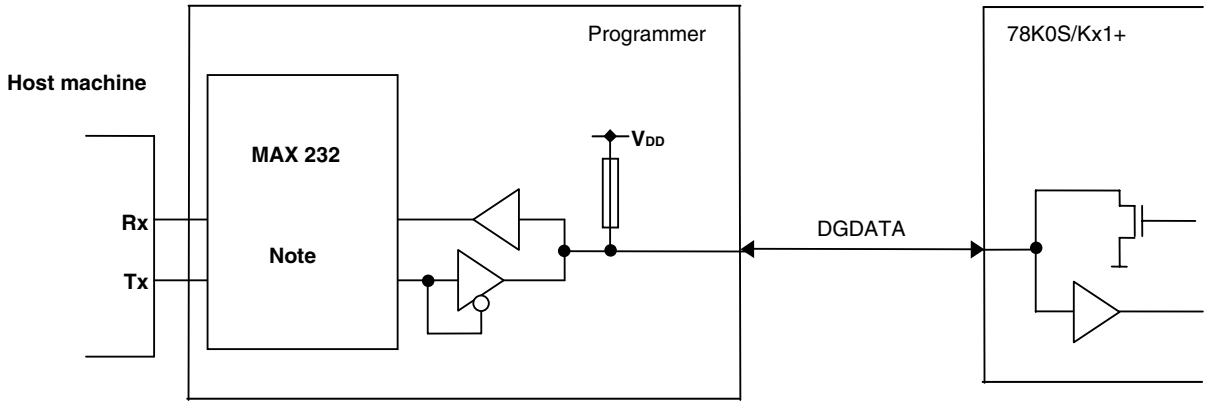
Depending on how the programmer is connected, the programmer can be used in a standalone mode without using the host machine, if a user program has been downloaded to the programmer in advance.

For example, NEC Electronics’ flash memory programmer PG-FP4 can be executed by GUI software with a host machine connected, or in the standalone mode.

As described, communication between the programmer and 78K0S/Kx1+ is established by a single-wire UART.

Figure 1-2 shows an example of the driver configuration if the host machine and programmer are connected with RS-232C.

Figure 1-2. Driver Configuration Example



Note All connections are not shown.

1.2 Information Specific to 78K0S/Kx1+

The 78K0S/Kx1 does not have a “signature” for product identification.

It is therefore necessary for the programmer to manage product-specific information (such as a device name and memory information).

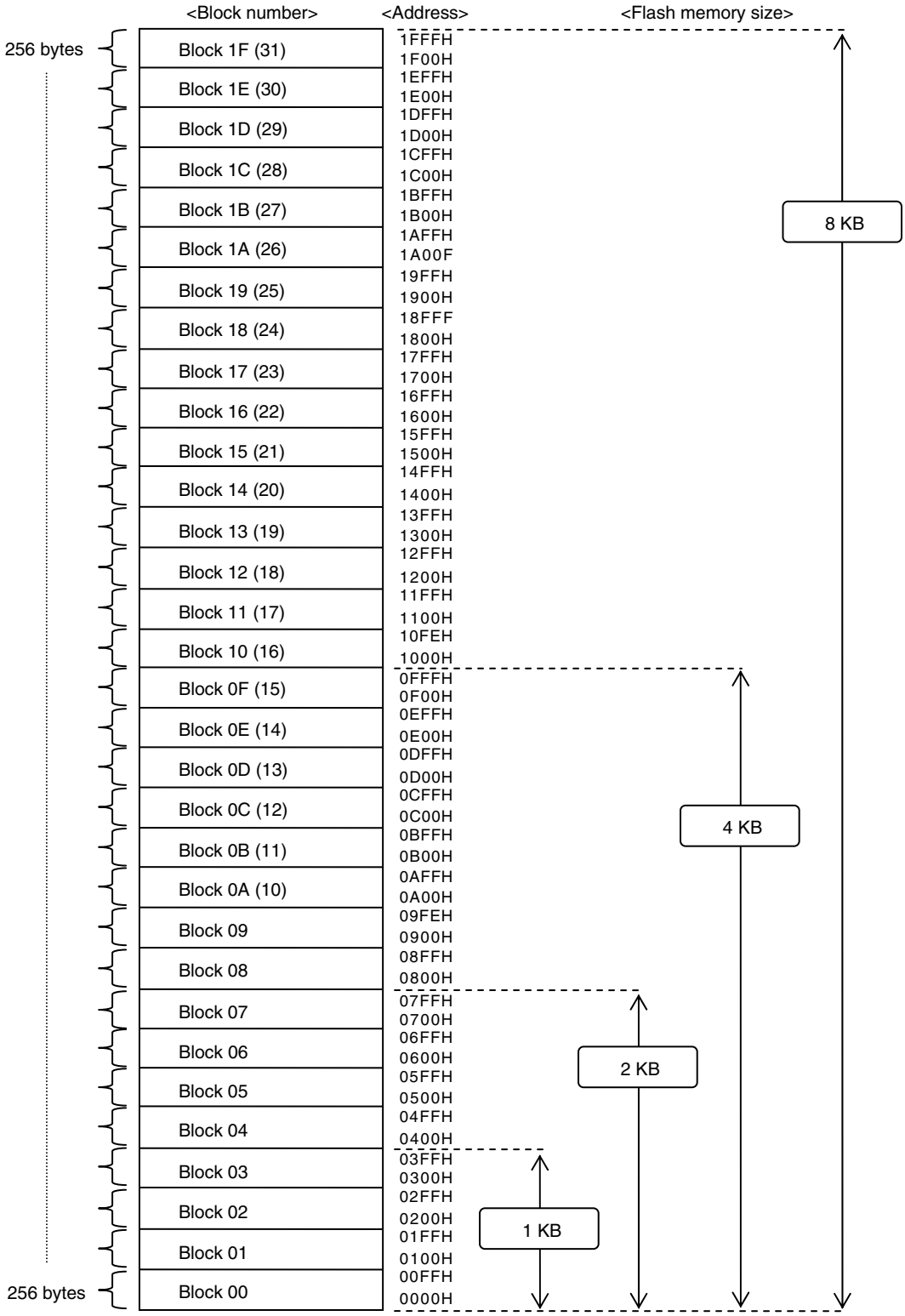
Table 1-1 shows the flash memory size of the 78K0S/Kx1+ and Figure 1-3 shows the configuration of the flash memory.

<R>

Table 1-1. Flash Memory Size of 78K0S/Kx1+

Device Name		Flash Memory Size
78K0S/KU1+	μPD78F9200	1 KB
	μPD78F9201	2 KB
	μPD78F9202	4 KB
78K0S/KY1+	μPD78F9210	1 KB
	μPD78F9211	2 KB
	μPD78F9212	4 KB
78K0S/KA1+	μPD78F9221	2 KB
	μPD78F9222	4 KB
78K0S/KB1+	μPD78F9232	4 KB
	μPD78F9234	8 KB

Figure 1-3. Flash Memory Configuration



CHAPTER 2 COMMUNICATION PROTOCOL

2.1 Communication Settings

Communication between the programmer and 78K0S/Kx1+ is established by a single-wire UART.

Table 2-1 shows the basic protocol of the single-wire UART.

Table 2-1. Basic Protocol

Item	Description
Direction	LSB first
Parity bit	Even parity
Stop bit	1 bit
Data length	8 bits
Typical clock[Note] (DGCLK)	8 MHz ±1%
Typical baud rate	115200 bps

Note Output the typical baud rate after setting the flash memory programming mode.

Caution Check the series/parallel resonant frequency and anti-resonant frequency of the oscillator used on the target system, and set the oscillation frequency to be supplied from the programmer to a value skewed at least 10% from the resonant frequency.

To supply a clock to DGCLK, use of the combination of the typical baud rate and typical clock is recommended.

When supplying the clock to DGCLK while the resonator is mounted on the target system, the clock and baud rate combinations listed in Table 2-2 can also be used.

Table 2-2. Combinations of Clock and Baud Rate (When Resonator Is Mounted on Target System)

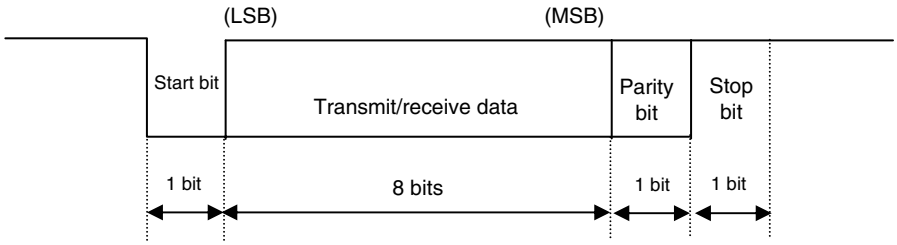
Clock	Baud Rate
10 MHz ±1%	144000 bps
9 MHz ±1%	129600 bps
6 MHz ±1%	86400 bps

2.2 Frame Format

2.2.1 Communication data format

Figure 2-1 shows the format of communication data.

Figure 2-1. Communication Data Format



2.2.2 Command frame format (from programmer to 78K0S/Kx1+)

Communications are performed using the following format for four fields in the command frame.

Command field (1 byte)	Block field (1 byte)	Offset field (1 byte) Fixed to 00H	Last address field (1 byte)

2.2.3 Description of fields

Each of the above fields is explained below. If an illegal value is transmitted in the command field, status code "Unknown error (01H)" is returned.

Table 2-3. Description of Fields

Field	Description	Value
Command	Command number	19H, 20H, 22H, 30H, 32H, 40H, B0H, A0H
Block	Block number	00H to 1FH[Note]
Offset	Fixed value	00H
Last address	Value of lowest byte of last address to be written	FFH, 00H

Note The usable block number differs as follows depending on the flash memory size.

<Flash memory size>	<Block number>
1 KB	00H to 03H
2 KB	00H to 07H
4 KB	00H to 0FH
8 KB	00H to 1FH

2.2.4 Status data format (from 78K0S/Kx1+ to programmer)

As a response from the 78K0S/Kx1+, 1-byte status data is transmitted to the programmer.

2.2.5 Checksum data format (from 78K0S/Kx1+ to programmer)

As a response to the Checksum command transmitted from the programmer, the 78K0S/Kx1+ transmits 2-byte checksum data to the programmer. The lower byte and the higher byte of the checksum data are transmitted in that order.

CHAPTER 3 SETTING FLASH MEMORY PROGRAMMING MODE

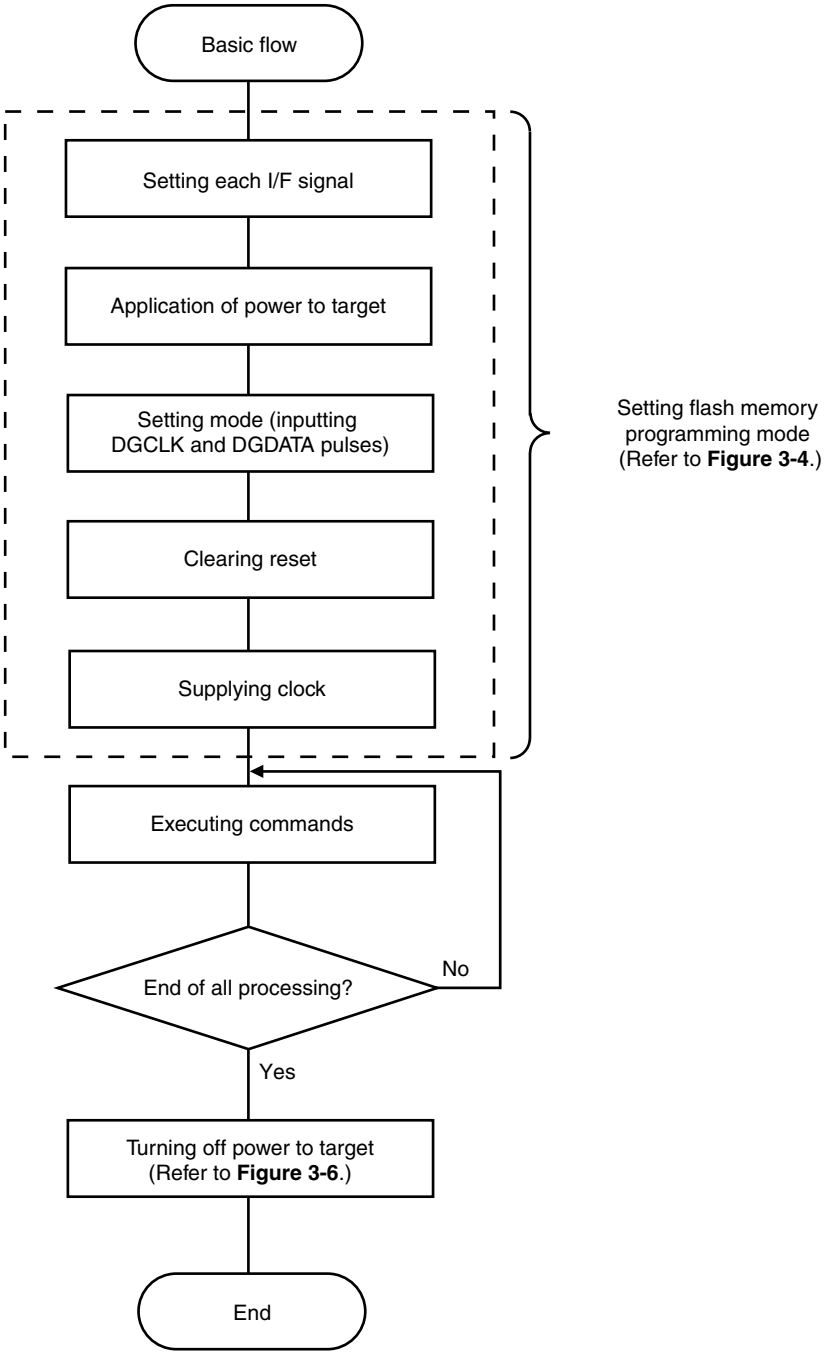
To rewrite the contents of the flash memory with the programmer, the 78K0S/Kx1+ must first be set in the flash memory programming mode.

The mode is set if a specific sequence of the DGCLK, DGDATA, and $\overline{\text{RESET}}$ pins is detected after the internal reset signal is cleared by the power-on clear (POC) circuit.

Supply V_{DD} starting from 0 V to ensure the correct operation of the power-on clear (POC) circuit.

Figure 3-1 shows the basic flow for setting the programmer.

Figure 3-1. Basic Flow for Setting Programmer



3.1 Procedure for Setting Flash Memory Programming Mode

The procedure for setting the flash memory programming mode is as follows.

<Step 1: Initializing hardware>

First, drive the $\overline{\text{RESET}}$ pin low, and the DGCLK and DGDATA pins high.

Pull up the DGCLK and DGDATA pins with a resistor of several kΩ each (the DGCLK and DGDATA pins are pulled down by a high resistance (30 kΩ typ.) inside the 78K0S/Kx1+ when $\overline{\text{RESET}}$ is input).

After power application, an internal reset signal is generated by the POC circuit, and each hardware unit is initialized.

<Step 2: Setting mode>

Set the 78K0S/Kx1+ in the flash memory programming mode as follows.

To set the flash memory programming mode, pulses of the following formats must be transmitted from the programmer to the DGCLK and DGDATA pins while the $\overline{\text{RESET}}$ pin is at low level after the internal reset signal has been cleared by the POC circuit.

- From programmer to DGCLK pin
  Input a single-shot pulse of high → low → high.
- From programmer to DGDATA pin
  Input five pulses of high → low → high after inputting the single-shot pulse to the DGCLK pin.

If an extra pulse is input to the DGCLK pin or if the number of clocks input to the DGDATA pin runs short, the flash memory programming mode is not specified but the normal operation mode is specified.

<Step 3: Fixing mode and manipulating flash programming>

After steps 1 and 2, make the $\overline{\text{RESET}}$ pin to determine the flash memory programming mode. After the mode has been determined, supply the clock from the programmer to the DGCLK pin. After a specific internal stabilization time, the 78K0S/Kx1+ enters a command wait status.

Timing charts illustrating the procedure for setting the flash memory programming mode and the flow for setting the mode are shown below.

For the value of Tx in the following figures, refer to **CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS**.

Figure 3-2. Timing of Changing Mode to Flash Memory Programming Mode (When Mode Is Set and Command Is Executed)

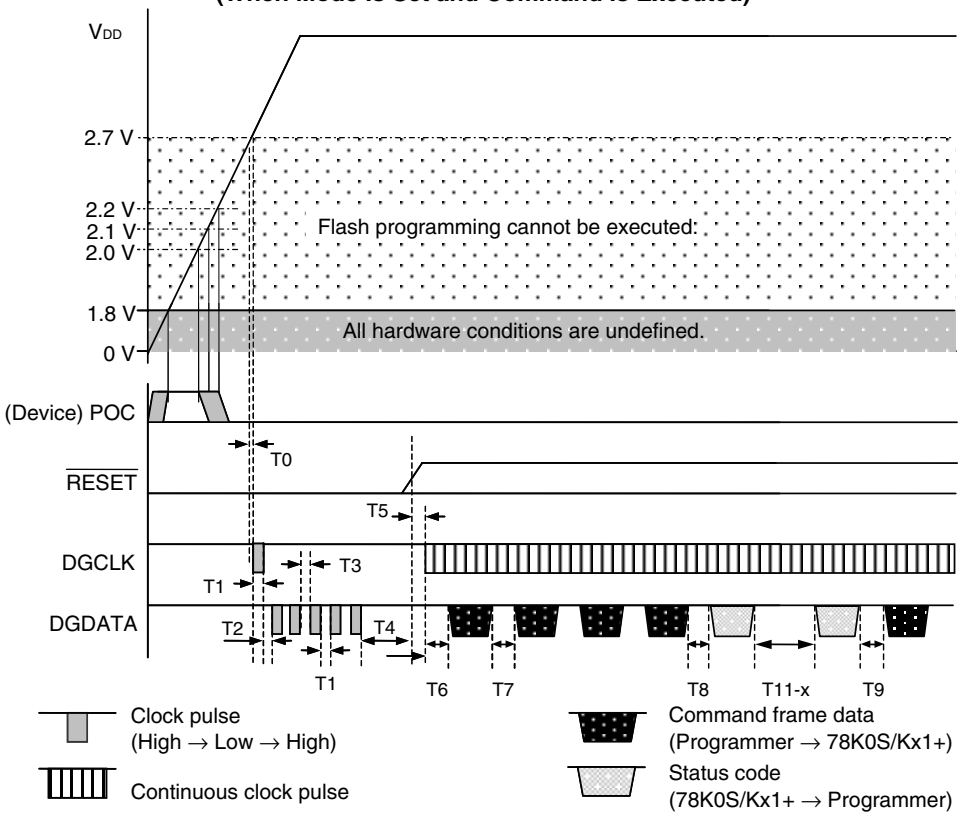


Figure 3-3. Timing of Changing Mode to Flash Memory Programming Mode (When Command Is Executed)

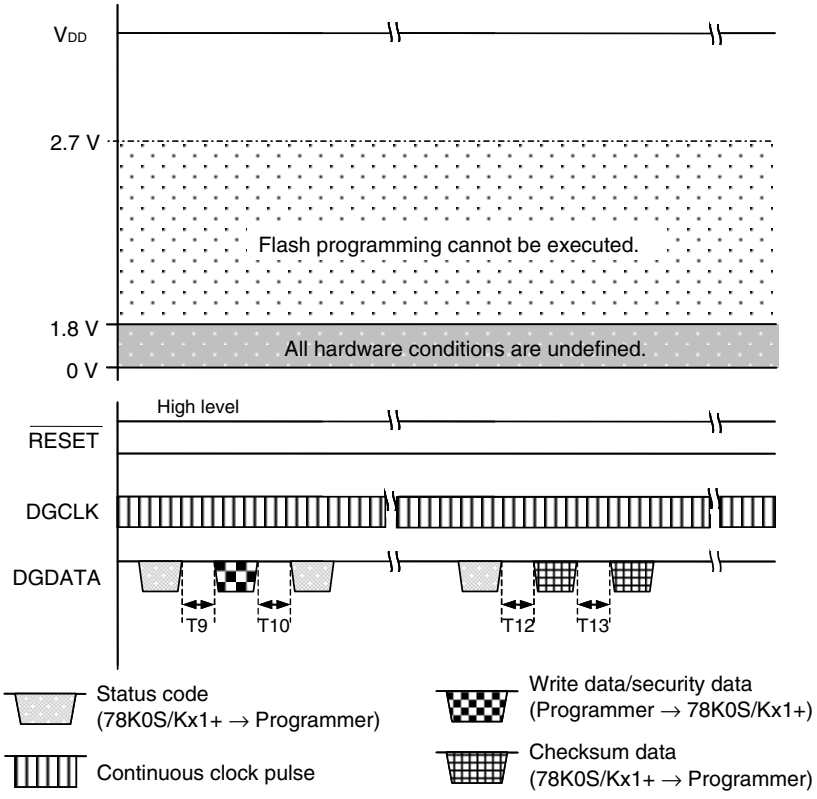
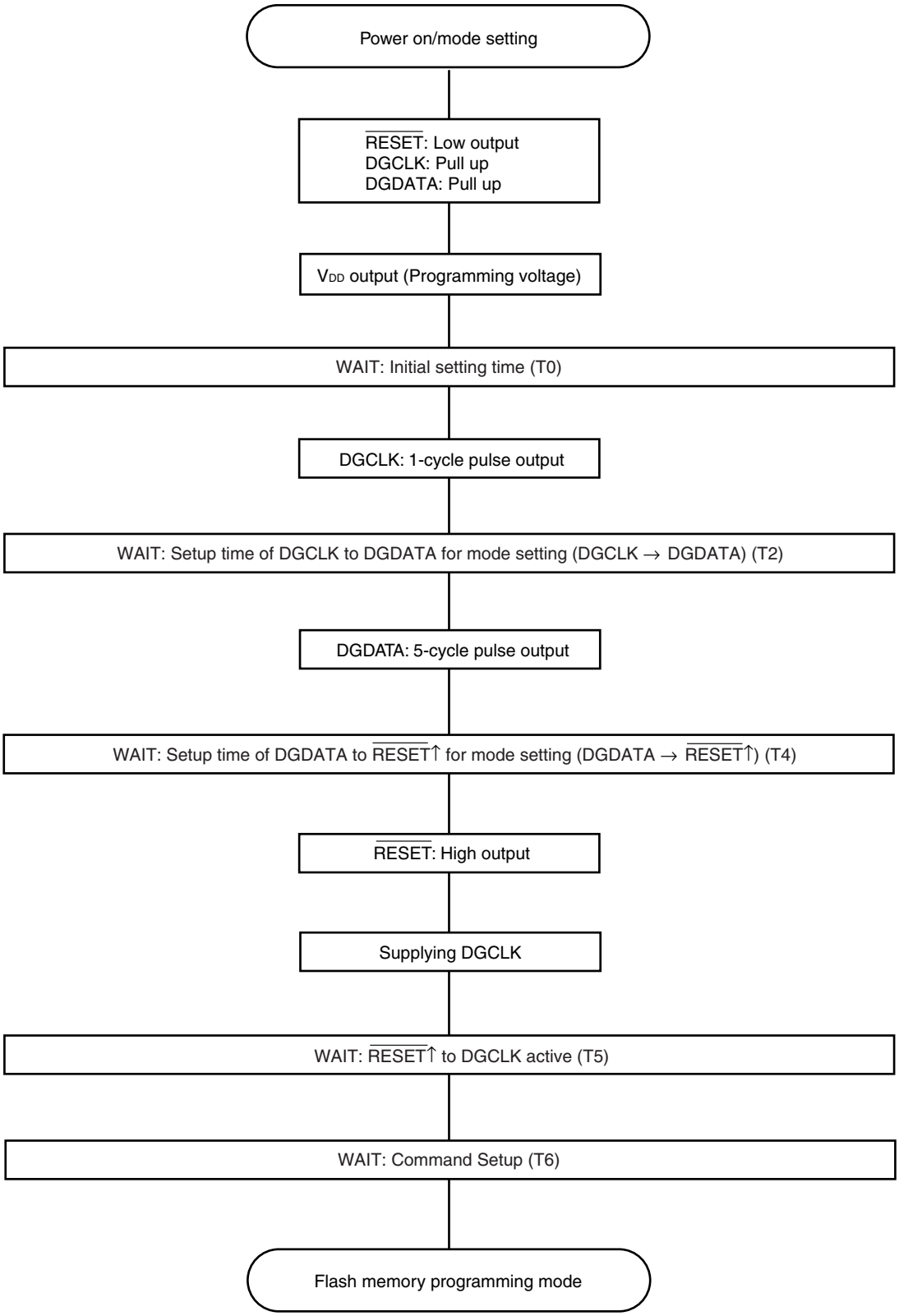


Figure 3-4. Flow for Setting Flash Memory Programming Mode



3.2 Exiting from Flash Memory Programming Mode

To exit from the flash memory programming mode, stop outputting DGCLK, input a low level to the $\overline{\text{RESET}}$ pin, and turn off the power to the 78K0S/Kx1+.

A timing chart and a flowchart illustrating the procedure for exiting from the flash memory programming mode are shown below.

Caution Stop outputting DGCLK at the appropriate time after a status code such as ACK has been received. Do not input the reset signal or turn off power during command processing.

Figure 3-5. Timing of Exiting from Flash Memory Programming Mode

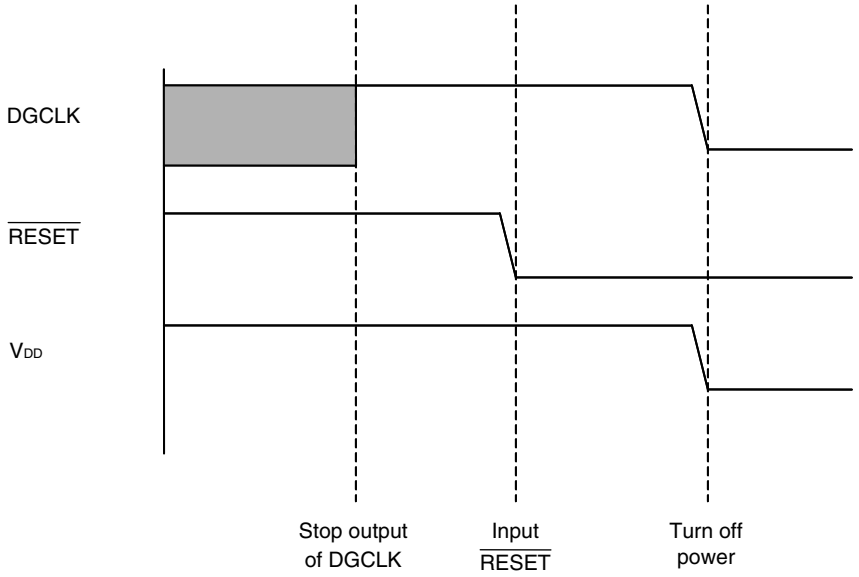


Figure 3-6. Flow for Exiting from Flash Memory Programming Mode

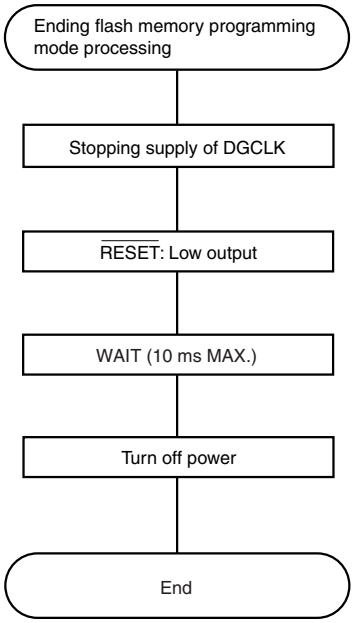
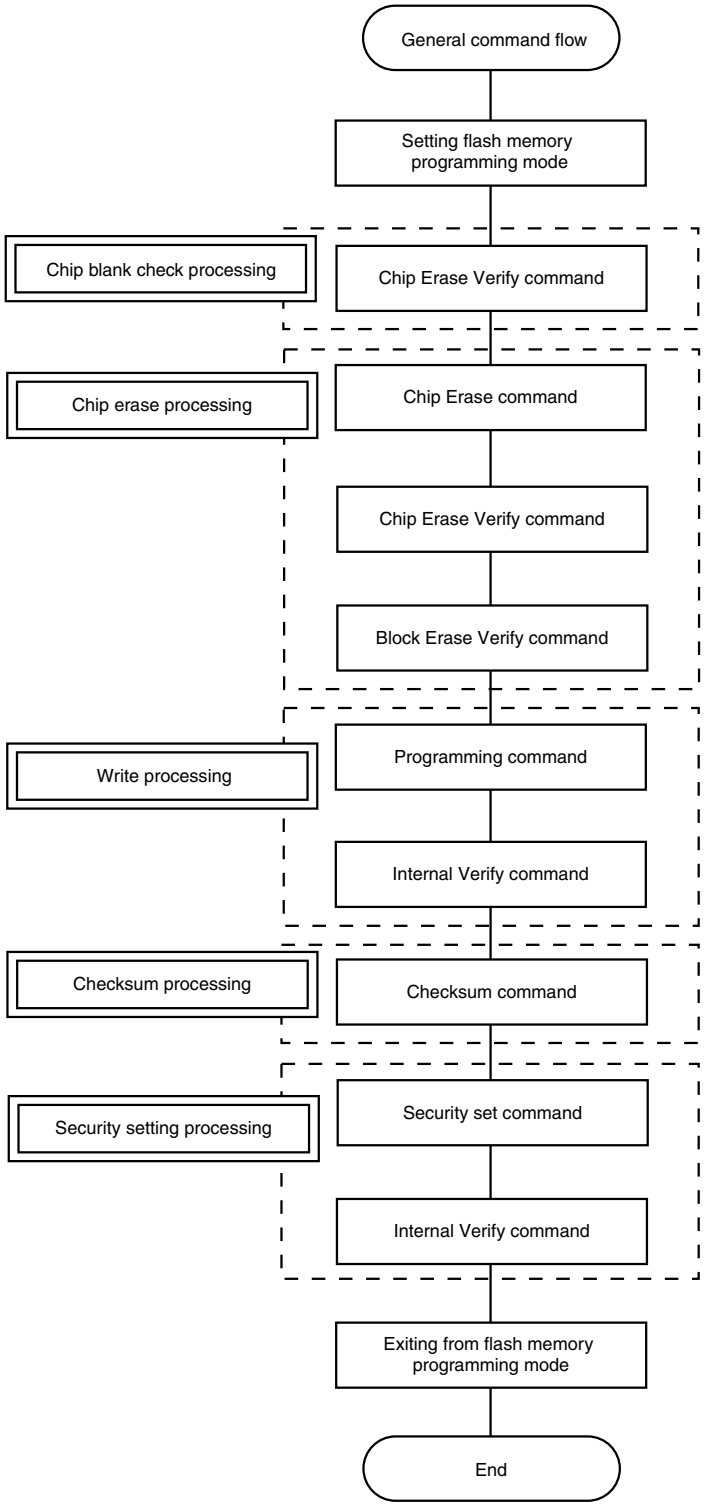


Figure 4-1 shows the general command flow for rewriting the flash memory with the programmer.

<R> **Figure 4-1. General Command Flow for Rewriting**



Remark In addition to the above processing, block blank check processing and block erase processing can also be supported.

4.1 Command Overview

The commands used by the programmer and their functions are listed below.

Table 4-1. Command List

Command No.	Command Name	Function
20H	Chip Erase	Erases the entire flash memory. This command also initializes the information set by the Security set command. After executing this command, be sure to execute the Chip Erase Verify and Block Erase Verify commands.
30H	Chip Erase Verify	Checks the erasure level of the entire flash memory.
22H	Block Erase	Erases a specified block of the flash memory. After executing this command, be sure to execute the Block Erase Verify command.
32H	Block Erase Verify	Checks the erasure level of a specified block.
40H	Programming	Writes data to a specified block. Before executing this command, be sure to perform an Erase operation (Chip/Block). After executing the command, be sure to execute the Internal Verify command.
19H	Internal Verify	Checks the write level of a specified block.
B0H	Checksum	Receives the checksum value of the data of a specified block.
40H	Security set	Sets security information. After executing this command, be sure to execute the Internal Verify command.

4.2 Status List

The following table lists the status codes the programmer receives from the 78K0S/Kx1+.

Table 4-2. Status Code List

Status Code	Status	Description
01H	Unknown error	Error if a command not supported or an abnormal frame is received
06H	Normal acknowledgment (ACK)	Normal acknowledgment. This status code is returned when: • A command has been correctly received. • Write data has been received. • The next write data is received and then 1 byte has been written. • One byte has been written. • Chip Erase Verify has been correctly completed. • Block Erase Verify has been correctly completed. • Internal Verify has been correctly completed.
15H	Negative acknowledgement (NACK)	Negative acknowledgement. This status code is returned if a parity error is found in a command or data.
1AH	MRG10 error	Erase verify error
1BH	MRG11 error	Internal verify error
1CH	Write error	Write error
1DH	Write data received but write error	Error if write error has been received but writing failed
1EH	Write data received error and write error	Error if both reception of write data and writing failed
1FH	Write data received error but write OK	Error if receiving write data failed but writing succeeded
FFH	Processing in progress (BUSY)	–

4.3 Chip Blank Check Processing

4.3.1 Description

This processing is to check whether the data has been erased from the entire flash memory.

<R> To execute chip blank check processing, execute the Chip Erase Verify command.

4.3.2 Basic command frame

Figures 4-2 shows the command frame executed for chip blank check processing.

Figure 4-2. Chip Erase Verify Command Frame

Field	Command	Block	Offset	Last address
Value	30H	Maximum block number[Note]	00H	FFH

Note The value that is valid as the maximum block number differs as follows depending on the flash memory size.

<Flash memory size>	<Block number>
1 KB	03H
2 KB	07H
4 KB	0FH
8 KB	1FH

4.3.3 Normal termination

<R> To execute chip blank check processing, execute the Chip Erase Verify command.

The processing flow between the 78K0S/Kx1+ and programmer when the processing is terminated normally is as follows.

<1> The programmer transmits the Chip Erase Verify command to the 78K0S/Kx1+.

<2> The 78K0S/Kx1+ transmits ACK when it has received the Chip Erase Verify command, and starts verification of erasure.

<3> The programmer receives ACK that indicates the end of erasure verification. This completes the chip blank check processing.

4.3.4 Abnormal termination

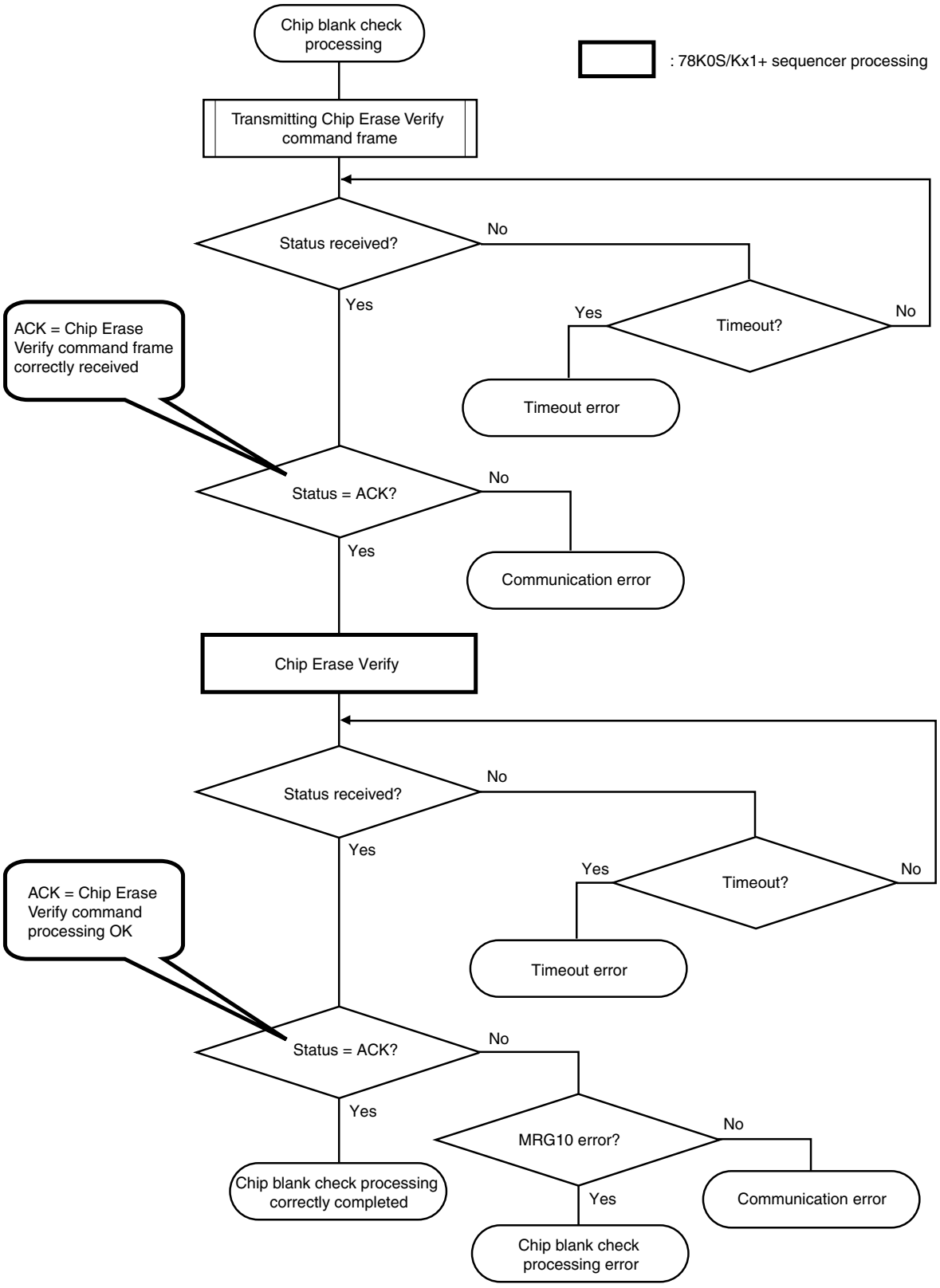
Abnormal termination occurs in the following three cases.

- If a parity error occurs when the 78K0S/Kx1+ receives a command from the programmer, the 78K0S/Kx1+ returns NACK. After that, the 78K0S/Kx1+ enters the command wait status.
- If the command transmitted from the programmer is not supported or in an abnormal format, the 78K0S/Kx1+ returns Unknown error. The 78K0S/Kx1+ then enters the command wait status.
- <R> If an error is detected in the Chip Erase Verify command, the 78K0S/Kx1+ terminates erasure verification processing and returns an error status (MRG 10 error). If this happens, the programmer terminates chip blank check processing, assuming that a chip blank check processing error has occurred.

4.3.5 Command flow

Figure 4-3 shows the flow of chip blank check processing.

<R> **Figure 4-3. Chip Blank Check Processing Flow**

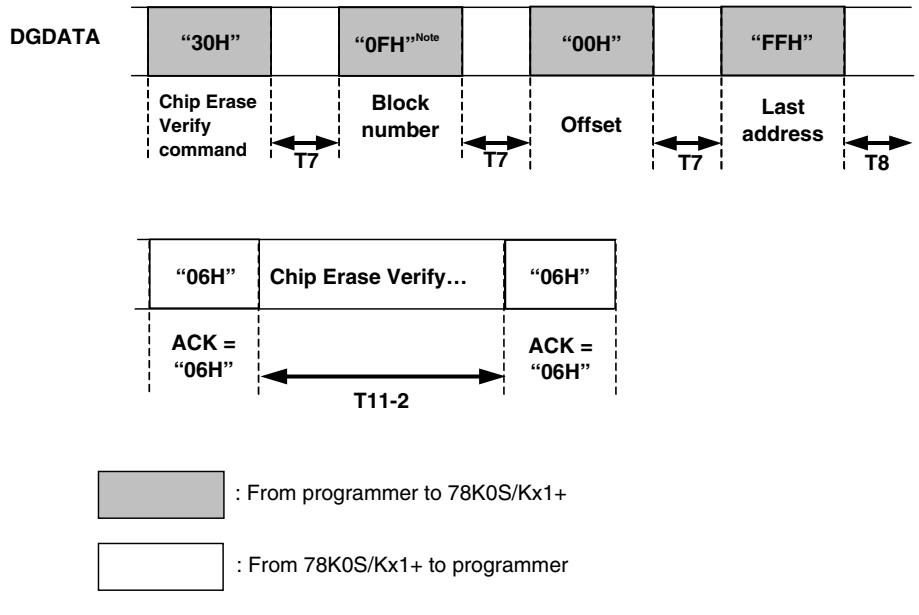


4.3.6 Timing chart

Figure 4-4 shows the timing of chip blank check processing.

For the value of Tx in the chart, refer to **CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS**.

<R> **Figure 4-4. Timing Chart of Chip Blank Check Processing**



Note This is the block number when the flash memory size is 4 KB.
It differs depending on the flash memory size.

4.4 Block Blank Check Processing

4.4.1 Description

This processing is to check whether the data of the block of the flash memory of a specified block number has been erased by execution of the Block Erase Verify command.

4.4.2 Basic command frame

The basic command frame of the command executed for block blank check processing is as shown in Figure 4-5.

Figure 4-5. Block Erase Verify Command Frame

Field	Command	Block	Offset	Last address
Value	32H	Block number[Note]	00H	FFH

Note The value valid as a block number differs as follows depending on the flash memory size.

<Flash memory size>	<Block number>
1 KB	00H to 03H
2 KB	00H to 07H
4 KB	00H to 0FH
8 KB	00H to 1FH

4.4.3 Normal termination

The Block Erase Verify command is executed for block blank check processing.

If command execution is terminated normally, the processing flow between the 78K0S/Kx1+ and programmer is as follows.

<1> The programmer transmits the Block Erase Verify command to the 78K0S/Kx1+.
<2> When the 78K0S/Kx1+ receives the Block Erase Verify command, it transmits ACK and starts verification of erasure.
<3> The program receives ACK that indicates completion of erasure verification, completing the block blank check processing.

4.4.4 Abnormal termination

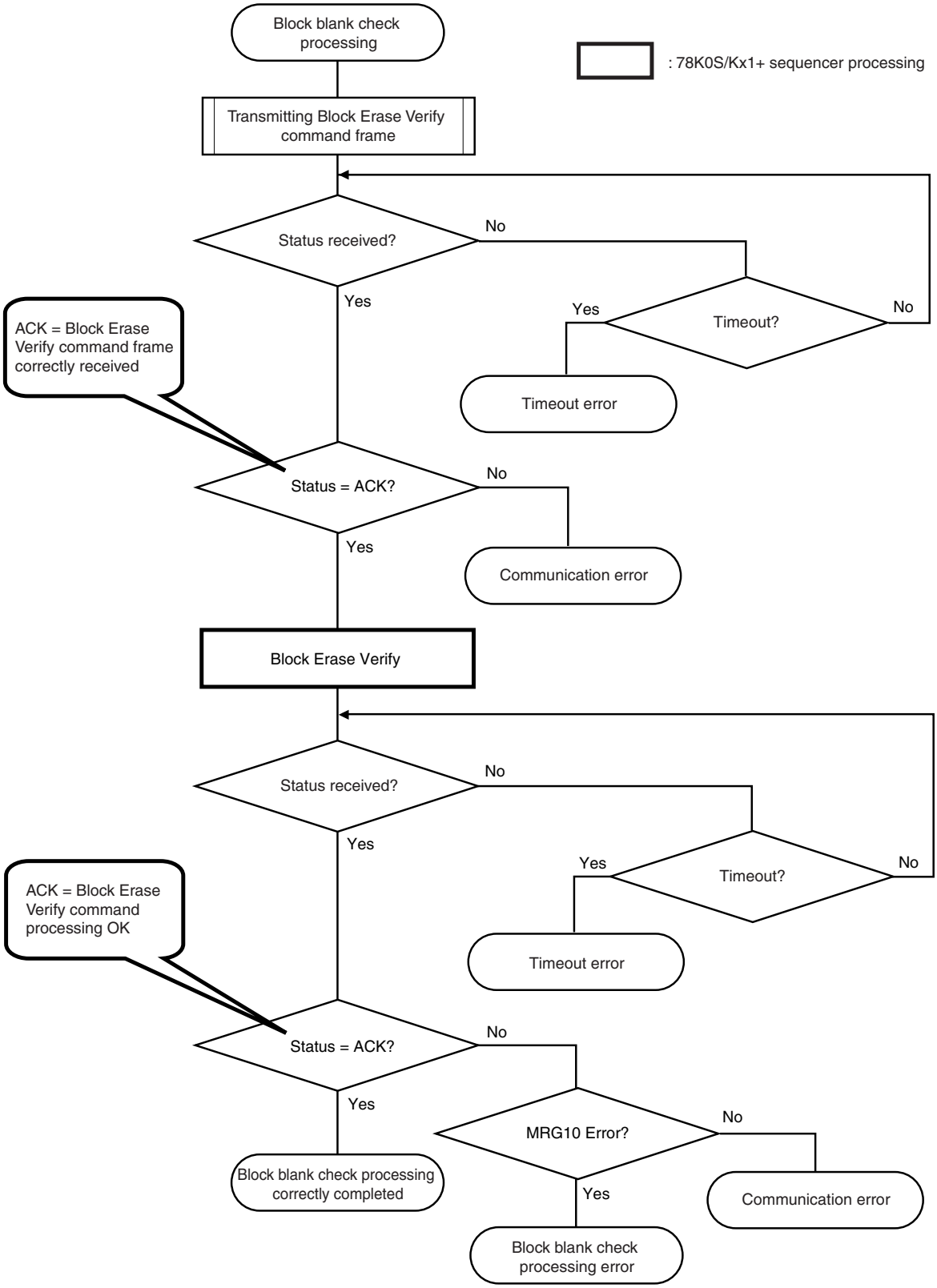
Abnormal termination occurs in the following three cases.

- If a parity error occurs when the 78K0S/Kx1+ receives a command from the programmer, the 78K0S/Kx1+ returns NACK. After that, the 78K0S/Kx1+ enters the command wait status.
- If the command transmitted from the programmer is not supported or in an abnormal format, the 78K0S/Kx1+ returns Unknown error. The 78K0S/Kx1+ then enters the command wait status.
- If an error is detected in the Block Erase Verify command, the 78K0S/Kx1+ terminates erasure verification processing and returns an error status (MRG 10 error). If this happens, the programmer terminates block blank check processing, assuming that a block blank check processing error has occurred.

4.4.5 Command flow

Figure 4-6 shows the flow of block blank check processing.

Figure 4-6. Block Blank Check Processing Flow

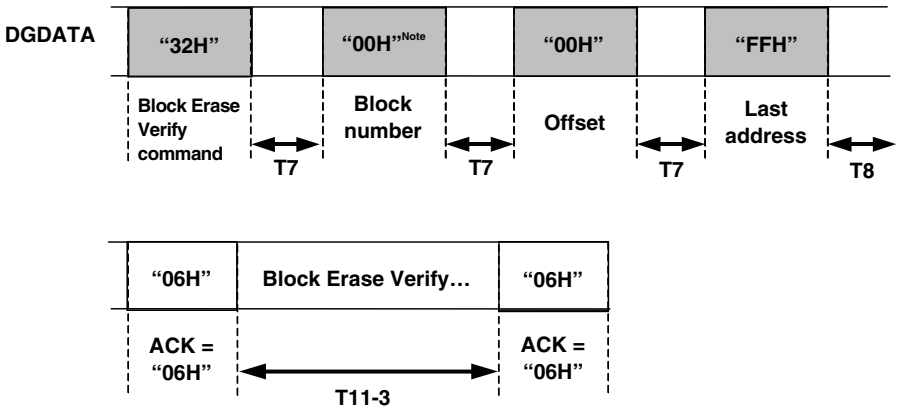


4.4.6 Timing chart

Figure 4-7 shows the timing of block blank check processing.

For the value of Tx in the chart, refer to **CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS**.

Figure 4-7. Timing Chart of Block Blank Check Processing



: From programmer to 78K0S/Kx1+

: From 78K0S/Kx1+ to programmer

Note This is the block number when block blank check is performed for block 00.

4.5 Chip Erase Processing

4.5.1 Description

This processing is to erase the entire flash memory (chip).

All the information set by the Security set command can also be initialized.

However, chip erase cannot be executed when erasing the chip is prohibited.

To execute chip erase processing, execute the Chip Erase, Chip Erase Verify, and Block Erase Verify commands in succession.

4.5.2 Basic command frame

The basic command frames of the three commands executed for chip erase processing are as shown in Figures 4-8 to 4-10.

Figure 4-8. Chip Erase Command Frame

Field	Command	Block	Offset	Last address
Value	20H	Maximum block number[Note]	00H	FFH

Figure 4-9. Chip Erase Verify Command Frame

Field	Command	Block	Offset	Last address
Value	30H	Maximum block number[Note]	00H	FFH

Note The value valid as the maximum block number differs as follows depending on the flash memory size.

<Flash memory size>	<Block number>
1 KB	03H
2 KB	07H
4 KB	0FH
8 KB	1FH

Figure 4-10. Block Erase Verify Command Frame

Field	Command	Block	Offset	Last address
Value	32H	80H (fixed)	00H	FFH

4.5.3 Normal termination

To execute chip erase processing, be sure to execute the Chip Erase, Chip Erase Verify, and Block Erase Verify commands in succession.

If command execution is terminated normally, the processing flow between the 78K0S/Kx1+ and programmer is as follows.

<1> The programmer transmits the Chip Erase command to the 78K0S/Kx1+.
<2> When the 78K0S/Kx1+ receives the Chip Erase command, it transmits ACK and starts erasing the chip.
<3> When the programmer receives ACK that indicates the completion of erasing processing, it transmits the Chip Erase Verify command.
<4> When the 78K0S/Kx1+ receives the Chip Erase Verify command, it transmits ACK and starts verifying if the chip has been correctly erased.
<5> When the programmer receives ACK that indicates completion of verification of erasure, it transmits the Block Erase Verify command to block 80H.
<6> When the 78K0S/Kx1+ receives the Block Erase Verify command, it transmits ACK and starts verifying whether block 80H has been correctly erased.
<7> When the programmer receives ACK that indicates completion of verification of erasure, the chip erase processing is completed.

4.5.4 Abnormal termination

Abnormal termination occurs in the following three cases.

- If a parity error occurs when the 78K0S/Kx1+ receives a command from the programmer, the 78K0S/Kx1+ returns NACK. After that, the 78K0S/Kx1+ enters the command wait status.
- If the command transmitted from the programmer is not supported or in an abnormal format, the 78K0S/Kx1+ returns Unknown error. The 78K0S/Kx1+ then enters the command wait status.
- If an error is detected in the Chip/Block Erase Verify command, the 78K0S/Kx1+ terminates erasure verification processing and returns an error status (MRG 10 error). If this happens, the programmer re-executes the Chip Erase and Chip/Block Erase Verify commands. The Chip Erase command is executed a total of 256 times. If the error status is not cleared after the command has been executed 256 times, the programmer terminates the chip erasure processing, assuming that a chip erase processing error has occurred.

4.5.5 Command flow

Figure 4-11 shows the flow of chip erase processing.

Figure 4-11. Chip Erase Processing Flow (1/3)

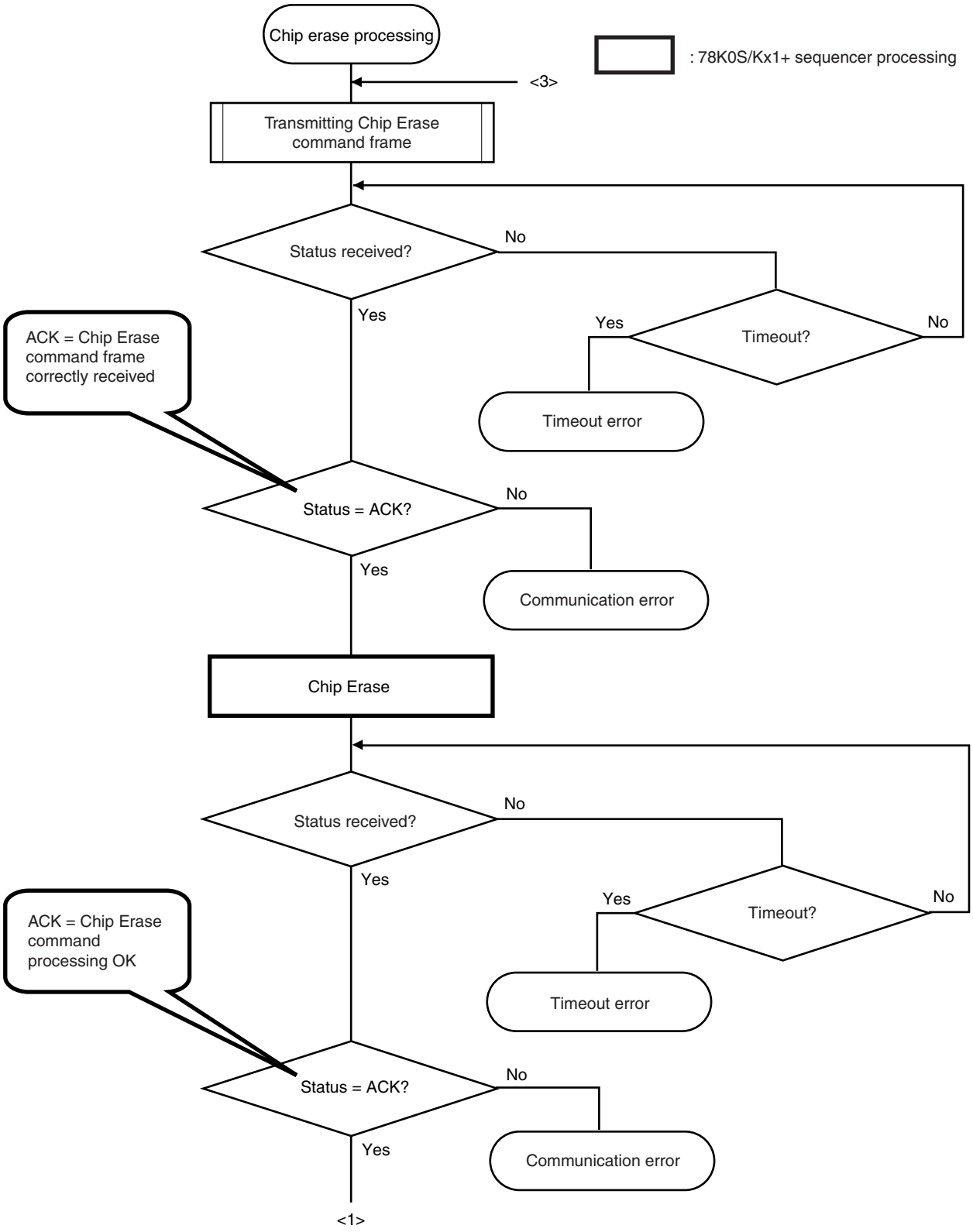


Figure 4-11. Chip Erase Processing Flow (2/3)

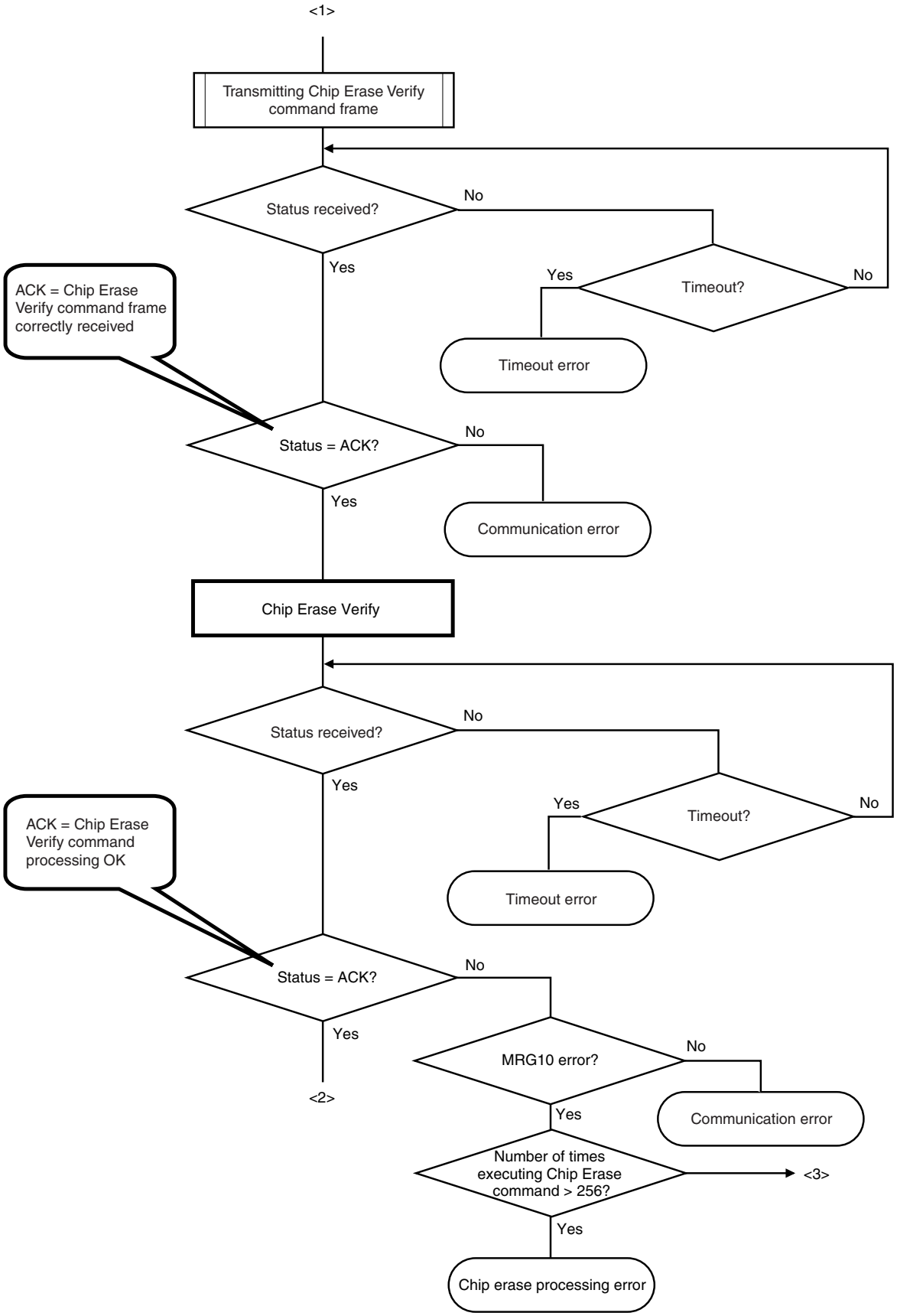
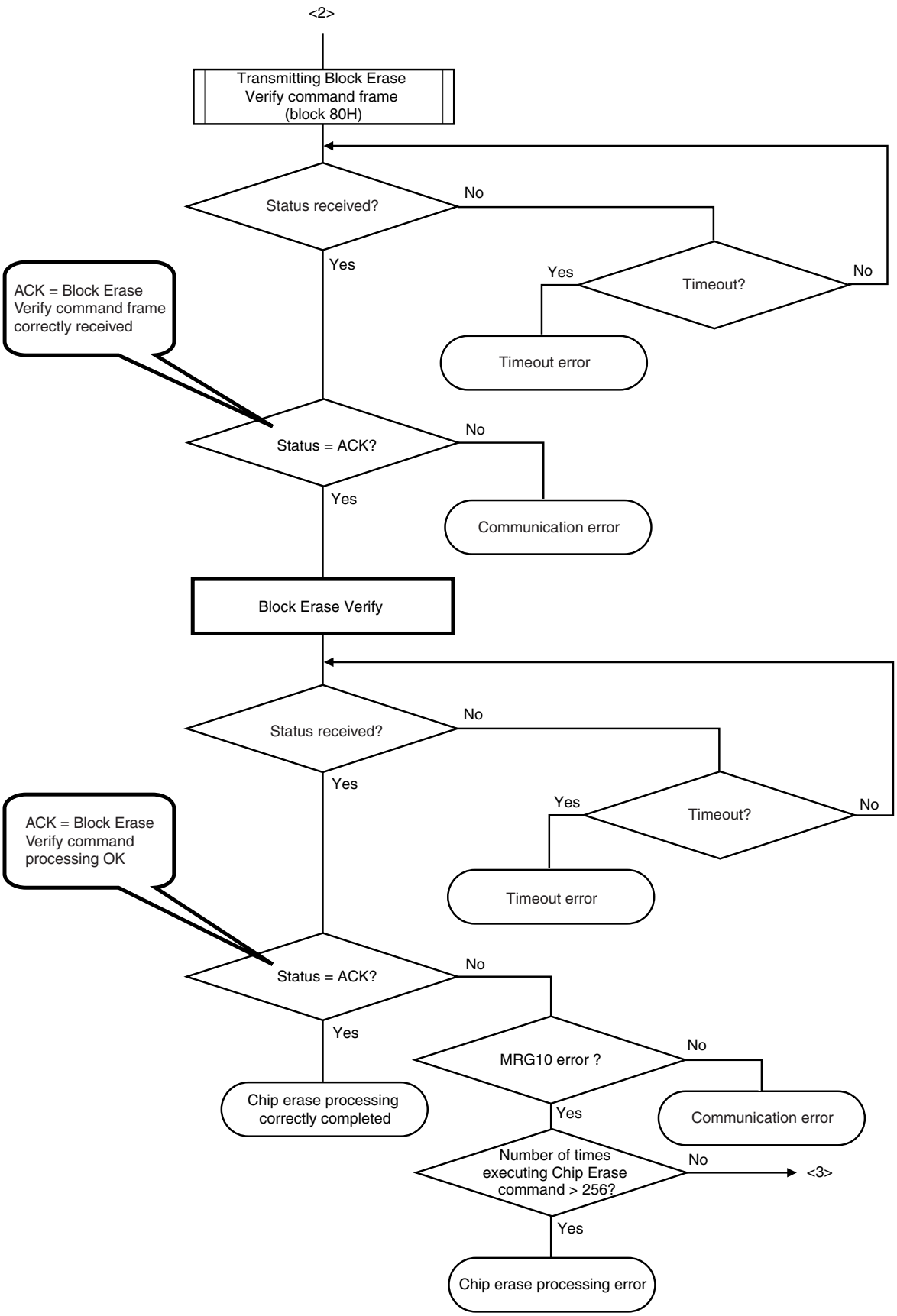


Figure 4-11. Chip Erase Processing Flow (3/3)

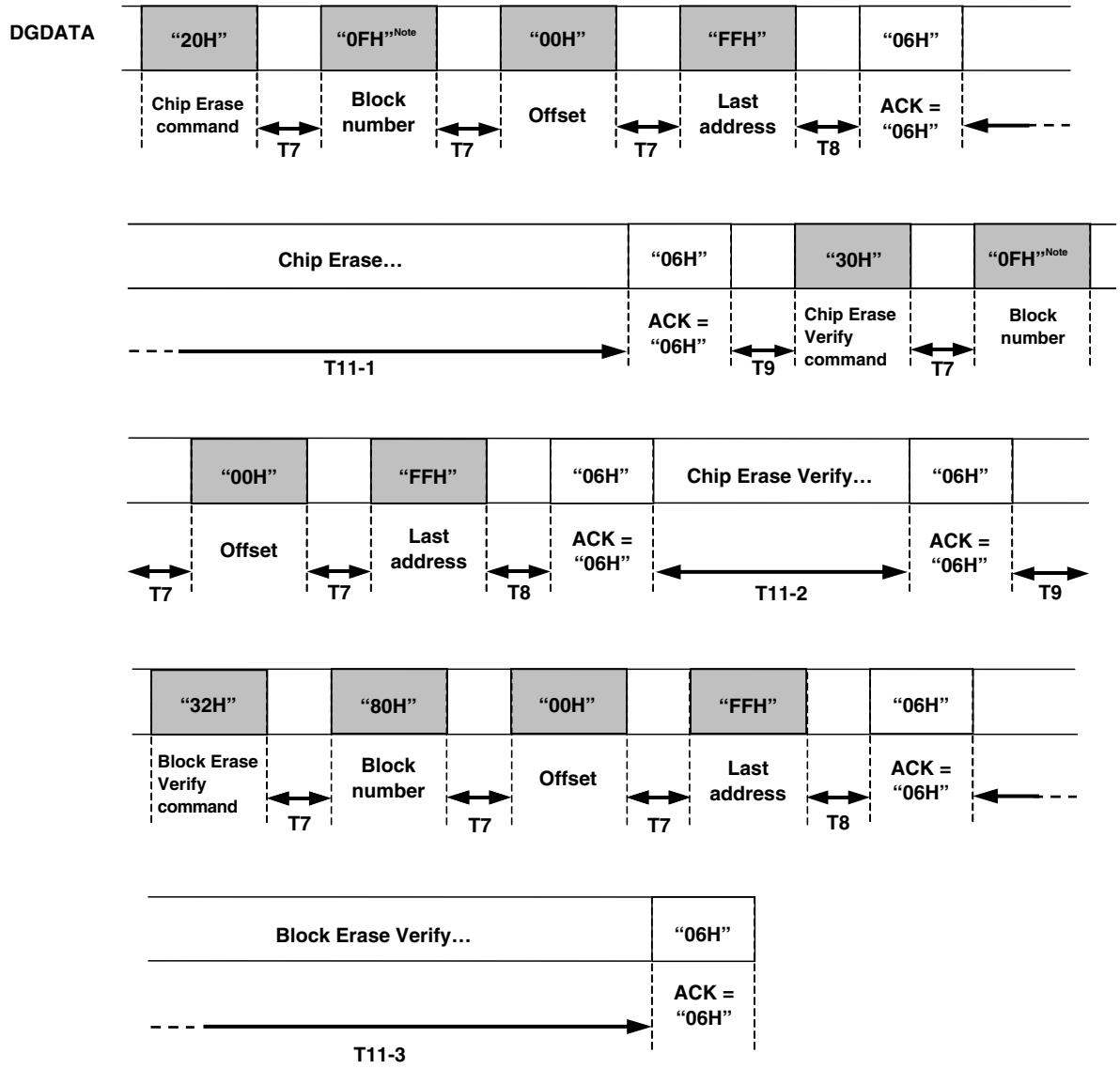


4.5.6 Timing chart

Figure 4-12 shows the timing of chip erase processing.

For the value of Tx in the chart, refer to **CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS**.

Figure 4-12. Timing Chart of Chip Erase Processing



: From programmer to 78K0S/Kx1+

: From 78K0S/Kx1+ to programmer

Note This is the block number when the flash memory size is 4 KB. It differs depending on the flash memory size.

4.6 Block Erase Processing

4.6.1 Description

This processing is to erase a block of the flash memory of a specified block number.

To erase a block, execute the Block Erase and Block Erase Verify commands in succession.

4.6.2 Basic command frame

The basic command frames of the two commands executed for block erase processing are as shown in Figures 4-13 and 4-14.

Figure 4-13. Block Erase Command Frame

Field	Command	Block	Offset	Last address
Value	22H	Block number[Note]	00H	FFH

Note The value valid as a block number differs as follows depending on the flash memory size.

<Flash memory size>	<Block number>
1 KB	00H to 03H
2 KB	00H to 07H
4 KB	00H to 0FH
8 KB	00H to 1FH

Figure 4-14. Block Erase Verify Command Frame

Field	Command	Block	Offset	Last address
Value	32H	Block number[Note]	00H	FFH

Note The block number of the Block Erase Verify command must be the same as the block number of the Block Erase command.

4.6.3 Normal termination

To execute block erase processing, be sure to execute the Block Erase and Block Erase Verify commands in succession.

If command execution is terminated normally, the processing flow between the 78K0S/Kx1+ and programmer is as follows.

<1> The programmer transmits the Block Erase command to the 78K0S/Kx1+.
<2> When the 78K0S/Kx1+ receives the Block Erase command, it transmits ACK and starts erasing the block.
<3> When the programmer receives ACK that indicates the completion of erasing processing, it transmits the Block Erase Verify command.
<4> When the 78K0S/Kx1+ receives the Block Erase Verify command, it transmits ACK and starts verifying if the block has been correctly erased.
<5> When the programmer receives ACK that indicates completion of verification of erasure, the block erase processing is completed.

4.6.4 Abnormal termination

Abnormal termination occurs in the following three cases.

- If a parity error occurs when the 78K0S/Kx1+ receives a command from the programmer, the 78K0S/Kx1+ returns NACK. After that, the 78K0S/Kx1+ enters the command wait status.
- If the command transmitted from the programmer is not supported or in an abnormal format, the 78K0S/Kx1+ returns Unknown error. The 78K0S/Kx1+ then enters the command wait status.
- If an error is detected in the Block Erase Verify command, the 78K0S/Kx1+ terminates erasure verification processing and returns an error status (MRG 10 error). If this happens, the programmer re-executes the Block Erase and Block Erase Verify commands. The Block Erase command is executed a total of 256 times. If the error status is not cleared after the command has been executed 256 times, the programmer terminates the block erase processing, assuming that a block erase processing error has occurred.

4.6.5 Command flow

Figure 4-15 shows the flow of block erase processing.

Figure 4-15. Block Erase Processing Flow (1/2)

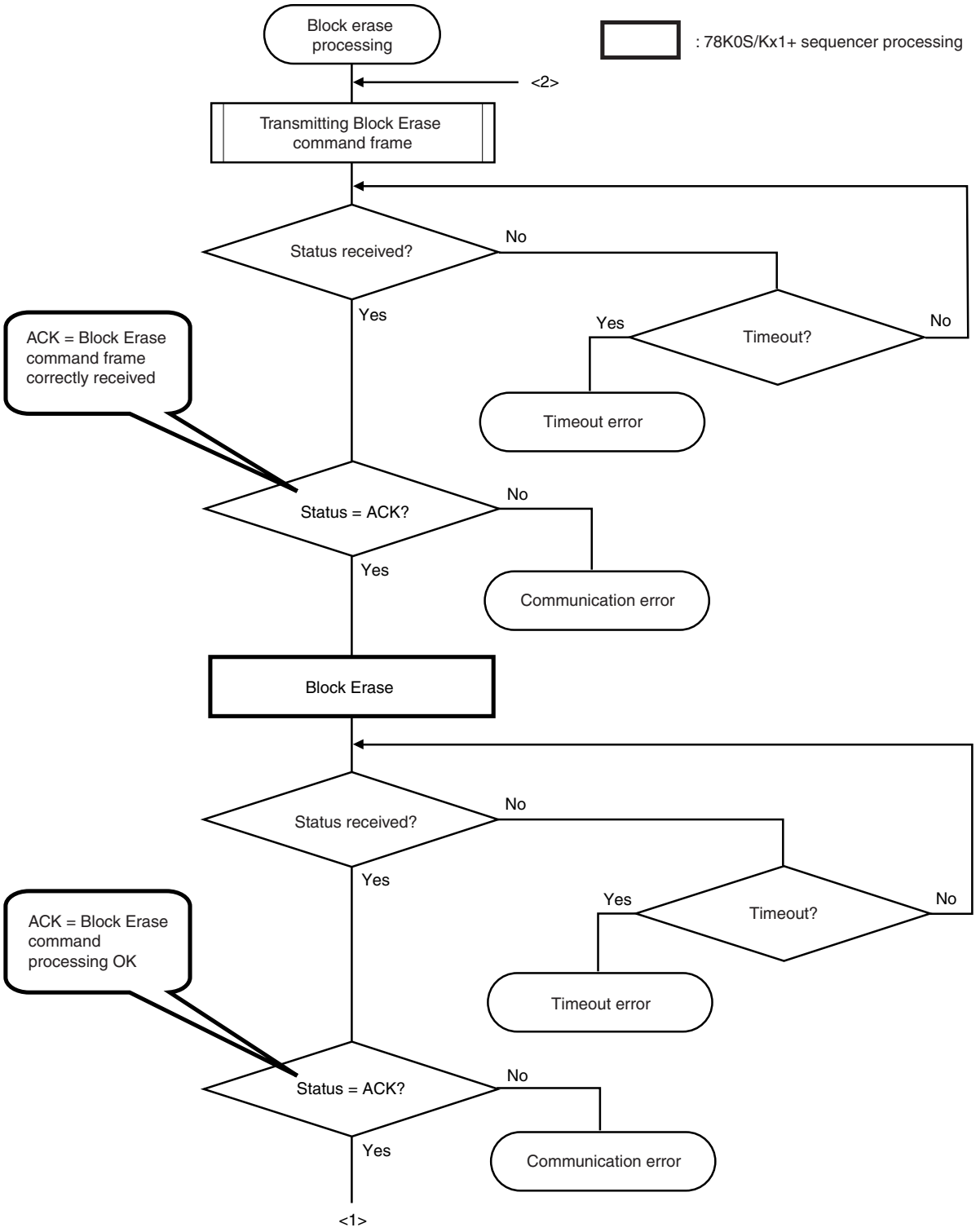
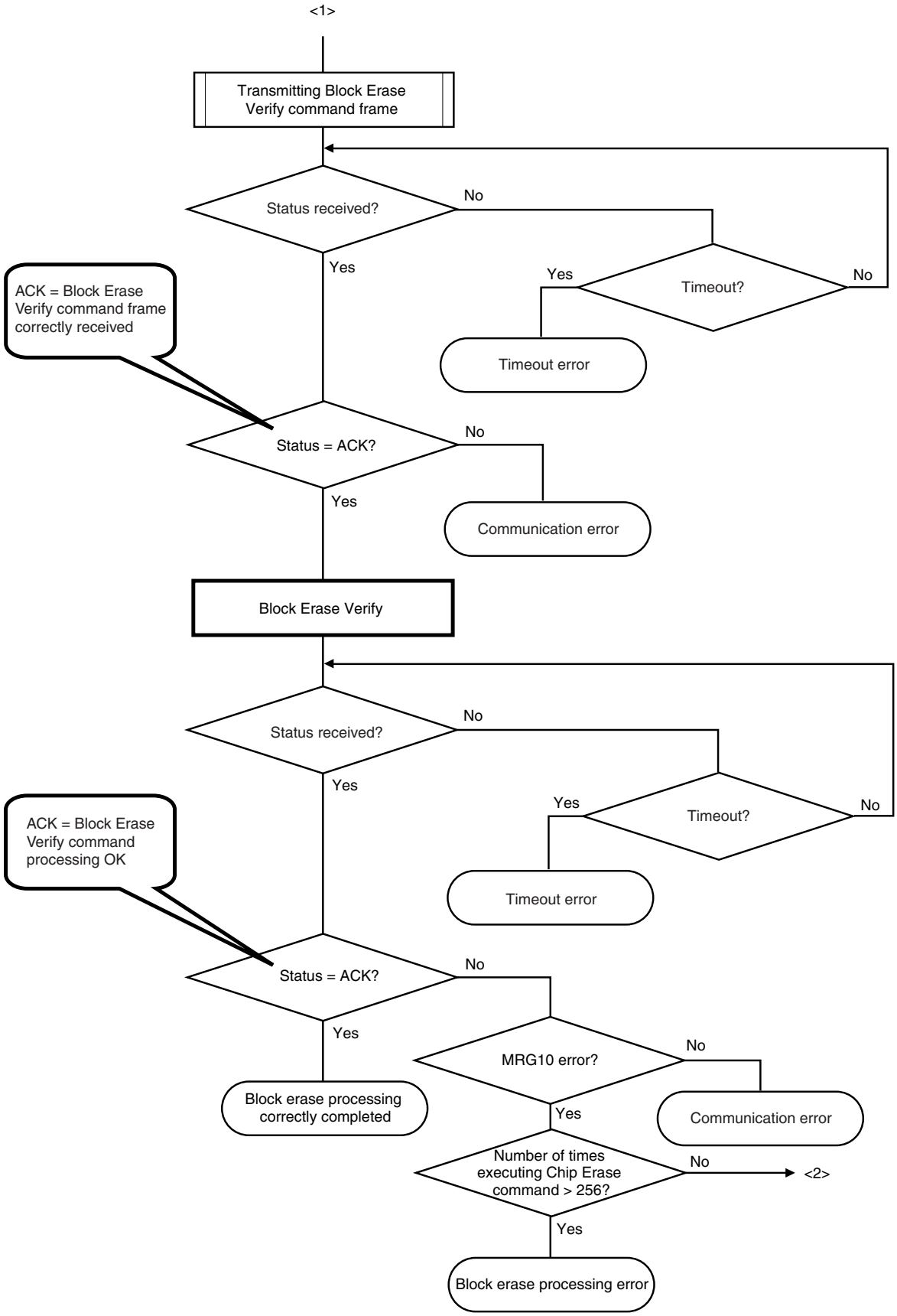


Figure 4-15. Block Erase Processing Flow (2/2)

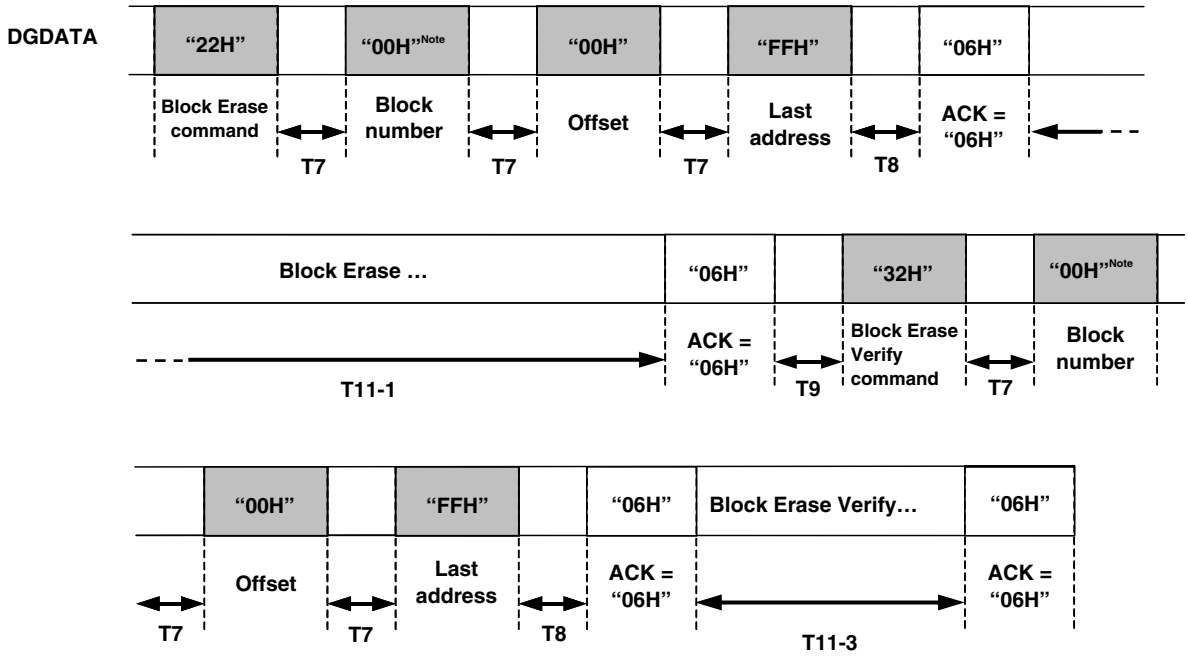


4.6.6 Timing chart

Figure 4-16 shows the timing of block erase processing.

For the value of Tx in the chart, refer to **CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS**.

Figure 4-16. Timing Chart of Block Erase Processing



Note This is the block number when block 00 is erased.

4.7 Write Processing

4.7.1 Description

This processing is to write a user program to the flash memory in block (256 bytes) units by executing the Programming command. After that, the Internal Verify command is executed to check the write level.

4.7.2 Basic command frame

The basic command frames of the two commands executed for write processing are as shown in Figures 4-17 and 4-18.

Figure 4-17. Programming Command Frame

Field	Command	Block	Offset	Last address
Value	40H	Block number[Note]	00H	FFH

Figure 4-18. Internal Verify Command Frame

Field	Command	Block	Offset	Last address
Value	19H	Block number[Note]	00H	FFH

Note The value valid as a block number differs as follows depending on the flash memory size.

<Flash memory size>	<Block number>
1 KB	00H to 03H
2 KB	00H to 07H
4 KB	00H to 0FH
8 KB	00H to 1FH

The block number of the Internal Verify command must be the same as the block number of the Programming command.

4.7.3 Normal termination

To program the flash memory, be sure to execute the Programming and Internal Verify commands in succession.

If command execution is terminated normally, the processing flow between the 78K0S/Kx1+ and programmer is as follows.

<1> The programmer transmits the Programming command to the 78K0S/Kx1+. When it receives ACK, it transmits the first byte of write data.

<2> When the 78K0S/Kx1+ receives the first byte of the write data, it transmits ACK and starts programming the flash memory.

<3> The programmer transmits the second byte of the write data (it can transmits the data even while the 78K0S/Kx1+ is being programmed).

<4> When the 78K0S/Kx1+ has completed writing the first byte and receiving the second byte, it starts writing the second byte.

<5> In this way, writing goes on up to the last address.

<6> When the 78K0S/Kx1+ has received the 256th byte (last data), it transmits ACK twice in a row as follows.

- First ACK: Writing the 255th byte has been completed and the data of the 256th byte has been received.
- Second ACK: Writing the data of the 256th byte has been completed.

<7> The programmer transmits the Internal Verify command when it has received the second ACK.

<8> The 78K0S/Kx1+ transmits ACK and starts internal verification after it has received the Internal Verify command.

<9> When the programmer receives ACK indicating completion of internal verification, the programming processing is completed.

4.7.4 Abnormal termination

Abnormal termination occurs in the following four cases.

- If a parity error occurs when the 78K0S/Kx1+ receives a command from the programmer, the 78K0S/Kx1+ returns NACK. After that, the 78K0S/Kx1+ enters the command wait status.
- If the command transmitted from the programmer is not supported or in an abnormal format, the 78K0S/Kx1+ returns Unknown error. The 78K0S/Kx1+ then enters the command wait status.
- If a write error (status code: 1CH, 1DH, 1EH, or 1FH) occurs while the Programming command is executed, the 78K0S/Kx1+ enters the command wait status. The programmer terminates processing, assuming that a write processing error has occurred.
- If an error is detected in the Internal Verify command, the 78K0S/Kx1+ terminates internal verification processing and returns an error status (MRG 11 error). It then enters the command wait status. The programmer terminates processing, assuming that a write processing error has occurred.

4.7.5 Command flow

Figure 4-19 shows the flow of write processing.

Figure 4-19. Write Processing Flow (1/5)

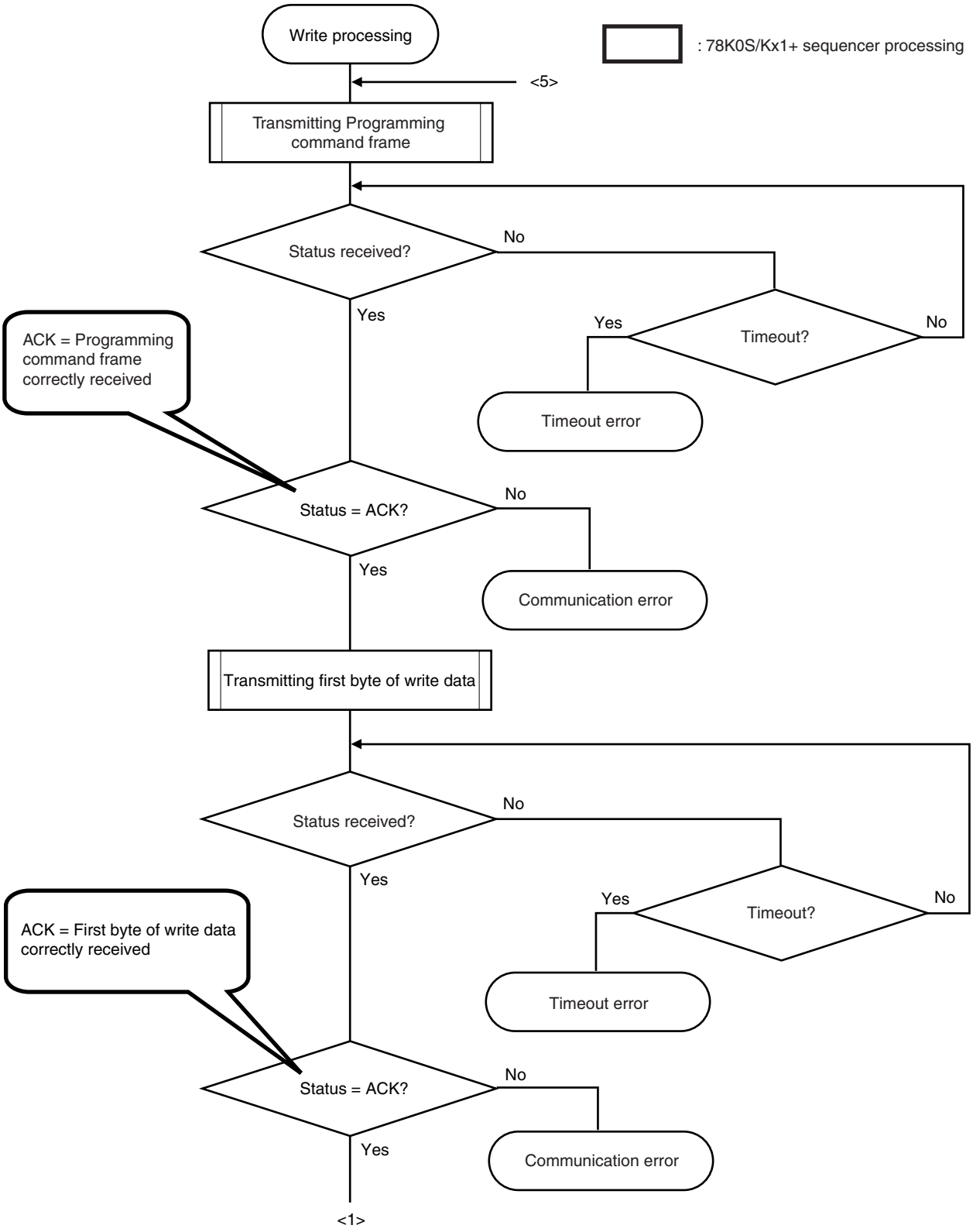


Figure 4-19. Write Processing Flow (2/5)

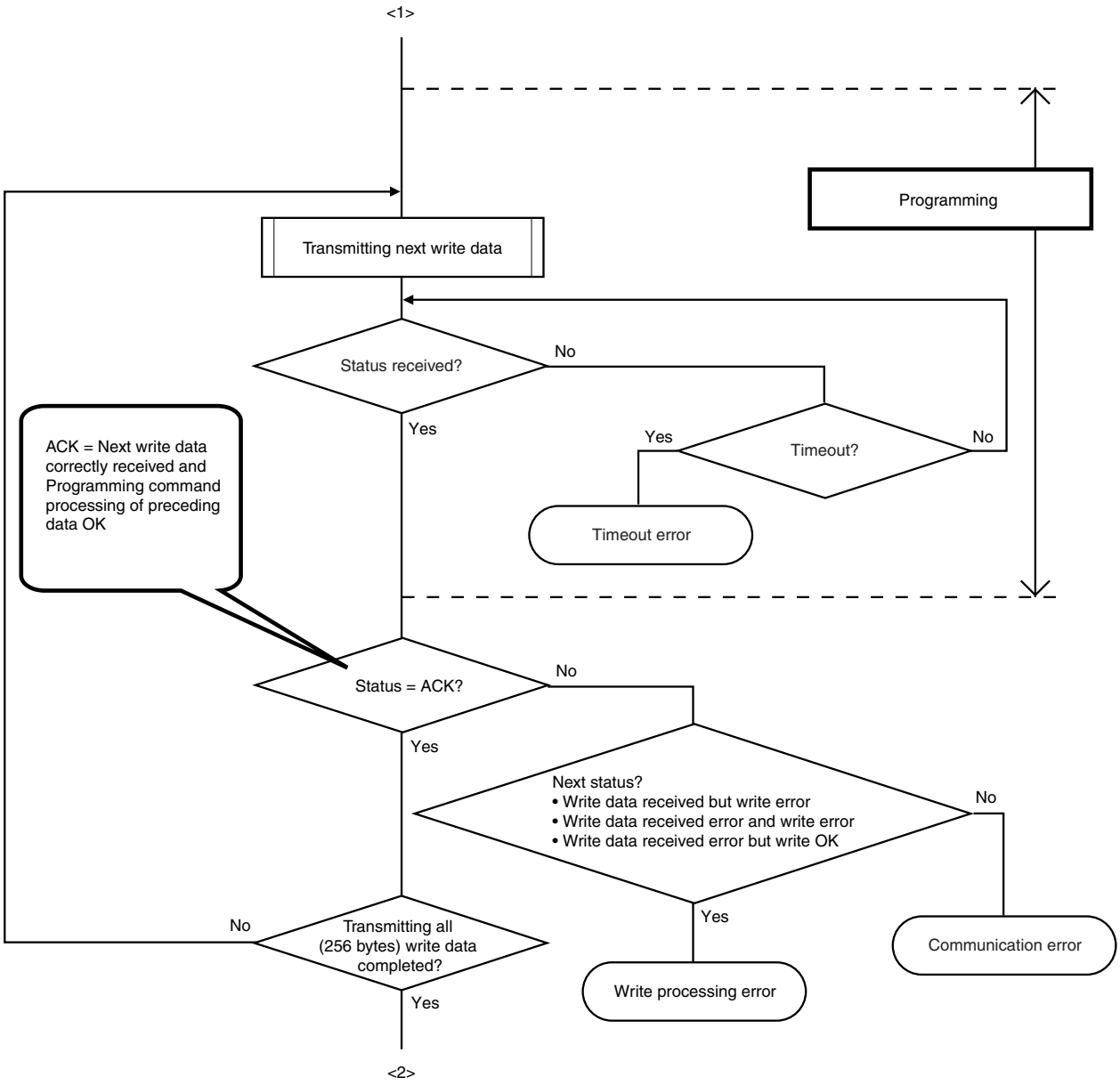


Figure 4-19. Write Processing Flow (3/5)

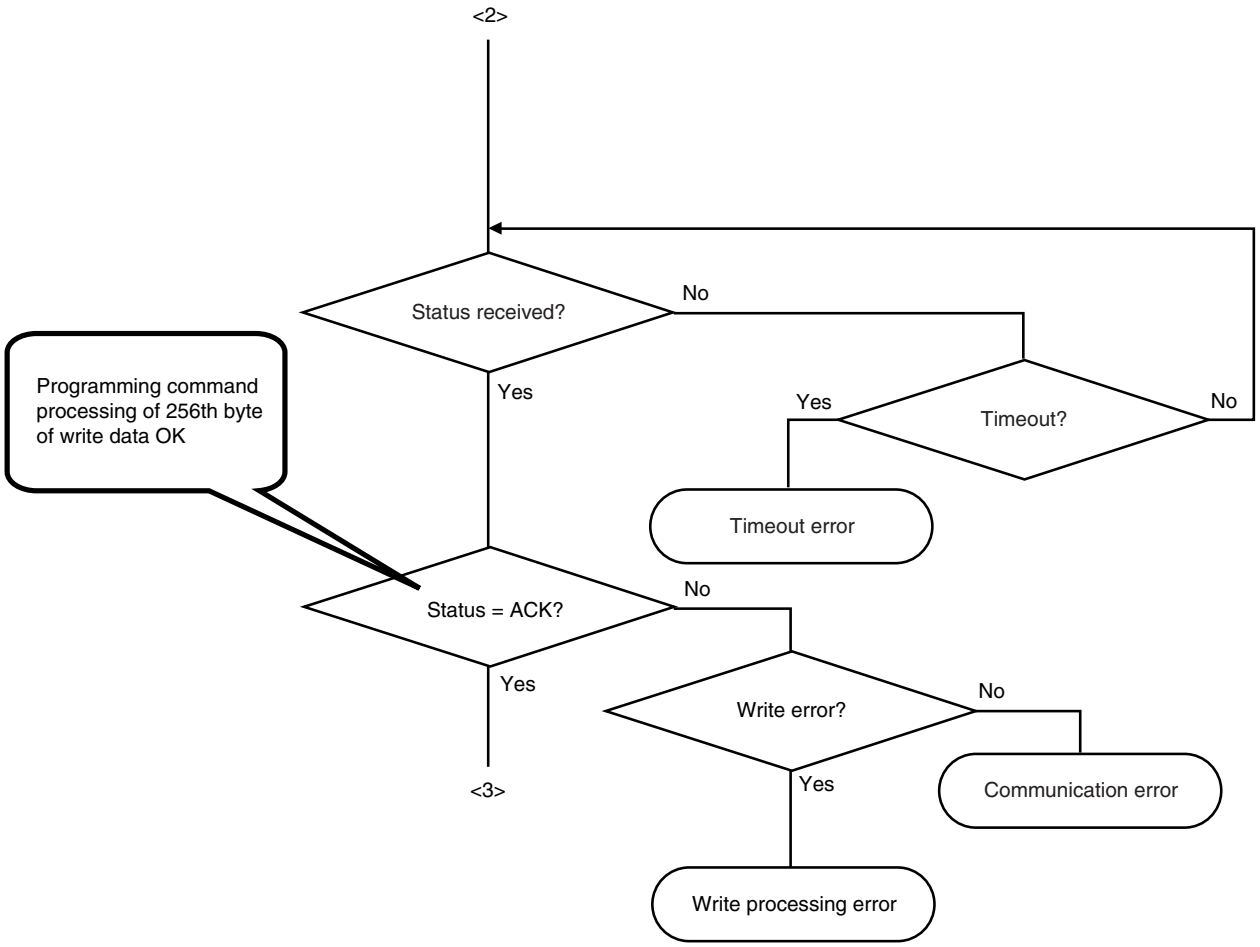


Figure 4-19. Write Processing Flow (4/5)

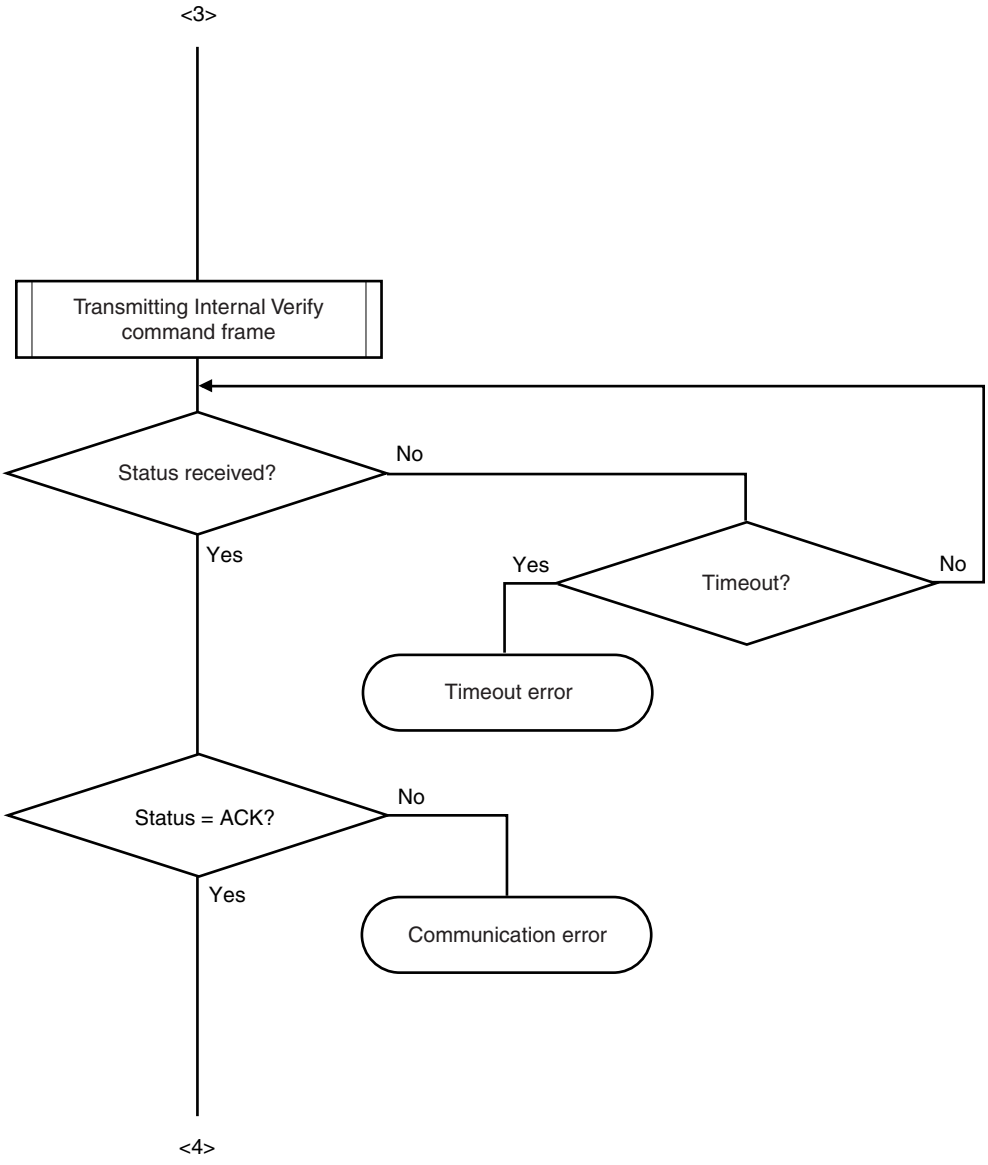
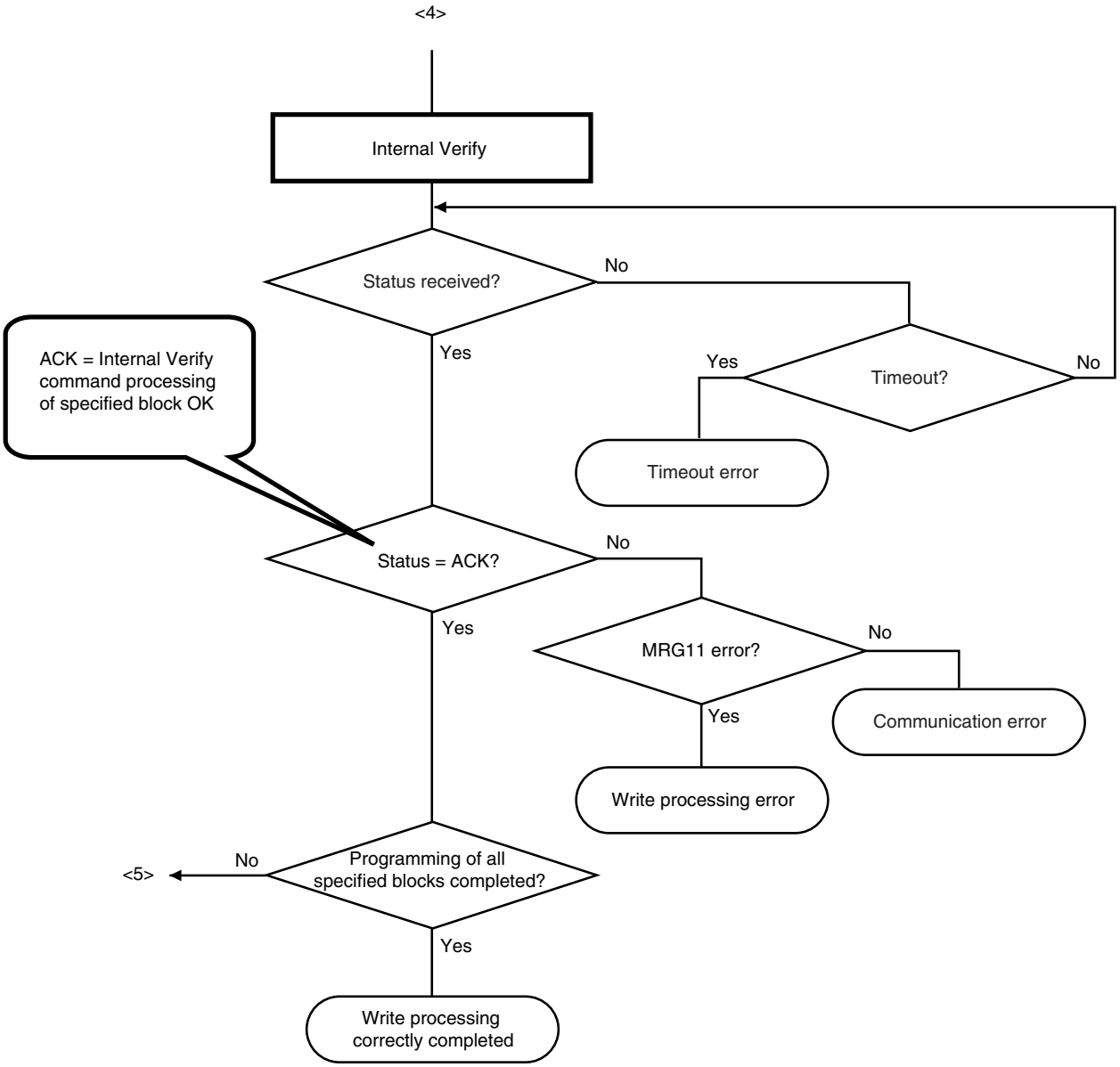


Figure 4-19. Write Processing Flow (5/5)

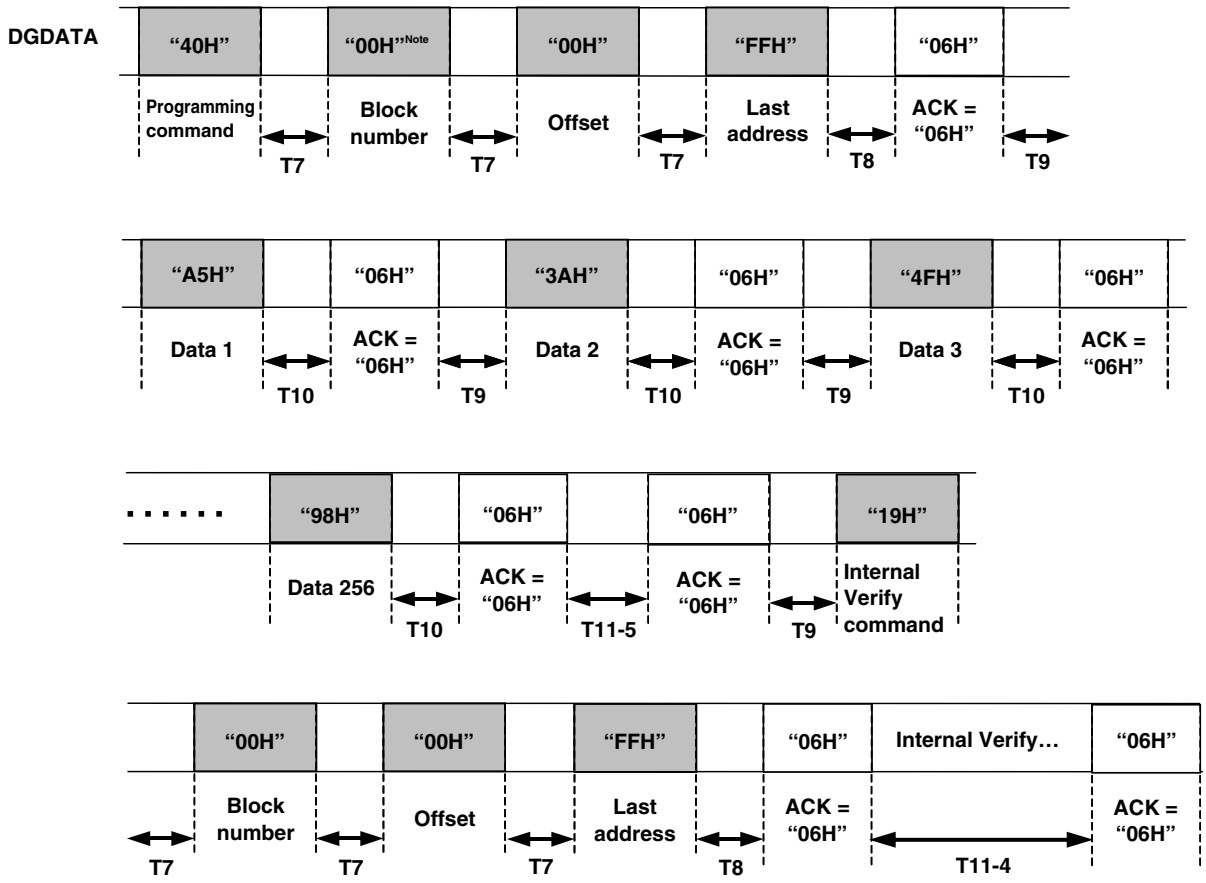


4.7.6 Timing chart

Figure 4-20 shows the timing of write processing.

For the value of Tx in the chart, refer to **CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS**.

Figure 4-20. Timing Chart of Write Processing



Note This is the block number when block 00 is written.

Remark Data 1 to 256 are the data that are written to the flash memory.

4.8 Security Setting Procedure

4.8.1 Description

This processing is to set security flags that protect the data of the flash memory from illegal access by a third party.

There are three types of security flags: write prohibit, block erase prohibit, and chip erase prohibit flags.

To set security flags, execute the Security set and Internal Verify commands in succession.

The set security flags become valid after the flash memory programming mode is cleared and then set again.

4.8.2 Basic command frame

The basic command frames of the two commands executed for security setting processing are as shown in Figures 4-21 and 4-22.

Figure 4-21. Security set Command Frame

Field	Command	Block	Offset	Last address
Value	40H	80H	00H	00H

Figure 4-22. Internal Verify Command Frame

Field	Command	Block	Offset	Last address
Value	19H	80H	00H	00H

Figure 4-23. Security Data (1 Byte Only)

	7	6	5	4	3	2	1	0
Security	1	1	PR5	PR4	PR3	PR2	PR1	PR0

After the Security set command has been executed, security flags are set in accordance with security data, and executing the Programming, Chip Erase, and Block Erase commands is prohibited depending on the set values of the security flags. The security flags are initialized when the chip is erased. Execution of all the commands is enabled again when the security flags have been initialized. If it is set to prohibit erasing the chip, however, neither the security flags nor the flash memory can be initialized. It is recommended to take measures so that the setting of the security flags can be checked before the flags are set.

Each pair of 2 bits of the lower 6 bits of a security data frame control the security function.

If one or both bits of a bit pair are cleared to 0, execution of the corresponding command is disabled. The details of the security data are shown below.

[Bits 5 and 4] Write protection

PR5	PR4	Control
1	1	Enables writing.
1	0	Disables writing.
0	1	
0	0	

[Bits 3 and 2] Chip erasure protection

PR3	PR2	Control
1	1	Enables erasing chip.
1	0	Disables erasing chip.
0	1	
0	0	

[Bits 1 and 0] Block erasure protection

PR1	PR0	Control
1	1	Enables erasing block.
1	0	Disables erasing block.
0	1	
0	0	

Each item of security setting and whether commands can be executed with given setting are shown below.

Operation Mode	Flash Memory Programming Mode			Self Programming Mode
Command / Item of security setting	Command operation after security setting √: Executable ×: Not executable			• All commands are executable regardless of security setting. • Only security set value can be held.
	Programming	Chip Erase	Block Erase	
Write prohibition	×	√	×	
Chip erase prohibition	√	×	×	
Block erase prohibition	√	√	×	

4.8.3 Normal termination

The flow is the same as that of write processing.

To execute security flag setting, be sure to execute the Security set and Internal Verify commands in succession.

If command execution is terminated normally, the processing flow between the 78K0S/Kx1+ and programmer is as follows.

<1> The programmer transmits the Security set command. After it has received ACK, it transmits security data (1 byte).

<2> The 78K0S/Kx1+ transmits ACK twice in a row as follows after it has received the security data (1 byte).
- First ACK: Security data has been received.
- Second ACK: Writing security data has been completed.

<3> The programmer transmits the Internal Verify command after it has received ACK twice.

<4> The 78K0S/Kx1+ receives the command, transmits ACK, and starts internal verification.

<5> The programmer receives ACK that indicates completion of the internal verification. This completes the security setting processing.

4.8.4 Abnormal termination

If the write processing is not completed correctly, use the Chip Erase command.

The security flags cannot be re-set (changing addition or setting) once they have been set. If such an attempt is made, a Write error (1CH) occurs.

Abnormal termination occurs in the following four cases (in the same manner as when the Programming command is executed).

- If a parity error occurs when the 78K0S/Kx1+ receives a command from the programmer, the 78K0S/Kx1+ returns NACK. After that, the 78K0S/Kx1+ enters the command wait status.
- If the command transmitted from the programmer is not supported or in an abnormal format, the 78K0S/Kx1+ returns Unknown error. The 78K0S/Kx1+ then enters the command wait status.
- If a write error (status code: 1CH, 1DH, 1EH, or 1FH) occurs while the Security set command is executed, the 78K0S/Kx1+ enters the command wait status. The programmer terminates processing, assuming that a write processing error has occurred.
- If an error is detected in the Internal Verify command, the 78K0S/Kx1+ terminates internal verification processing and returns an error status (MRG 11 error). It then enters the command wait status. The programmer terminates processing, assuming that a security setting processing error has occurred.

Caution If the security setting processing is not completed correctly, execute the Chip Erase command before resetting or turning off the power to the device.

4.8.5 Command flow

Figure 4-24 shows the flow of security setting processing.

Figure 4-24. Security Setting Processing Flow (1/3)

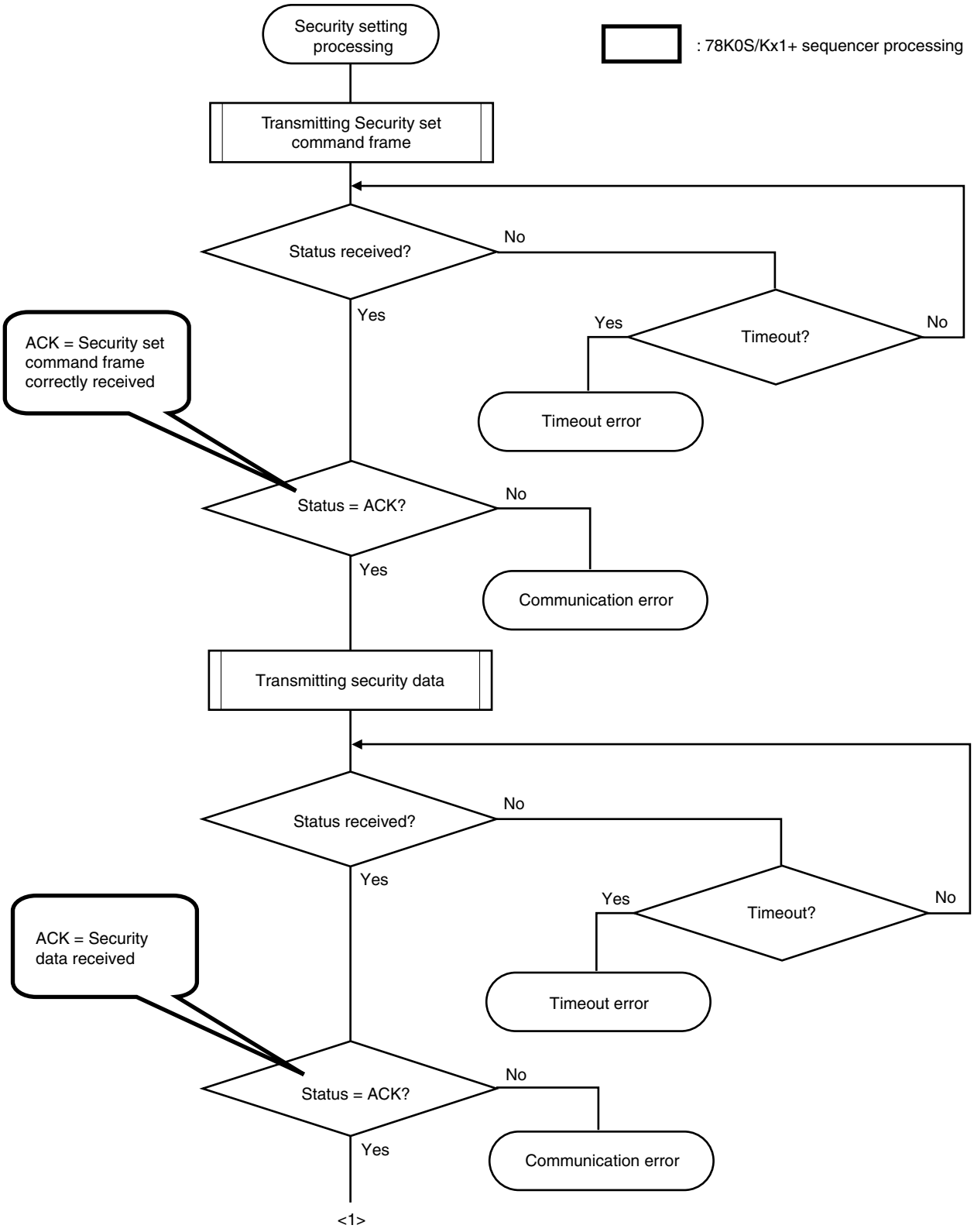


Figure 4-24. Security Setting Processing Flow (2/3)

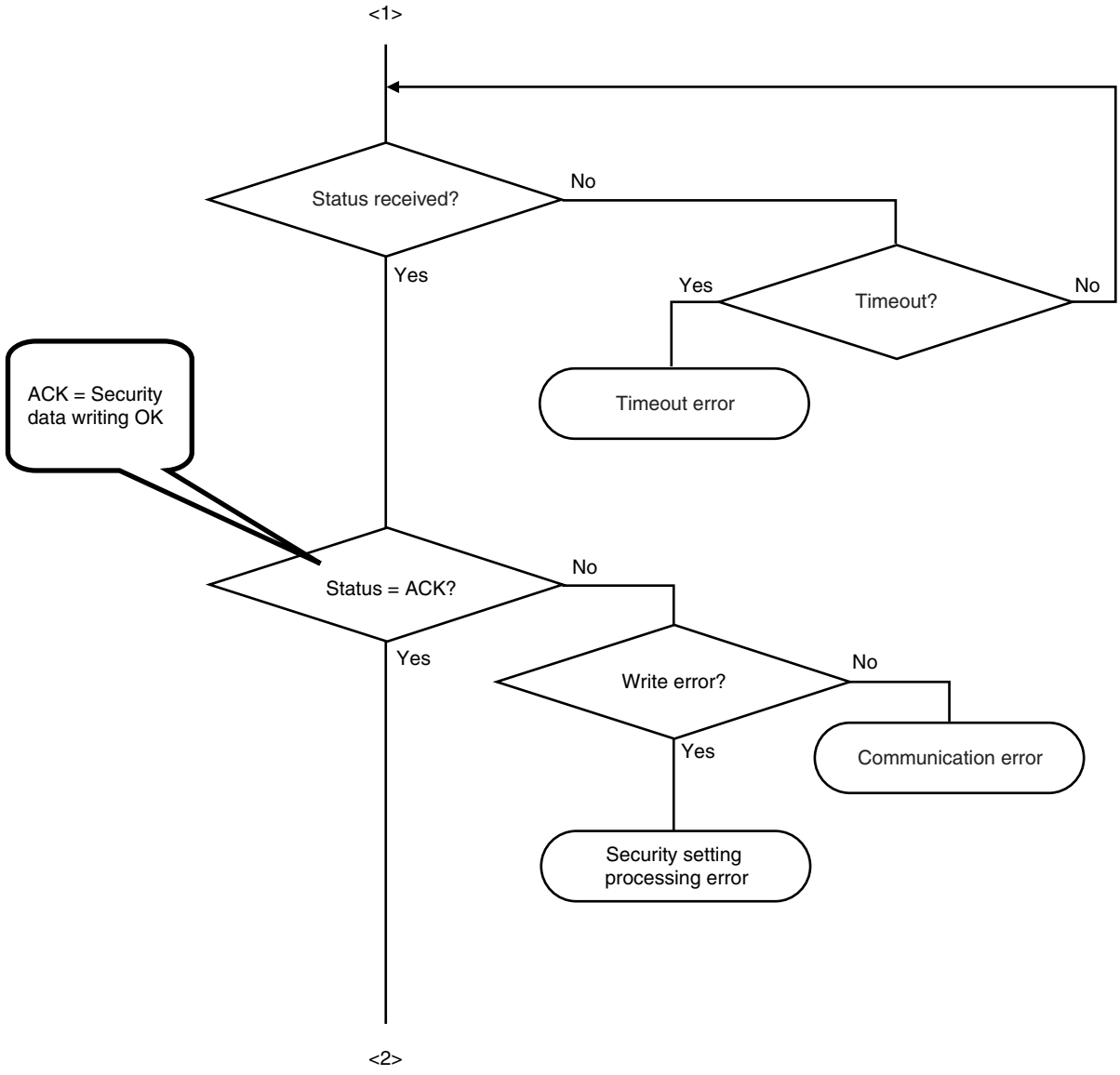
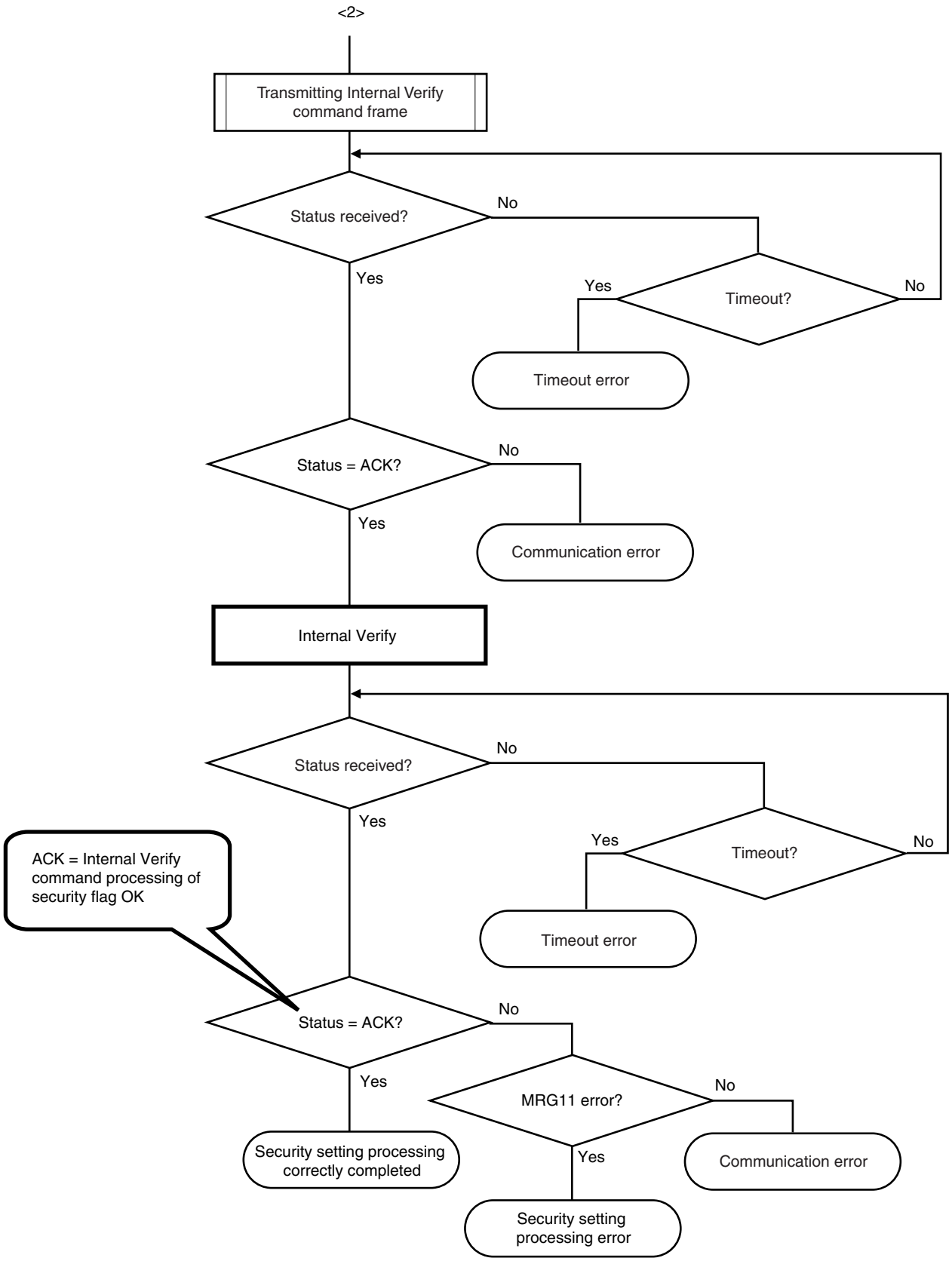


Figure 4-24. Security Setting Processing Flow (3/3)

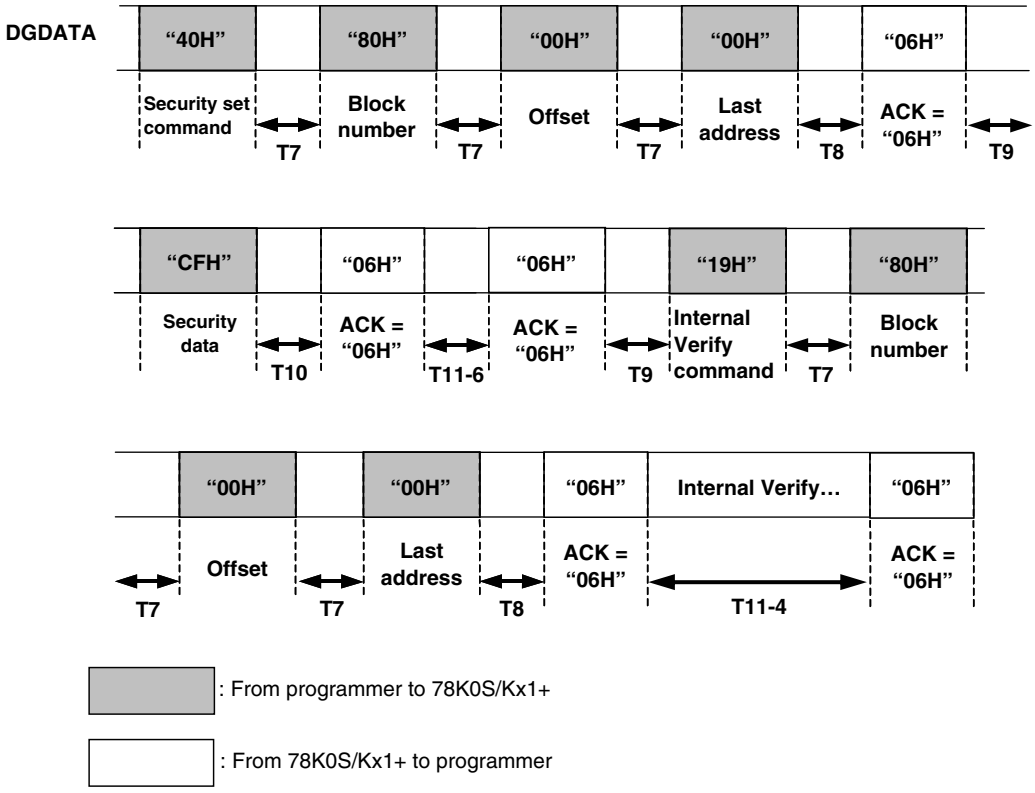


4.8.6 Timing chart

Figure 4-25 shows the timing of security setting processing.

For the value of Tx in the chart, refer to **CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS**.

Figure 4-25. Timing Chart of Security Setting Processing



Remark For the security data, refer to **4.8.2 Basic command frame**.

4.9 Checksum Processing

4.9.1 Description

This processing is to receive the checksum data of an area from block 0 to a specified block.

As a checksum value, the lower 2 bytes of an operation result are transmitted from the 78K0S/Kx1+ in the order of lower byte, then higher byte.

4.9.2 Basic command frame

The basic command frame of the command executed for checksum processing is as shown in Figure 4-26.

Figure 4-26. Checksum Command Frame

Field	Command	Block	Offset	Last address
Value	B0H	Block number[Note]	00H	FFH

Note The value valid as a block number differs as follows depending on the flash memory size.

<Flash memory size>	<Block number>
1 KB	00H to 03H
2 KB	00H to 07H
4 KB	00H to 0FH
8 KB	00H to 1FH

4.9.3 Normal termination

Checksum data of the lower 2 bytes of an operation result is received. The lower byte and the higher byte of the checksum data are received in that order.

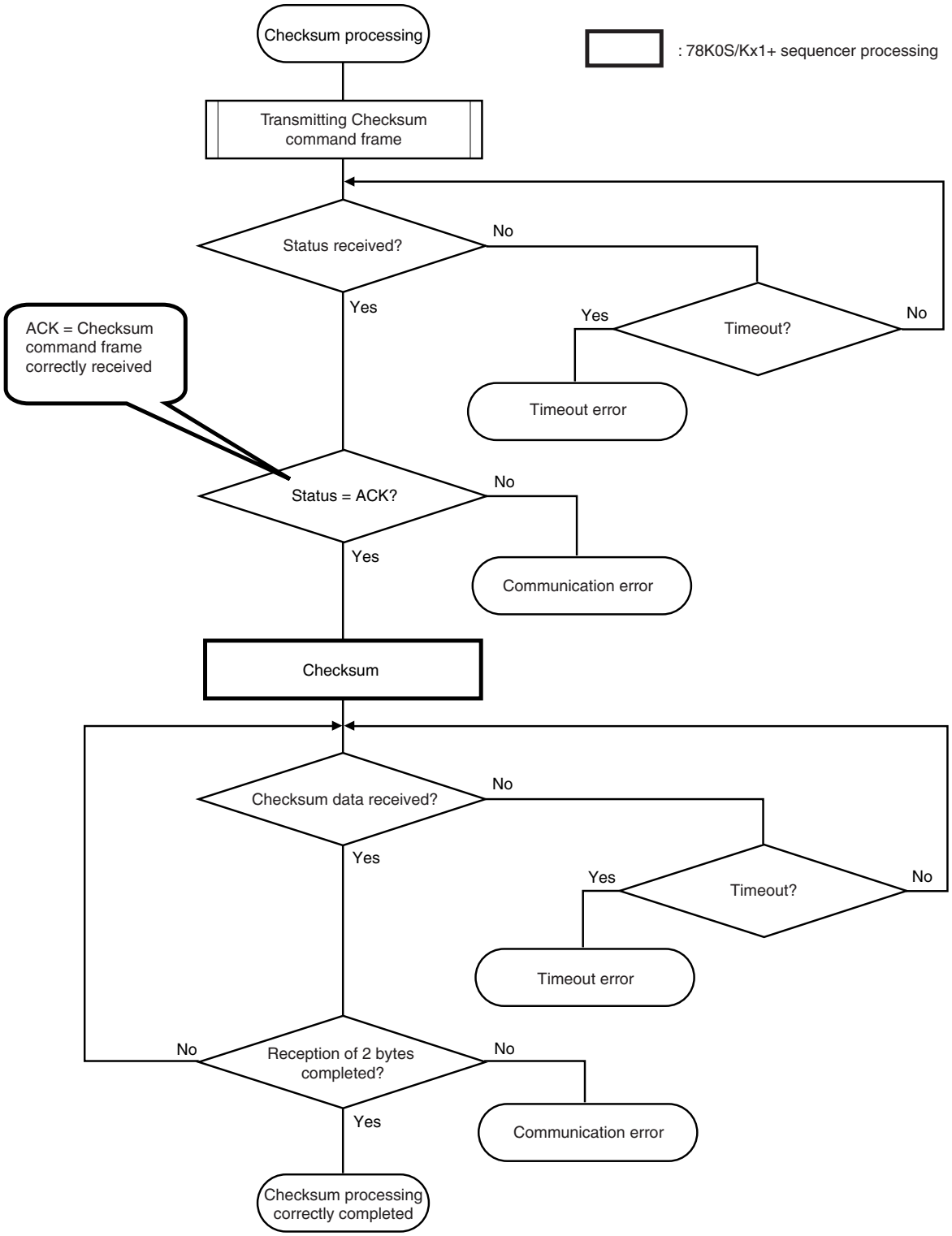
4.9.4 Abnormal termination

If a parity error occurs, NACK is returned, and checksum processing is terminated.

4.9.5 Command flow

Figure 4-27 shows the flow of checksum processing.

Figure 4-27. Checksum Flow Processing

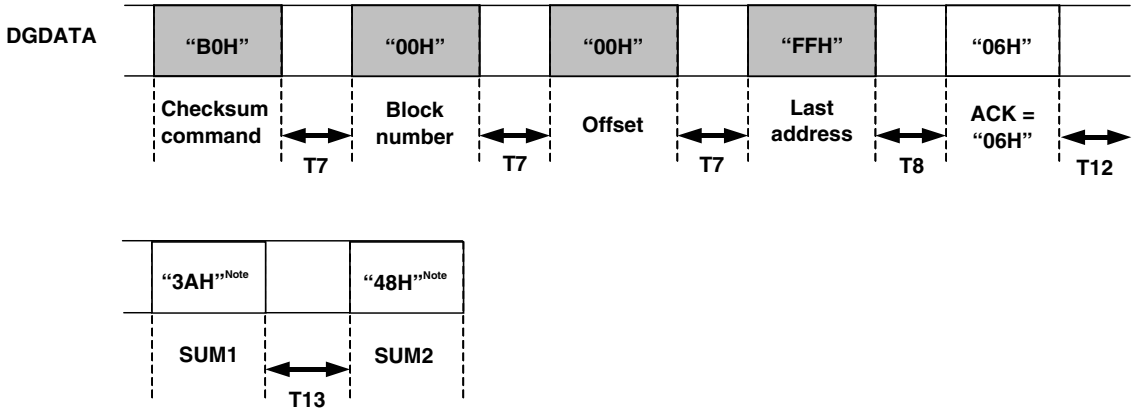


4.9.6 Timing chart

Figure 4-28 shows the timing of checksum processing.

For the value of Tx in the chart, refer to **CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS**.

Figure 4-28. Timing Chart of Checksum Processing



Note Checksum value 483AH is the data of SUM1 and SUM2.

Remark SUM1 is the lower byte of the checksum value.
SUM2 is the higher byte of the checksum value.

4.9.7 Checksum algorithm

Figure 4-29 shows the algorithm of the checksum processing.

Figure 4-29. Algorithm of Checksum Processing

```
#define BLOCKSIZ  256

/* ROM data of one block must be stored. */
unsigned char          rom_data [BLOCKSIZ];

unsigned char
bist_calc()
{
        int    i;
        unsigned short bist, bist_temp;

        bist = 0;
        for(i = 0; i < BLOCKSIZ; i++){
                bist_temp = bist & 0x1;
                bist_temp = (bist_temp << 8) | (bist_temp << 9) | (bist_temp << 11) | (bist_temp << 12);
                bist = (bist >> 1) ^ rom_data[i] ^ bist_temp;
        }
        return((unsigned char)bist);
}
```

CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS

This chapter describes the parameter characteristics between the programmer and the 78K0S/Kx1+ in the flash memory programming mode.

Be sure to refer to the user's manual of the 78K0S/Kx1+ for electrical specifications when designing a programmer.

Parameter Characteristics 1 (T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Frequency tolerance	ΔF	DGCLK frequency tolerance	–1		1	%
Baud rate	–	DGCLK = 8 MHz		115.2		kbps
Optional baud rate (When resonator is mounted on target system)	–	DGCLK = 10 MHz		144.0		kbps
	–	DGCLK = 9 MHz		129.6		kbps
	–	DGCLK = 6 MHz		86.4		kbps

Parameter Characteristics 2 (T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbol	MIN.	TYP.	MAX.	Unit
Initial setting time		T0	10			ms
Minimum low width for mode setting		T1	1			μs
Setup time of DGCLK to DGDATA for mode setting		T2	1			μs
Minimum high width for mode setting		T3	1			μs
Setup time of DGDATA to $\overline{\text{RESET}}$↑ for mode setting		T4	1			μs
$\overline{\text{RESET}}$↑ to DGCLK active		T5	2			ms
Command setup		T6	2			μs
Command data interval		T7	20			μs
Command to status interval[Note 1]		T8			6	μs
Status to command/data interval		T9	1			μs
Data to status interval[Note 1]		T10			150	μs
ACK to status interval	Chip/Block Erase command[Note 2]	T11-1			10	ms
	Chip Erase Verify command[Note 2]	T11-2			16	ms
	Block Erase Verify command[Note 2]	T11-3			500	μs
	Internal Verify command[Note 2]	T11-4			6	ms
	Programming command[Note 2] (After last (256th byte) write data is transmitted)	T11-5			150	μs
	Security command[Note 2] (After security data is transmitted)	T11-6			150	μs
ACK to checksum 1st byte (Checksum command)[Note 3]	Checksum area up to 4 KB	T12-1			4	ms
	Checksum area up to 8 KB	T12-2			8	ms
Checksum 1st byte to checksum 2nd byte (Checksum command)[Note 4]		T13			2	μs

(Descriptions for Notes 1 to 4 and a Remark are provided on the next page.)

Notes 1. The maximum time required after the 78K0S/Kx1+ receives a command frame or data from the programmer until it transmits status data. The programmer needs to continue the status receive processing up to this maximum time.

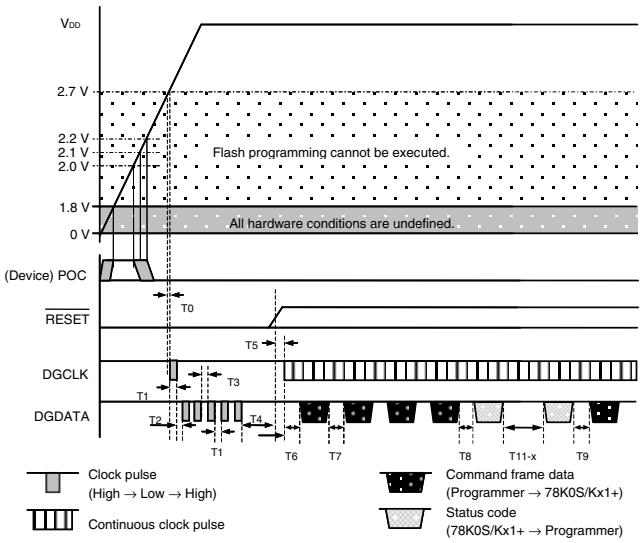
2. The maximum time required after the 78K0S/Kx1+ transmits ACK for a command frame reception or a data reception from the programmer, until it transmits ACK for the command processing completion. The programmer needs to continue the status receive processing up to this maximum time.

3. The maximum time required after the 78K0S/Kx1+ receives a command frame from the programmer until it transmits the first byte of the checksum data. The programmer needs to continue the status receive processing up to this maximum time.

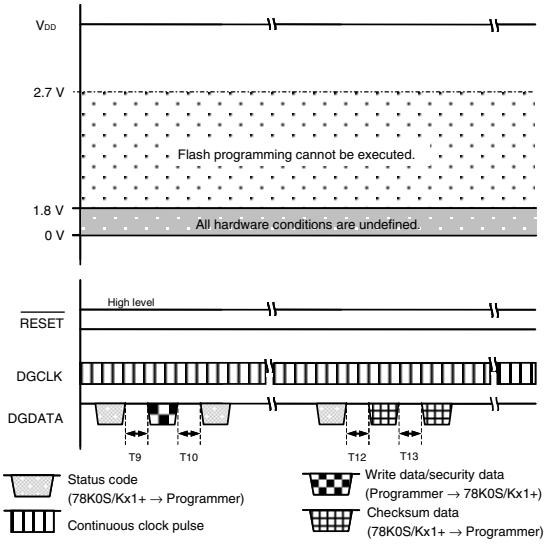
4. The maximum time required after the 78K0S/Kx1+ transmits the first byte of the checksum data until it transmits the second byte of the checksum data. The programmer needs to continue the data receive processing up to this maximum time.

Remark The item names in the “ACK to status interval” are related to each command name that is issued from the programmer to the 78K0S/Kx1+.

When Mode Is Set and Command Is Executed



When Command Is Executed



APPENDIX REVISION HISTORY

A.1 Major Revisions in This Edition

Page	Description
p. 10	Addition of 78K0S/KU1+ in **Table 1-1. Flash Memory Size of 78K0S/Kx1+**
p. 19	Modification of **Figure 4-1. General Command Flow for Rewriting**
p. 22	Modification to description in **4.3.1 Description**
p. 22	Deletion of **Figure 4-3. Block Erase Verify Command Frame**
p. 22	Modification to and deletion of description in **4.3.3 Normal termination**
p. 23	Modification to description and deletion of Caution in **4.3.4 Abnormal termination**
p. 24	Modification of **Figure 4-3. Chip Blank Check Processing Flow** and deletion of an illustration of (2/2) in that
p. 25	Modification of **Figure 4-4. Timing Chart of Chip Blank Check Processing**
p. 62 in previous edition	Deletion of **CHAPTER 6 ELECTRICAL SPECIFICATIONS (REFERENCE)**

A.2 Revision History of Previous Editions

A history of the revisions up to this edition is shown below. “Applied to:” indicates the chapters to which the revision was applied.

Edition	Description	Applied to:
2nd	Modifications to **Figure 3-2 Timing of Changing Mode to Flash Memory Programming Mode (When Mode Is Set and Command Is Executed)** and **Figure 3-3 Timing of Changing Mode to Flash Memory Programming Mode (When Command Is Executed)**	CHAPTER 3 SETTING FLASH MEMORY PROGRAMMING MODE
	Change of “T11” to “T11-5” in **Figure 4-21 Timing Chart of Write Processing**	CHAPTER 4 COMMAND SPECIFICATIONS
	Change of symbol names in **Figure 4-26 Timing Chart of Security Setting Processing**	
	Change of symbol names in **Figure 4-29 Timing Chart of Checksum Processing**	
	CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS • Addition of **Parameter Characteristics 1** table, and modification of **Parameter Characteristics 2** table • Modification of DGDATA timing charts	CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS
3rd	Modification to description in **2.1 Communication Settings** and to the title of **Table 2-2**.	CHAPTER 2 COMMUNICATION PROTOCOL
	Change of the position of Checksum processing in **Figure 4-1 General Command Flow for Rewriting**	CHAPTER 4 COMMAND SPECIFICATIONS
	Modification to command number of Security set in **Table 4-1 Command List**	
	Modification to last address values in **Figure 4-26 Timing Chart of Security Setting Processing**	
	CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS • Change of “Optional baud rate” parameter in **Parameter Characteristics 1** • Change of maximum value of T8 in **Parameter Characteristics 2** • Modification to T12 description according to the Checksum area divided by 2 in **Parameter Characteristics 2**	CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS

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