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April 1st, 2010
Renesas Electronics Corporation

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7548/7549 Group

Serial I/O (Clock Synchronous Serial I/O Mode: Example 2)

1. Abstract

The following article introduces and shows an example of how to use the serial I/O (Clock Synchronous Serial I/O Mode: Example 2) on the 7548/7549 Group device.

2. Introduction

The application explained in this document applies to the following MCU and parameter(s):
Applicable MCU: 7548/7549 Group
Oscillation frequency: 4 MHz

Function set ROM data 0 to 2 are areas used to set peripheral functions by data written to the QzROM and can not be set by program. Data set to these areas are valid after a reset of the MCU is released. Make sure to set values according to the user system regardless of the use of peripheral functions. Set values used in this sample program are as follows.

Function set ROM data 0 FSROM0 (address FFD8h): 10000000b
Function set ROM data 1 FSROM1 (address FFD9h): 10000001b
Function set ROM data 2 FSROM2 (address FFDAh): 00001011b

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

3. Contents

3.1 Cyclic Transmission or Reception of Block Data (Data of Specified Number of Bytes) Between Two Microcomputers

Outline: When the clock synchronous serial I/O is used for communication, the synchronization of the clock and data between the transmit side and the receive side may be shifted because of noise included in the synchronous clock. Normal operations are performed constantly by using “heading adjustment” to correct the shift. The “heading adjustment” is carried out by using the interval between blocks in this application example.

Specifications:

- Serial I/O (clock synchronous serial I/O mode) is used.
- Synchronous clock frequency: 125 kHz (f(XIN) = 4 MHz divided by 32)
- Byte cycle: 500 µs
- Number of transmit bytes: 8 bytes/block
- Block transfer cycle: 16 ms
- Block transfer term: 4 ms
- Interval between blocks: 12 ms
- Heading adjustment time: 8 ms

  Master control
- Data is transmitted and received by interrupt routine executed every byte cycle (500 µs)

  Slave control
- Data is transmitted and received by serial I/O receive interrupt routine
- The heading adjustment is carried out by interrupt routine executed every 1ms

Limitations of specifications:

- Reading the receive data and writing the next transmit data must be completed within the time obtained from the calculation formula “byte cycle - 1 byte transfer time”.

  Note: The time taken from generating this serial I/O receive interrupt to inputting the next synchronous clock must be 436 µs.
- “Heading adjustment time < interval between blocks” must be satisfied.

Figure 3.1 shows the Connection Diagram.

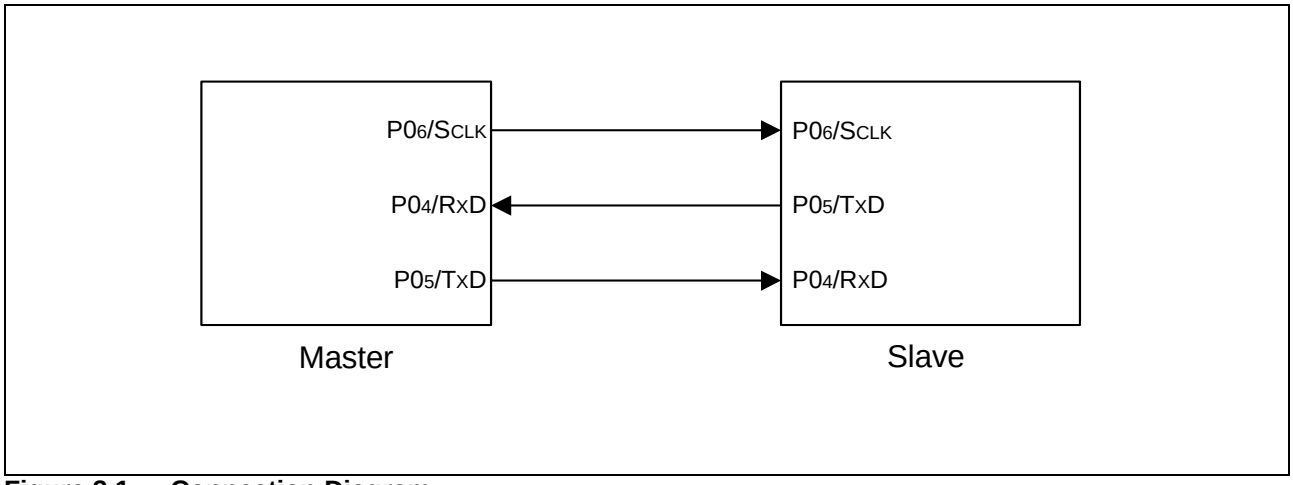

Figure 3.1 Connection Diagram

Figure 3.2 shows the Timing Chart. In the slave, when a synchronous clock is not input within a predetermined amount of time (heading adjustment time), the next clock input is processed as the beginning (heading) of a block. When a clock is input again after one block (8 bytes) is received, the clock is ignored.
Figure 3.3 shows the Relevant Register Settings.

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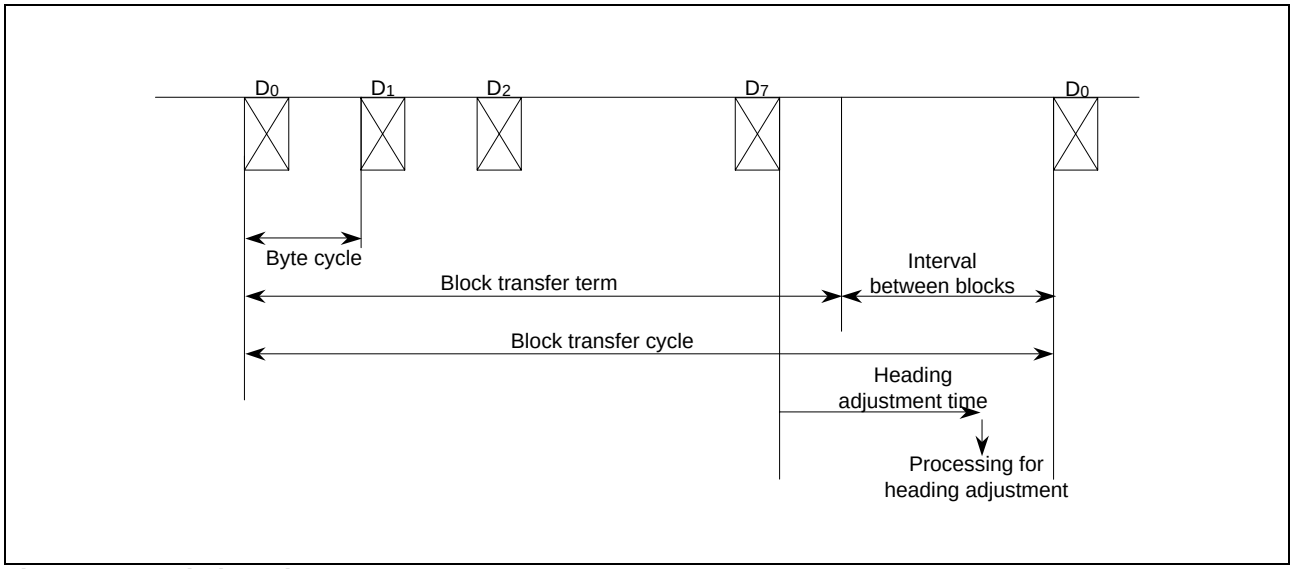
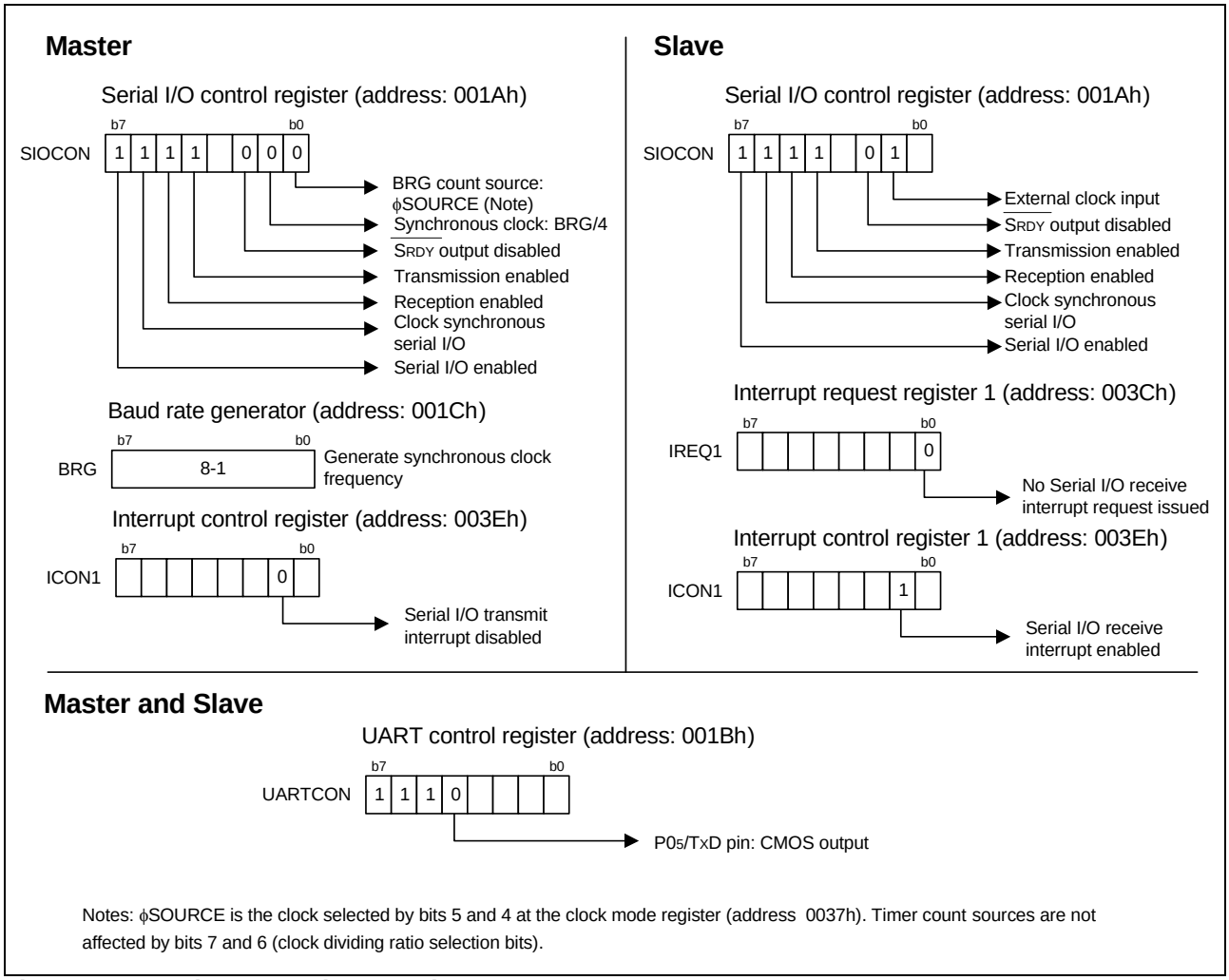


Figure 3.2 Timing Chart



Notes: φSOURCE is the clock selected by bits 5 and 4 at the clock mode register (address 0037h). Timer count sources are not affected by bits 7 and 6 (clock dividing ratio selection bits).

Figure 3.3 Relevant Register Settings

Control by software:

• Master Control

The master starts transmission or reception by writing transmit data to the transmit buffer register in the interrupt routine executed every 500 µs. In this interrupt routine, the receive data is read and then the next transmit data is written to the transmit buffer register. Additionally, the master controls one block (8 bytes) transmission and reception and generates block intervals.

Figure 3.4 shows the Master Control Procedure.

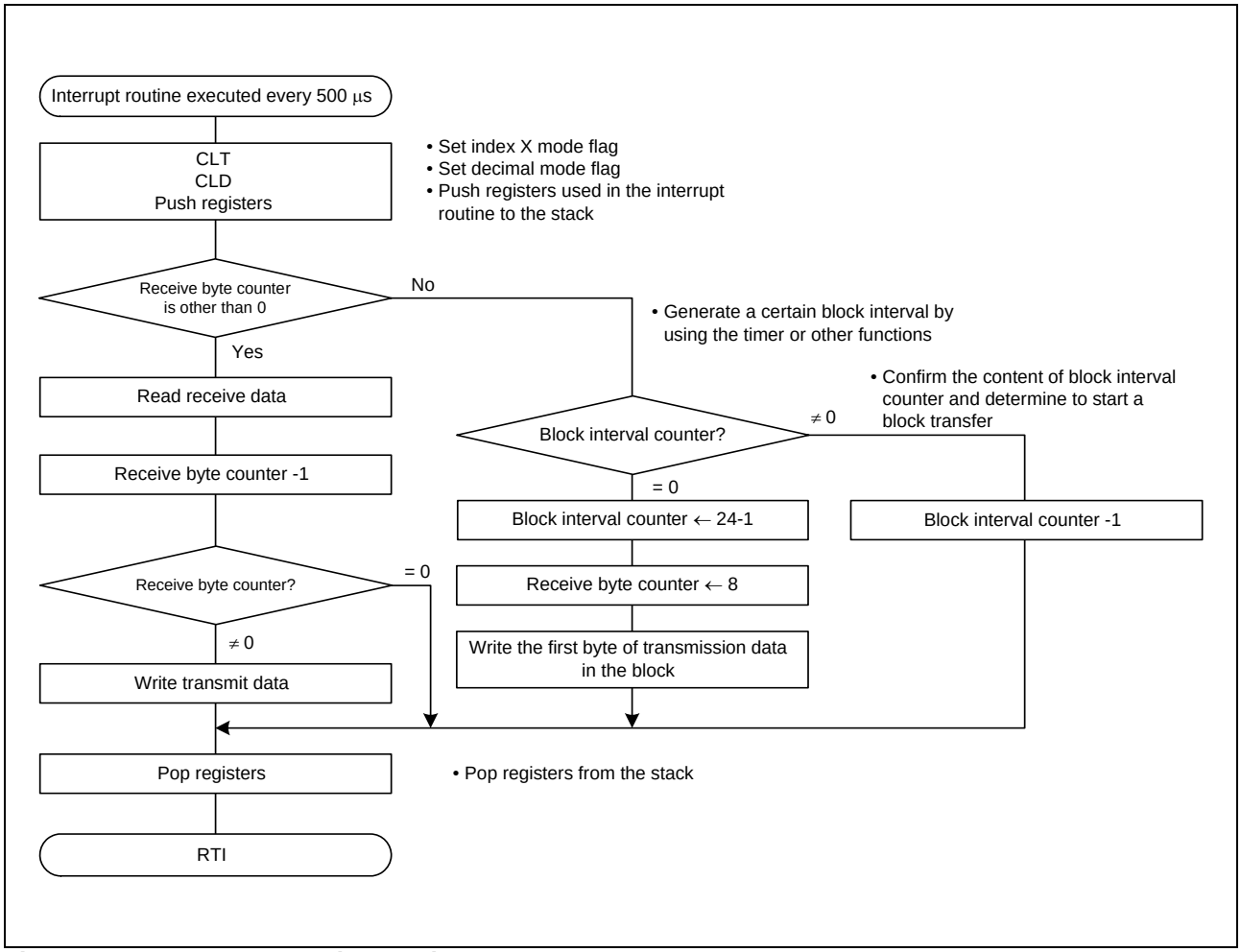


Figure 3.4 Master Control Procedure

Control by software:

• Slave control

After setting the relevant registers as shown in figure 3.3, the slave will be able to receive a synchronous clock at any time, and the serial I/O receive interrupt request occurs each time an 8-bit data is received. In the serial I/O receive interrupt routine, the data to be transmitted next is written to the transmit buffer register after the receive data is read out. However, if no serial I/O receive interrupt request occurs after a predetermined amount of time (heading adjustment time), the following processing will be performed in the interrupt routine executed every 1ms.

1. Serial I/O is initialized.
2. The first byte of the transmission data in the block is written into the transmit buffer register.
3. The receive byte counter is initialized in order to process the next receive data as the first byte of receive data in the block.

Figure 3.5 shows the Slave Control Procedure.

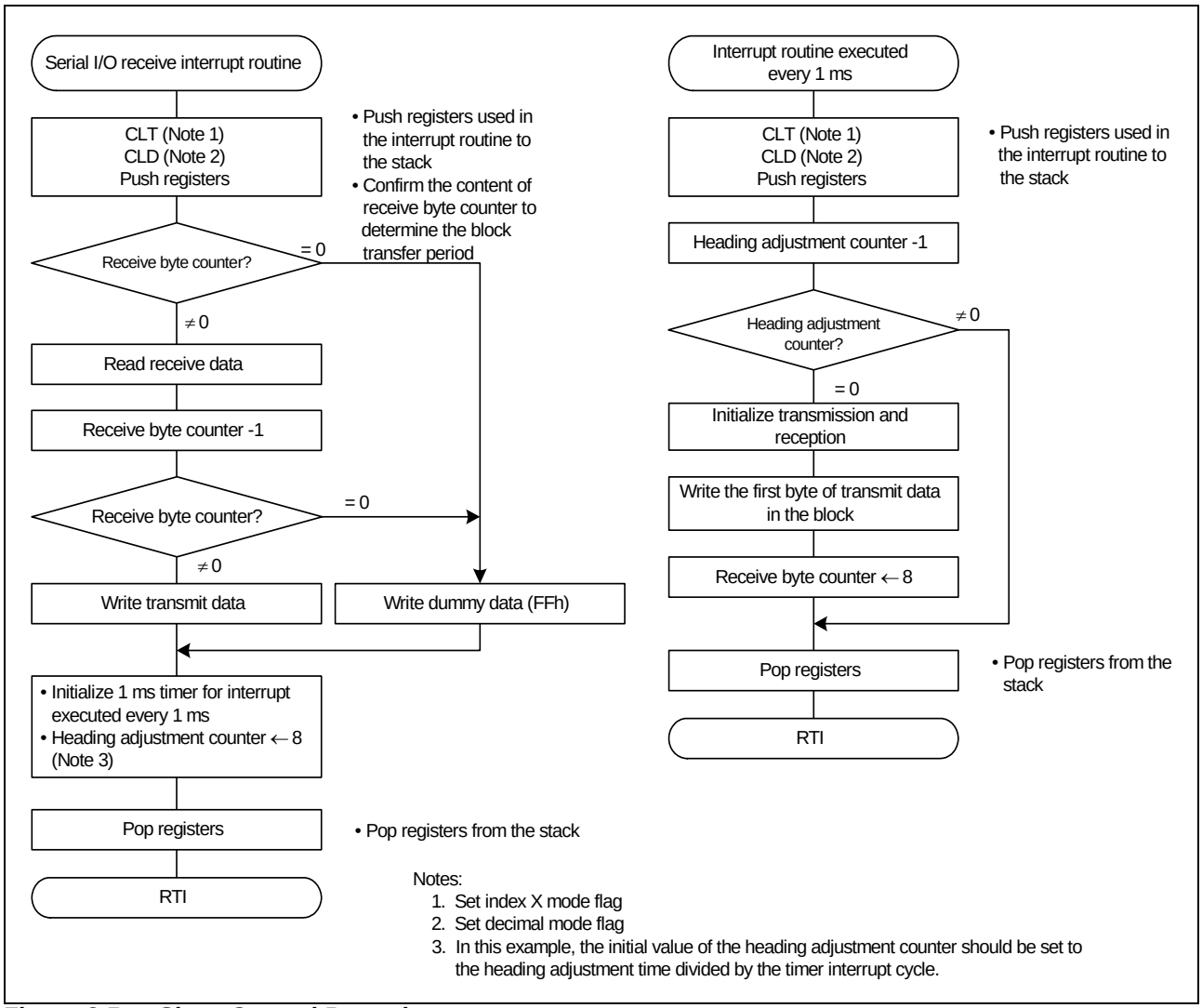


Figure 3.5 Slave Control Procedure

4. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click “Application Notes” in the left side menu on the page of the 7548/7549 Group.

5. Reference Document

Datasheet
7548/7549 Group Datasheet
Download the latest version from the Renesas Technology website.

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REVISION HISTORY	7548/7549 Group Serial I/O (Clock Synchronous Serial I/O Mode: Example 2)

Rev.	Date	Description	
		Page	Summary
1.00	Mar 26, 2007	–	First Edition issued
1.01	Oct 01, 2007	2	Section 3.1, clerical errors revised

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