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Renesas Electronics Corporation

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7544 Group

Timer A Operation (Pulse Width HL Continuously Measurement Mode)

1. Abstract

The following article introduces and shows an application example of pulse width HL continuously measurement mode of timer A.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: 7544 Group

3. Contents

Outline: An input signal is detected by using the pulse width HL continuously measurement mode.

Specifications: Whether a normal-range signal is input or not is judged by measuring a pulse width input from the $P0_0$/$CNTR_1$ pin.
$f(X_{IN})/16$ ($f(X_{IN})$ = 6.4 MHz) is used as the count source, and "H" and "L" pulse width of the input pulse are measured by using the pulse width HL continuously measurement mode. When the following conditions are satisfied, it is recognized as a normal value. When the following conditions are not satisfied, it is recognized as an unusual value.
200 ms ≤ "H" pulse width < 1.2 s
600 ms ≤ "L" pulse width of < 2.2 s
1.0 s ≤ one period ("H" pulse width + "L" pulse width) < 3.0 s
Operation clock: $f(X_{IN})$ = 6.4 MHz, high-speed mode

3.1 Example of Peripheral Circuit

Figure 1 shows an example of a peripheral circuit.

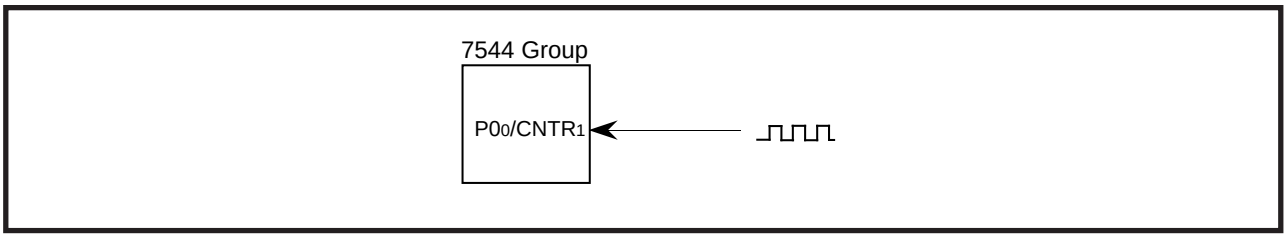

Figure 1 Example of peripheral circuit

3.2 Operation Timing When Pulse is Input

Figure 2 shows an operation timing when a pulse is input.

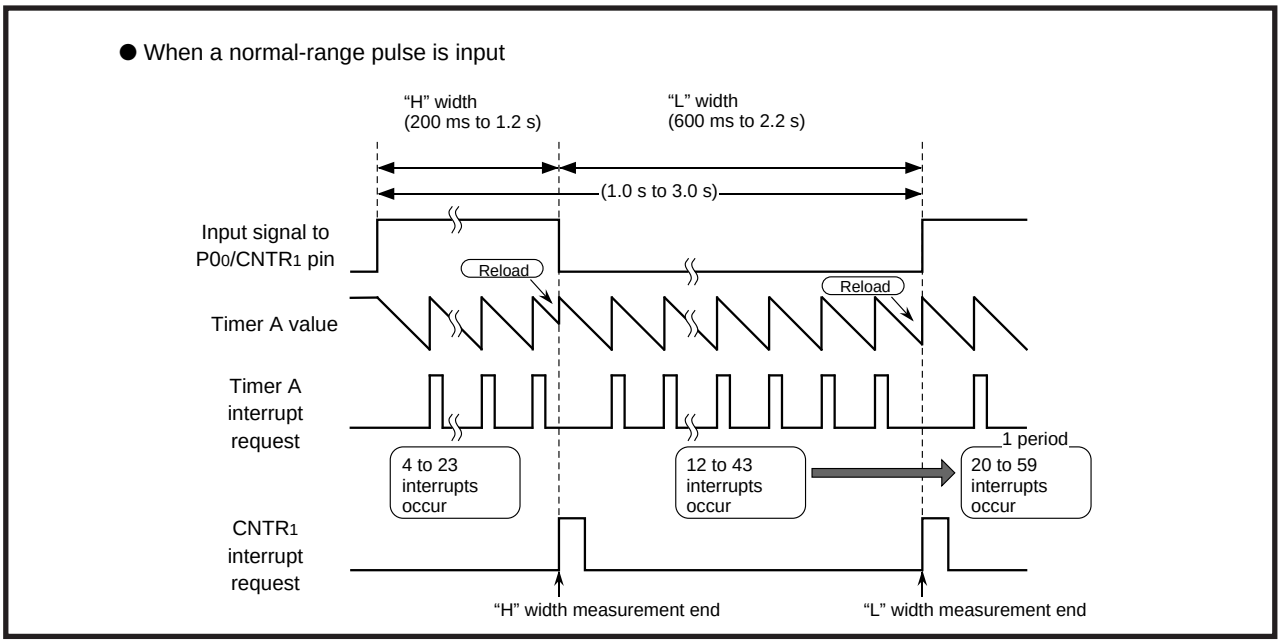

Figure 2 Operation timing when pulse is input

3.3 Example of Control Procedure

Figure 3 and Figure 4 show an example of control procedure.

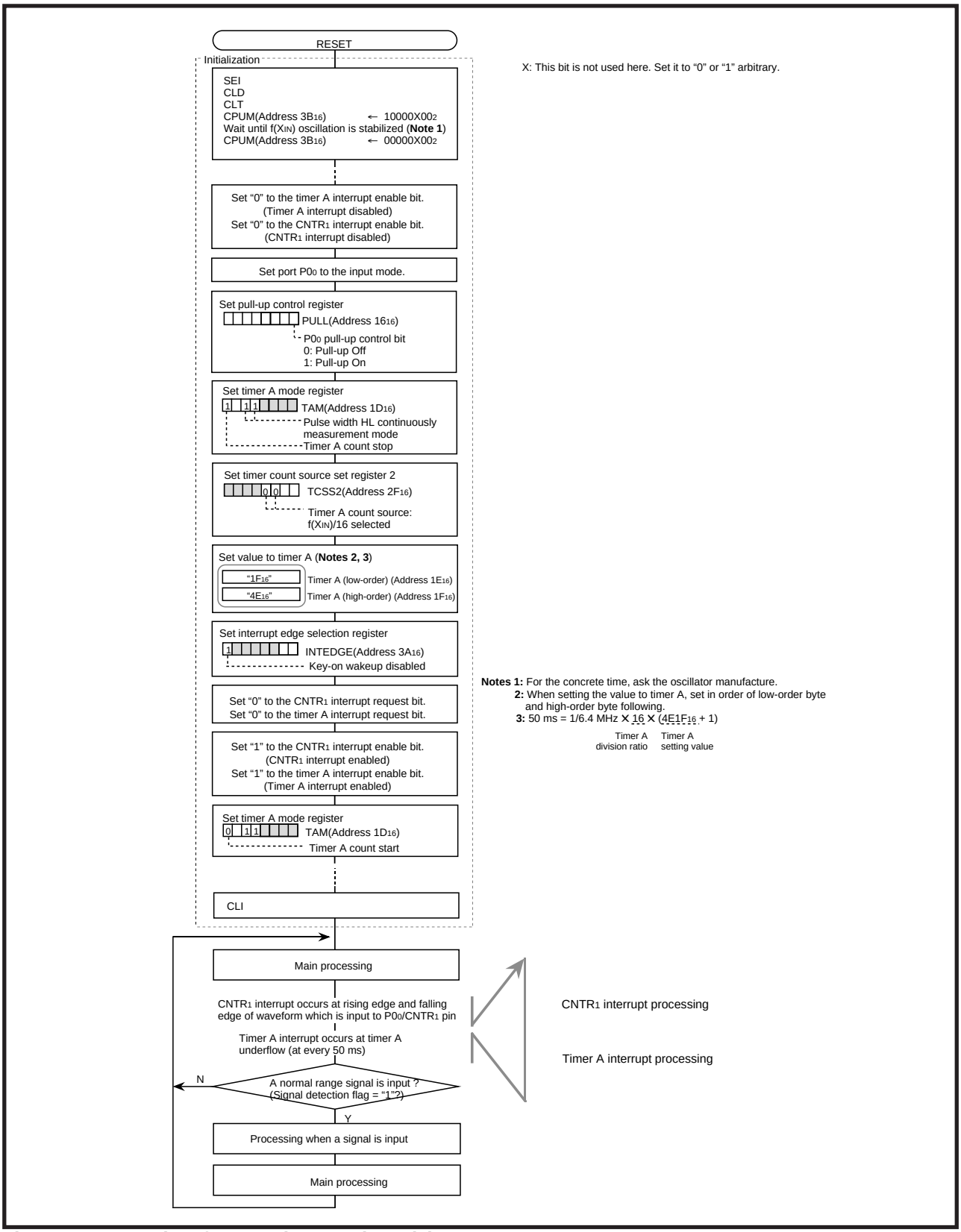

Figure 3 Example of control procedure (1)

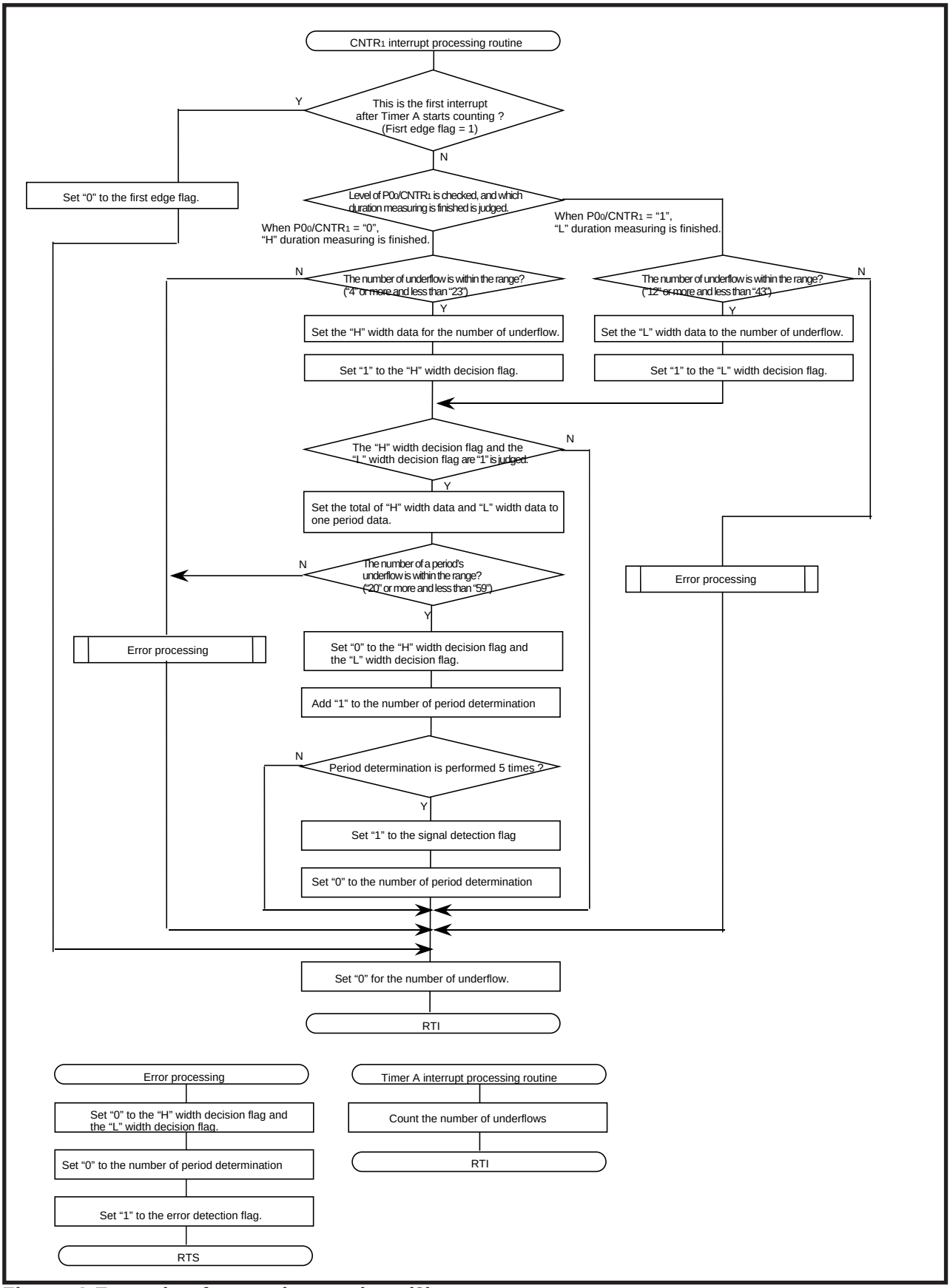

Figure 4 Example of control procedure (2)

4. Sample Programming Code

```
[Reset Start ••• Main Routine Process]

RESET:
          SEI                       ; Interrupt disable
          CLD
          CLT
;
          LDX  #$FF                 ; Set stack bottom
          TXS
;
          LDM  #%10000000,CPUM      ; Set CPU mode register
;
; Wait f(XIN) oscillation stabilizing time
;
          LDM  #%00000000,CPUM      ; Set CPU mode register
;
          LDA  #0
          LDX  #>RAM_top
RAM_clear:    STA  $00,X
          INX
          BNE  RAM_clear
;
          CLB  2,ICON2              ; TimerA interrupt disable
          CLB  6,ICON1              ; CNTR1 interrupt disable
;
          LDM  #%00000000,P0D       ; Set Port P0 direction register
;
          CLB  0,PULL               ; Port P00 Pull_up off
;
          LDM  #%10110000,TAM       ; Set Timer A mode register
;
          LDM  #%00000000,TCSS2     ; Set Timer count source set register 2
;
          LDM  #$1F,TAL             ; Set Timer A (low-order)
          LDM  #$4E,TAH             ; Set Timer A (high-order)
;
          SEB  7,INTEDGE            ; disable key on wake-up interrupt
;
          CLB  2,IREQ2              ; TimerA interrupt request clear
          CLB  6,IREQ1              ; CNTR1 interrupt request clear
          SEB  2,ICON2              ; TimerA interrupt enable
          SEB  6,ICON1              ; CNTR1 interrupt enable
;
          SEB  f_first_edge         ; ignore first edge

          CLB  7,TAM                ; start timer A count
;
          CLI
;
__MAIN:

          BBC  f_RING,__MAIN
               ;
               ;  process
               ;
          BRA  __MAIN
;
```

Figure 5 Sample Programming Code (1)

[CNTR1 Interrupt Process]

```
__int_CNTR1:
          CLD
          CLT
          PHA
;
          BBC  f_first_edge,__int_CNTR1_00
          CLB  f_first_edge
          BRA  __int_CNTR1_RT

__int_CNTR1_00:
          BBS  P0_0,__int_CNTR1_10
;
          LDA  TimerA_CNT
          STA  B_TimerA_CNT_L
;
          CMP  #4                ; High-Level 4over and 23under check
          BCC  __error
          CMP  #23
          BCS  __error
          SEB  fix_H
          BRA  __int_CNTR1_11
;
__int_CNTR1_10:
          LDA  TimerA_CNT
          STA  B_TimerA_CNT_H
;
          CMP  #12               ; Low-Level 12over and 43under check
          BCC  __error
          CMP  #43
          BCS  __error
          SEB  fix_L
;
__int_CNTR1_11:
          BBC  fix_L,__int_CNTR1_RT
          BBC  fix_H,__int_CNTR1_RT
          CLC
          LDA  B_TimerA_CNT_L
          ADC  B_TimerA_CNT_H
          STA  B_TimerA_CNT
          CMP  #20               ; Total 20over and 59under check
          BCC  __error
          CMP  #59
          BCS  __error
;
          CLB  fix_L
          CLB  fix_H
          INC  RING_CNT

          LDA  RING_CNT
          CMP  #5
          BCC  __int_CNTR1_RT
          SEB  f_RING
          LDM  #0,RING_CNT
          BRA  __int_CNTR1_RT
;
__error:
          CLB  fix_H
          CLB  fix_L
          LDM  #0,RING_CNT
          SEB  f_error
;
__int_CNTR1_RT:
          LDM  #0,TimerA_CNT
          PLA
          RTI
;
```

Figure 6 Sample Programming Code (2)

5. Reference

Data Sheet
7544 Group Data sheet
7544 Group Data sheet (QzROM Version)

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REVISION HISTORY	7544 Group Timer A Operation (Pulse Width HL Continuously Measurement Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Apr 01, 2003	-	First Edition issued
2.00	Nov 12, 2004	2-4	Contents: Specifications and Figures 1 to 3 revised.
		5	Sample Programming Code added.
2.01	Apr 18, 2005	6	Sample Programming Code added.

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