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April 1st, 2010
Renesas Electronics Corporation

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7544 Group
List of Registers

1. Abstract

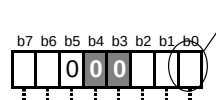
The following article describes the control registers of the 7544 Group.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: 7544 Group

3. Structure of Register

.....register



..... register (....) [Address : ....16]

b	Name	Functions	At reset *2	RW *3
0	.....bits	0 0 : ..... 0 1 : ..... 1 0 : ..... 1 1 : Do not select.	0	RW
1			0	RW
2	.....bit	0 : ..... 1 :	0	RW
3	The contents are “0” at reading. If writing to these bits, write“0”.		0	RO
4	The contents are undefined at reading. If writing to this bit, write“0”.		Undefined	-
5	If writing to this bit, write “0”.		0	RW
6	.....flag	0 : ..... 1 :	0	RO
7	.....bit	0 : ..... 1 :	0	RO

*1

Blank	: Set “1” or “0” to this bit as usage.
0	: If writing to this bit, write “0”.
1	: If writing to this bit, write “1”.
×	: This bit is not used in the specific mode or state.
■	: Nothing is arranged for this bit.

*2

0	: “0” at reset release
1	: “1” at reset release
Undefined	: Undefined at reset release

*3

RW	: Read enabled. Write enabled.
RO	: Read enabled. This value depends on each bit at writing.
WO	: Write enabled. Undefined at reading.
-	: Undefined at reading. This value depends on each bit at writing.

4. List of Registers

Port Pi register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi register (Pi) (i = 0 to 3)

[Addresses 00_{16}, 02_{16}, 04_{16}, 06_{16}]

b	Name	Functions	At reset	RW
0	Port P_{i0}	•In output mode Write •••••••• Port latch Read •••••••• Port latch •In input mode Write •••••••• Port latch Read •••••••• Value of pin	Undefined	RW
1	Port P_{i1}		Undefined	RW
2	Port P_{i2}		Undefined	RW
3	Port P_{i3}		Undefined	RW
4	Port P_{i4}		Undefined	RW
5	Port P_{i5}		Undefined	RW
6	Port P_{i6}		Undefined	RW
7	Port P_{i7}		Undefined	RW

Note: Nothing is arranged for the following bits.
Port P1: Bits 5, 6 and 7
Port P2: Bits 6 and 7
Port P3: Bits 5 and 6
The contents are undefined at reading. If writing to this bit, write “0”.

Fig. 4.1 Structure of Port Pi register (i = 0 to 3)

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (PiD) (i = 0 to 3)

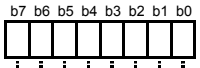
[Addresses 01_{16}, 03_{16}, 05_{16}, 07_{16}]

b	Name	Functions	At reset	RW
0	Port P_{i0} direction register	0 : Input mode 1 : Output mode	0	WO
1	Port P_{i1} direction register	0 : Input mode 1 : Output mode	0	WO
2	Port P_{i2} direction register	0 : Input mode 1 : Output mode	0	WO
3	Port P_{i3} direction register	0 : Input mode 1 : Output mode	0	WO
4	Port P_{i4} direction register	0 : Input mode 1 : Output mode	0	WO
5	Port P_{i5} direction register	0 : Input mode 1 : Output mode	0	WO
6	Port P_{i6} direction register	0 : Input mode 1 : Output mode	0	WO
7	Port P_{i7} direction register	0 : Input mode 1 : Output mode	0	WO

Notes:
1. Nothing is arranged for the following bits.
   Port P1: Bits 5, 6 and 7
   Port P2: Bits 6 and 7
   Port P3: Bits 5 and 6
   The contents are undefined at reading. If writing to this bit, write “0”.
2. In ports set to output mode, the pull-up control bit becomes invalid and pull-up resistor is not connected.

Fig. 4.2 Structure of Port Pi direction register (i = 0 to 3)

Pull-up control register



Pull-up control register (PULL)

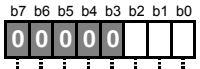
[Address 16_{16}]

b	Name	Functions	At reset	RW
0	$P0_0$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	0	RW
1	$P0_1$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	0	RW
2	$P0_2$, $P0_3$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	0	RW
3	$P0_4$–$P0_7$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	0	RW
4	Ports $P3_0$–$P3_3$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	0	RW
5	Port $P3_4$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	0	RW
6	If writing to this bit, write “0” or “1”.		0	RW
7	$P3_7$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	0	RW

Note: Pins set to output ports are disconnected from pull-up control.

Fig. 4.3 Structure of Pull-up control register

Port P1P3 control register



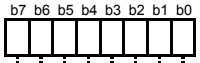
Port P1P3 control register (P1P3C)

[Address 17_{16}]

b	Name	Functions	At reset	RW
0	$P3_7$/INT_0 input level selection bit	0 : CMOS level 1 : TTL level	0	RW
1	$P3_4$/INT_1 input level selection bit	0 : CMOS level 1 : TTL level	0	RW
2	$P1_0$, $P1_2$ input level selection bit	0 : CMOS level 1 : TTL level	0	RW
3	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.4 Structure of Port P1P3 control register

Transmit buffer register



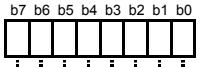
Transmit buffer register (TB)

[Address 18_{16}]

b	Functions	At reset	RW
0	The transmission data is written to this buffer register.	Undefined	WO
1	Write transmission data to this register.	Undefined	WO
2		Undefined	WO
3		Undefined	WO
4		Undefined	WO
5		Undefined	WO
6		Undefined	WO
7		Undefined	WO

Note: This register is assigned to the same address as the receive buffer register. This register cannot be read.

Receive buffer register



Receive buffer register (RB)

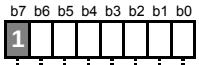
[Address 18_{16}]

b	Functions	At reset	RW
0	The receive data is read from this buffer register.	Undefined	RO
1	Read receive data from this register.	Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note: This register is assigned to the same address as the transmit buffer register. This register cannot be written to.

Fig. 4.5 Structure of Transmit buffer register/Receive buffer register

Serial I/O status register



Serial I/O status register (SIOSTS)

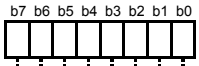
[Address 19_{16}]

b	Name	Functions	At reset	RW
0	Transmit buffer empty flag (TBE) (Note 1)	0: Buffer register full 1: Buffer register empty	0	RO
1	Receive buffer full flag (RBF) (Notes 1, 2)	0: Buffer register empty 1: Buffer register full	0	RO
2	Transmit shift completion flag (TSC)(Note1)	0: Transmit shift in progress 1: Transmit shift completed	0	RO
3	Overrun error flag (OE) (Note 3)	0: No error 1: Overrun error	0	RO
4	Parity error flag (PE) (Note 3)	0: No error 1: Parity error	0	RO
5	Framing error flag (FE) (Note 3)	0: No error 1: Framing error	0	RO
6	Summing error flag (SE) (Note 3)	0: (OE) U (PE) U (FE) = 0 1: (OE) U (PE) U (FE) = 1	0	RO
7	The contents are “1” at reading. If writing to this bit, write “0”.		1	RO

Notes:
1. Write “0” to this bit at writing.
2. This bit becomes “0” when the receive buffer register is read.
3. This bit becomes “0” when written to this register. If writing to this bit, write “0”.

Fig. 4.6 Structure of Serial I/O status register

Serial I/O control register



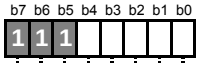
Serial I/O control register (SIOCON)

[Address $1A_{16}$]

b	Name	Functions	At reset	RW
0	BRG count source selection bit (CSS)	0: f(X_{IN}) 1: f(X_{IN})/4	0	RW
1	Serial I/O synchronous clock selection bit (SCS)	0: BRG output divided by 4 when clock synchronous serial I/O is selected, BRG output divided by 16 when UART is selected. 1: External clock input when clock synchronous serial I/O is selected, external clock input divided by 16 when UART is selected.	0	RW
2	$\overline{SRDY}$ output enable bit (SRDY)	0: $P1_3$ pin operates as ordinary I/O pin 1: $P1_3$ pin operates as $\overline{SRDY}$ output pin	0	RW
3	Transmit interrupt source selection bit (TIC)	0: Interrupt when transmit buffer has emptied (TBE=1) 1: Interrupt when transmit shift operation is completed (TSC=1)	0	RW
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	RW
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	RW
6	Serial I/O mode selection bit (SIOM)	0: Clock asynchronous (UART) serial I/O 1: Clock synchronous serial I/O	0	RW
7	Serial I/O enable bit (SIOE)	0: Serial I/O disabled (pins $P1_0$ to $P1_3$ operate as ordinary I/O pins) 1: Serial I/O enabled (pins $P1_0$ to $P1_3$ operate as serial I/O pins)	0	RW

Fig. 4.7 Structure of Serial I/O control register

UART control register



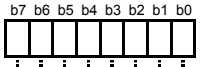
UART control register (UARTCON)

[Address 1B16]

b	Name	Functions	At reset	RW
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	RW
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	RW
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	RW
4	P11/TxD1 P-channel output disable bit (POFF)	0: CMOS output (in output mode) 1: N-channel open drain output (in output mode)	0	RW
5	The contents are “1” at reading. If writing to these bits, write “1”.		1	RO
6			1	RO
7			1	RO

Fig. 4.8 Structure of UART control register

Baud rate generator



Baud rate generator (BRG)

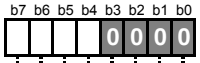
[Address 1C16]

b	Functions	At reset	RW
0	Set the divided value of BRG count source.	Undefined	RW
1	The baud rate generator divides the frequency of the count source by 1/(n+1), where n is the value written to the baud rate generator.	Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Note: Only write to this register while transmit/receive operation is stopped.

Fig. 4.9 Structure of Baud rate generator

Timer A mode register



Timer A mode register (TAM)

[Address 1D16]

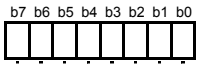
b	Name	Functions	At reset	RW
0	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
1			0	RO
2			0	RO
3			0	RO
4	Timer A operating mode bits	b5 b4 0 0 : Timer mode 0 1 : Period measurement mode 1 0 : Event counter mode 1 1 : Pulse width HL continuously measurement mode	0	RW
5			0	RW
6	CNTR1 active edge switch bit	The function depends on the operating mode of Timer A. (refer to Table 4.1)	0	RW
7	Timer A count stop bit	0 : Count start 1 : Count stop	0	RW

Fig. 4.10 Structure of Timer A mode register

Table 4.1 CNTR1 active edge switch bit function

Timer A operation mode	Set value	Timer function selection	CNTR1 interrupt request occurrence source
Timer mode	“0”	–	CNTR1 input signal falling edge (No influence to timer count)
	“1”	–	CNTR1 input signal rising edge (No influence to timer count)
Period measurement mode	“0”	Measure falling edge period	Input signal falling edge
	“1”	Measure rising edge period	Input signal rising edge
Event counter mode	“0”	Count at rising edge	Input signal falling edge
	“1”	Count at falling edge	Input signal rising edge
Pulse width HL continuously measurement mode	“0”	Measure “H” pulse width and “L” pulse width	Input signal falling edge and rising edge
	“1”		

Timer A high-order register, Timer A low-order register



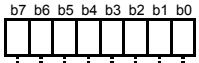
Timer A high-order register (TAH), Timer A low-order register (TAL)

[Addresses 1F16, 1E16]

b	Functions	At reset	RW
0	Set a count value of timer A. [At write] Writes data to both timer A latch and timer A simultaneously. Write both registers from TAL to TAH in consecutive order. [At read] The timer A count value is read by reading these registers. Read both registers from TAH to TAL in consecutive order.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.11 Structure of Timer A high-order register, Timer A low-order register

Prescaler 1



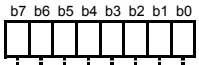
Prescaler 1 (PRE1)

[Address 28_{16}]

b	Functions	At reset	RW
0	Set the Prescaler 1 count value.	1	RW
1	[At write]	1	RW
2	Writes data to both prescaler 1 latch and prescaler 1 simultaneously.	1	RW
3	[At read]	1	RW
4	The count value of prescaler 1 latch is read by reading this register.	1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.12 Structure of Prescaler 1

Timer 1 register



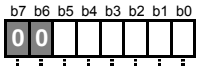
Timer 1 register (T1)

[Address 29_{16}]

b	Functions	At reset	RW
0	Set the Timer 1 count value.	1	RW
1	[At write]	0	RW
2	Writes data to both prescaler 1 latch and prescaler 1 simultaneously.	0	RW
3	[At read]	0	RW
4	The count value of timer 1 latch is read by reading this register.	0	RW
5		0	RW
6		0	RW
7		0	RW

Fig. 4.13 Structure of Timer 1 register

Timer X mode register



Timer X mode register (TXM)
[Address 2B16]

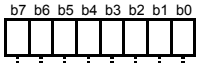
b	Name	Functions	At reset	RW
0	Timer X operating mode bits	b1 b0 0 0 : Timer mode 0 1 : Pulse output mode 1 0 : Event counter mode 1 1 : Pulse width measurement mode	0	RW
1			0	RW
2	CNTR0 active edge switch bit	The function depends on the operating mode of Timer X. (refer to Table 4.2)	0	RW
3	Timer X count stop bit	0 : Count start 1 : Count stop	0	RW
4	P03/TXOUT output valid bit	0 : Output invalid (I/O port) 1 : Output valid (Inverted CNTR0 output)	0	RW
5	Timer X write control bit	0 : Write to latch and timer simultaneously 1 : Write to only latch	0	RW
6	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
7			0	RO

Fig. 4.14 Structure of Timer X mode register

Table 4.2 CNTR0 active edge switch bit function

Timer X operation mode	Set value	Timer function selection	CNTR0 interrupt request occurrence source
Timer mode	“0”	–	CNTR0 input signal falling edge (No influence to timer count)
	“1”	–	CNTR0 input signal rising edge (No influence to timer count)
Pulse output mode	“0”	Pulse output start from “H”	Output signal falling edge
	“1”	Pulse output start from “L”	Output signal rising edge
Event counter mode	“0”	Count at rising edge	Input signal falling edge
	“1”	Count at falling edge	Input signal rising edge
Pulse width measurement mode	“0”	Measure “H” pulse width	Input signal falling edge
	“1”	Measure “L” pulse width	Input signal rising edge

Prescaler X



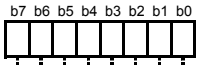
Prescaler X (PREX)

[Address $2C_{16}$]

b	Functions	At reset	RW
0	Set the prescaler X count value.	1	RW
1	[At write]	1	RW
2	When writing is executed, writing to "latch only" or "Prescaler X and Timer X	1	RW
3	and their latches" can be selected by the setting value of the timer X write	1	RW
4	control bit.	1	RW
5	[At read]	1	RW
6	The count value of prescaler X latch is read by reading this register.	1	RW
7		1	RW

Fig. 4.12 Structure of Prescaler X

Timer X register



Timer X register (TX)

[Address $2D_{16}$]

b	Functions	At reset	RW
0	Set the timer X count value.	1	RW
1	[At write]	1	RW
2	When writing is executed, writing to "latch only" or "Prescaler X and Timer X	1	RW
3	and their latches" can be selected by the setting value of the timer X write	1	RW
4	control bit.	1	RW
5	[At read]	1	RW
6	The count value of timer X latch is read by reading this register.	1	RW
7		1	RW

Fig. 4.13 Structure of Timer X register

Timer count source set register 1

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

Timer count source set register 1 (TCSS1)

[Address $2E_{16}$]

b	Name	Functions	At reset	RW
0	Timer X count source selection bits	b1 b0 0 0 : f(XIN)/16 0 1 : f(XIN)/2 1 0 : f(XIN) (Note) 1 1 : Not available	0	RW
1			0	RW
2	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: f(XIN) can be used as timer X count source when using a ceramic resonator or on-chip oscillator.
Do not use it at RC oscillation.

Fig. 4.17 Structure of Timer count source set register 1

Timer count source set register 2

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

Timer count source set register 2 (TCSS2)

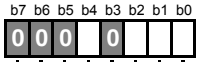
[Address $2F_{16}$]

b	Name	Functions	At reset	RW
0	Timer 1 count source selection bits	b1 b0 0 0 : f(XIN)/16 0 1 : f(XIN)/2 1 0 : f(XIN) (Note) 1 1 : Not available	0	RW
1			0	RW
2	Timer A count source selection bits	b3 b2 0 0 : f(XIN)/16 0 1 : f(XIN)/2 1 0 : f(XIN) (Note) 1 1 : Not available	0	RW
3			0	RW
4	The contents are “0” at reading. If writing to these bits, write “0”.		0	RO
5			0	RO
6			0	RO
7			0	RO

Note: System operates using an on-chip oscillator as a count source by setting the on-chip oscillator to oscillation enabled by bit 3 of CPUM.

Fig. 4.18 Structure of Timer count source set register 2

A/D control register



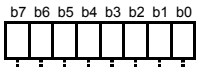
A/D control register (ADCON)

[Address 34_{16}]

b	Name	Functions	At reset	RW
0	Analog input pin selection bits	b2b1b0 0 0 0 : $P2_0/AN_0$ 0 1 0 : $P2_1/AN_1$ 0 0 1 : $P2_2/AN_2$ 0 1 1 : $P2_3/AN_3$ 1 0 0 : $P2_4/AN_4$ 1 0 1 : $P2_5/AN_5$ 1 1 0 : Disable 1 1 1 : Disable	0	RW
1			0	RW
2			0	RW
3	The contents are “0” at reading. If writing to this bit, write “0”.		0	RO
4	AD conversion completion bit	0 : Conversion in progress 1 : Conversion completed	1	RW
5	The contents are “0” at reading. If writing to this bit, write “0”.		0	RO
6			0	RO
7			0	RO

Fig. 4.19 Structure of A/D control register

A/D register



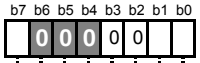
A/D register (AD)

[Address 35_{16}]

b	Functions	At reset	RW
0	A-D conversion result can be read.	Undefined	RO
1		Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Fig. 4.20 Structure of A/D register

MISRG



MISRG register (MISRG)

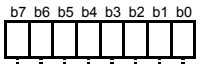
[Address 38_{16}]

b	Name	Functions	At reset	RW
0	Oscillation stabilization time set bit after release of the STP instruction	0 : Set "00_{16}" in timer 1, and "FF_{16}" in prescaler 1 automatically 1 : Not set automatically	0	RW
1	Ceramic/quartz-crystal or RC oscillation stop detection function active bit	0 : Detection function inactive 1 : Detection function active	0	RW
2	When these bits are read out, the contents are "0". If writing to these bits, write "0".		0	RW
3			0	RW
4	When these bits are read out, the contents are "0". If writing to these bits, write "0".		0	RO
5			0	RO
6			0	RO
7	Oscillation stop detection status bit	0 : Oscillation stop not detected 1 : Oscillation stop detected	0 (Note 2)	RW

Notes:
1. The oscillation stop detection circuit is not included in the emulator MCU "M37544RSS".
2. The oscilation stop detection status bit is "1" at normal reset.

Fig. 4.21 Structure of MISRG

Watchdog timer control register



Watchdog timer control register (WDTCON)

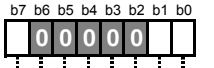
[Address 39_{16}]

b	Name	Functions	At reset	RW
0	Watchdog timer H		1	RO
1			1	RO
2			1	RO
3			1	RO
4			1	RO
5			1	RO
6	STP instruction disable bit (Note 1)	0 : STP instruction enabled 1 : STP instruction disabled	0	RW
7	Watchdog timer H count source selection bit	0 : Watchdog timer L underflow 1 : f(X_{IN})/16	0	RW

Notes:
1. This bit can be set to "0" but not "1" by program.
2. The watchdog timer is set to "$FFFF_{16}$" by writing to this register.

Fig. 4.22 Structure of Watchdog timer control register

Interrupt edge selection register



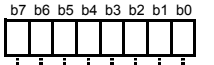
Interrupt edge selection register (INTEDGE)

[Address 3A16]

b	Name	Functions	At reset	RW
0	INT0 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
1	INT1 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
2	When these bits are read out, the contents are “0”. If writing to these bits, write “0”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7	P00 key-on wakeup enable bit	0 : Key-on wakeup enabled 1 : Key-on wakeup disabled	0	RW

Fig. 4.23 Structure of Interrupt edge selection register

CPU mode register



CPU mode register (CPUM)

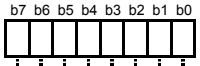
[Address 3B16]

b	Name	Functions	At reset	RW
0	Processor mode bits	b1 b0 0 0 : Single-chip mode 0 1 : Not available 1 0 : Not available 1 1 : Not available	0	RW
1			0	RW
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	RW
3	On-chip oscillator oscillation control bit	0 : On-chip oscillator oscillation enabled 1 : On-chip oscillator oscillation stop	0	RW
4	XIN oscillation control bit	0 : Ceramic/quartz-crystal or RC oscillation enabled 1 : Ceramic/quartz-crystal or RC oscillation stop	0	RW
5	Oscillation mode selection bit (Note 1)	0 : Ceramic/quartz-crystal oscillation 1 : RC oscillation	0	RW
6	Clock division ratio selection bits	b7 b6 0 0 : f(φ) = f(XIN)/2 (High-speed mode) 0 1 : f(φ) = f(XIN)/8 (Middle-speed mode) 1 0 : applied from on-chip oscillator 1 1 : f(φ) = f(XIN) (Double-speed mode) (Note 2)	0	RW
7			1	RW

Note 1: The bit can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. However, by reset the bit is initialized and can be rewritten, again.
(It is not disable to write any data to the bit for emulator MCU “M37544RSS”.)
2: These bits are used only when a ceramic/quartz-crystal oscillation is selected. Do not use these when an RC oscillation is selected.

Fig. 4.24 Structure of CPU mode register

Interrupt request register 1



Interrupt request register 1 (IREQ1)

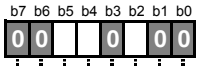
[Address $3C_{16}$]

b	Name	Functions	At reset	RW
0	Serial I/O receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
1	Serial I/O transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
2	INT_0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
3	INT_1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
4	Key-on wake up interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
5	$CNTR_0$ interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
6	$CNTR_1$ interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
7	Timer X interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)

Note: This bit can be set to “0” but not to “1” by program.

Fig. 4.25 Structure of Interrupt request register 1

Interrupt request register 2



Interrupt request register 2 (IREQ2)

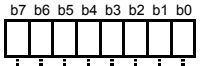
[Address $3D_{16}$]

b	Name	Functions	At reset	RW
0	The contents are “0” at reading. If writing to this bit, write “0”.		0	RO
1			0	RO
2	Timer A interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
3	The contents are “0” at reading. If writing to this bit, write “0”.		0	RO
4	A/D conversion interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
5	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	RW (Note)
6	The contents are “0” at reading. If writing to this bit, write “0”.		0	RO
7			0	RO

Note: This bit can be set to “0” but not to “1” by program.

Fig. 4.26 Structure of Interrupt request register 2

Interrupt control register 1



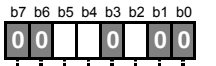
Interrupt control register 1 (ICON1)

[Address $3E_{16}$]

b	Name	Functions	At reset	RW
0	Serial I/O receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
1	Serial I/O transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
2	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
3	INT_1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
4	Key-on wake up interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
5	$CNTR_0$ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
6	$CNTR_1$ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
7	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW

Fig. 4.27 Structure of Interrupt control register 1

Interrupt control register 2



Interrupt control register 2 (ICON2)

[Address $3F_{16}$]

b	Name	Functions	At reset	RW
0	The contents are “0” at reading. If writing to this bit, write “0”.		0	RO
1			0	RO
2	Timer A interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
3	The contents are “0” at reading. If writing to this bit, write “0”.		0	RO
4	A/D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
5	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	RW
6	The contents are “0” at reading. If writing to this bit, write “0”.		0	RO
7			0	RO

Fig. 4.28 Structure of Interrupt request register 2

5. Reference

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		Page	Summary
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