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# 7542Group

# Timer X Operation (Pulse Width Measurement Mode)

#### 1. Abstract

The following article introduces and shows an application example of pulse width measurement mode of timer X.

# 2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: 7542 Group



# 3. Pulse Output Mode Setting Method

Figure 1 and Figure 2 shows the setting method for pulse width measurement mode of timer X.

Process 1: Disable timer X interrupt and CNTR0 interrupt.
CNTRo interrupt disabled
Interrupt control register 2 (ICON2) [Address: 3F16]
Timer X interrupt disabled
Process 2: Set the CNTR <sub>0</sub> pin to the input mode.
Port1 direction register (P1D) [Address: 0316]
Set the P14/CNTR <sub>0</sub> pin to the input mode
Process 3: Set timer X mode register.
b7 b0 1 1 1 Timer X mode register (TXM) [Address: 2B16]
Image: Image of the second
CNTRo active edge switch
0: "H" level with measurement
1: "L" level with measurement
Timer X count stop
Process 4: Set timer count source set register.
Timer count source set register (TCSS) [Address: 2A16]
Timer X count source selection bits
b1b0
0 0:f(XiN)/16
0.1:f(X N)/2
1 0:f(Xiℕ) (Note) 1 1: Not available
Note: f(XIN) can be used only when a ceramic resonator or an on-chip oscillator is used.
Do not use f(XIN) at RC oscillator.
Process 5: Set the count value to timer X.
• Set the count value to prescaler X and timer X.
Prescaler X (PREX) [Address: 2C16]
Count value
Timer X (TX) [Address: 2D16]
Count value





Proc	cess 6: In order not to execute the no requested interrupt processing,
	set "0" (no requested) to the timer X interrupt request bit and CNTRo interrupt request bit.
Proc	cess 7: When the interrupt is used, set "1" (interrupt enabled) to the interrupt enable bit.
Proc	cess 8: Start counting timer X.

Figure 2 Setting method for pulse width measurement mode (2)



#### 4. Application Example of Pulse Width Measurement Mode

Outline: "H" level width of pulse input to P14/CNTR0 pin is counted.

**Specifications**: The "H" level width of a FG pulse input to the P14/CNTR0 pin is counted. An underflow is detected by the timer X interrupt. The completion of "H" level of input pulse is detected by the CNTR0 interrupt.

Operation clock:  $f(X_{IN}) = 4.19$  MHz, high-speed mode

# 4.1 Connection of Timer and Setting of Division Ratio

Figure 3 shows the connection of timer and setting of division ratio.

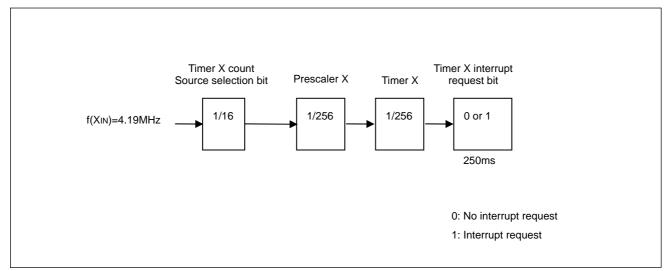


Figure 3 Connection of timer and setting of division ratio

# 4.2 Example of Control Procedure

Figure 4 shows an example of control procedure.



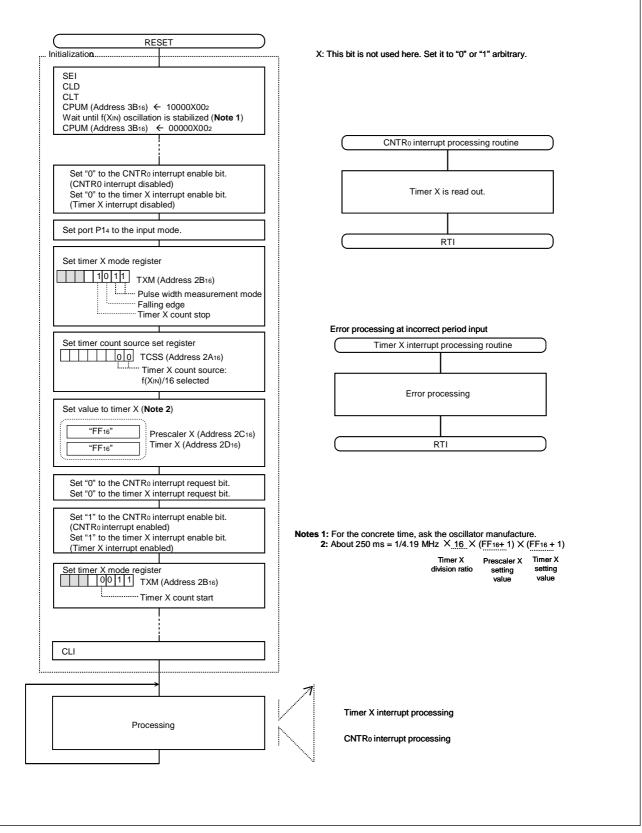


Figure 4 Example of control procedure



### 5. Reference

Renesas Technology Corporation Semiconductor Home Page http://www.renesas.com

E-mail Support E-mail: support\_apl@renesas.com

Data Sheet 7542 Group Data sheet (Use the latest version on the home page: http://www.renesas.com)



# **Revision Record**

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		Page	Summary	
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