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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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# 7542 Group Clock Asynchronous Serial I/O (UART)

### 1. Abstract

The following article introduces and shows an application example of clock asynchronous (UART) of serial I/O1.

#### 2. Introduction

The explanation of this issue is applied to the following condition: Applicable MCU: 7542 Group



#### 3. Contents

For clock asynchronous serial I/O (UART), the baud rate and transfer formats used by a transmitter and receiver must be identical.

In the 7542 Group, eight serial data transfer formats can be selected.

Also, as for the serial I/O2, it has an equivalent function to serial I/O1 except that TxD2 output structure for serial I/O2 is CMOS only. Accordingly, the application example of the following serial I/O1 is applicable for serial I/O2.

#### 3.1 Data Transfer Rate

The transfer bit rate is calculated by the following formula;

• When the internal clock is selected (when baud rate generator is used)

Transfer bit rate [bps] =  $\frac{f(X_{IN})}{Division ratio ^{*1} X (BRG1 setting value ^{*2} + 1) X 16}$ 

Division ratio<sup>\*1</sup> : "1" or "4" is selected (set by bit 0 of serial I/O1 control register) BRG1 setting value<sup>\*2</sup> : 0 to 255 ( $00_{16}$  to FF<sub>16</sub>) is set

• When the external clock is selected

Transfer bit rate [bps] = Clock input to SCLK1 pin/16

Table 1 shows the setting example of baud rate generator and transfer bit rate values.

| BRG count source | BRG1 set value          | Transfer bit rate (bps)             |                                |
|------------------|-------------------------|-------------------------------------|--------------------------------|
|                  |                         | At f(X <sub>IN</sub> ) = 4.9152 MHz | At $f(X_{IN}) = 8 \text{ MHz}$ |
| f(XIN) / 4       | 255 (FF <sub>16</sub> ) | 300                                 | 488.28125                      |
| f(XIN) / 4       | 127 (7F <sub>16</sub> ) | 600                                 | 976.5625                       |
| f(XIN) / 4       | 63 (3F <sub>16</sub> )  | 1200                                | 1953.125                       |
| f(XIN) / 4       | 31 (1F16)               | 2400                                | 3906.25                        |
| f(XIN) / 4       | 15 (0F <sub>16</sub> )  | 4800                                | 7812.5                         |
| f(XIN) / 4       | 7 (0716)                | 9600                                | 15625                          |
| f(XIN) / 4       | 3 (0316)                | 19200                               | 31250                          |
| f(XIN) / 4       | 1 (0116)                | 38400                               | 62500                          |
| f(XIN)           | 3 (0316)                | 76800                               | 125000                         |
| f(XIN)           | 1 (0116)                | 153600                              | 250000                         |
| f(XIN)           | 0 (0016)                | 307200                              | 500000                         |

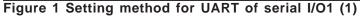
Table 1 Setting example of baud rate generator1 (BRG1) and transfer bit rate values



#### 3.2 UART Setting Method

Figure 1 and Figure 2 show the setting method for UART of serial I/O1.

| Process 1: Stop and initialize serial I/O.  |
|---|
| Image: |
| Process 2: Disable serial I/O1 transmit/receive interrupt.  |
| b7       b0         Interrupt control register 1 (ICON1) [Address 3E16]         Serial I/O1 receive interrupt disabled         Serial I/O1 transmit interrupt disabled  |
| Process 3: Set serial I/O1 control register.  |
| b7       b0         Serial I/O1 control register (SIO1CON) [Address 1A16]         BRG count source selected (set in internal clock selected)         0: f(XiN)         1: f(XiN)/4         Serial I/O1 synchronous clock selected (Note 1)         0: BRG output/16         1: External clock input/16         7: When transmit buffer has emptied         1: When transmit shift operation is completed         Transmit enable selected         0: Transmit disabled (at half-duplex communication receive)         1: Transmit enable d(at full-duplex communication transmit)         1: Receive enabled (at full-duplex communication transmit)         1: Receive enable (P10–P12 pins operate as serial I/O1 pins)(Note 3)   |
| <ul> <li>Note 1: Setting of serial I/O1 synchronous clock selection bit is as follows;</li> <li>"0": P12 pin can be used as a normal I/O pin</li> <li>"1": P12 pin is used as an input pin for an external clock.</li> <li>2: When data transmission is executed at the state that an external clock input is selected as the synchronous clock, set "1" to the transmit enable bit while the ScLK1 is "H" state.</li> <li>3: When clock asynchronous (UART) serial I/O is selected, P13 pin can be used as a normal I/O pin.</li> </ul>  |
|   |





| b7  | b0   |
|---|--|
|   | UART1 control register (UART1CON) [Address 1B <sub>16</sub> ]  |
|   | Select character length  |
|   | 0: 8 bits  |
|   | 1: 7 bits  |
|   | Select parity enable       0: Parity disabled  |
|   | 1: Parity enabled  |
|   | Select parity (valid only when parity is enabled)  |
|   | 0: Even parity   |
|   | 1: Odd parity<br>Select stop bit length  |
|   | 0: 1 stop bit  |
|   | 1: 2 stop bits   |
|   | Select P11/TxD1 P-channel output disable (in output mode)  |
|   | 0: CMOS output<br>1: N-channel open-drain output   |
|   |  |
|   |  |
| Process 5: whe  | en BRG output/16 is selected as synchronous clock, set value to baud rate generate   |
|   |  |
|   | Baud rate generator1 (BRG1) [Address 1C16]   |
| L   | Set baud rate value  |
| to th   | der not to execute the no requested interrupt processing, set "0" (no requested)<br>the serial I/O1 transmit/receive interrupt request bit.  |
|   | be serial I/O1 transmit/receive interrupt request bit.          b0       Interrupt request register 1 (IREQ1) [Address 3C16]         Image: No serial I/O1 receive interrupt request issued  |
| to th   | bo bo Interrupt request register 1 (IREQ1) [Address 3C16]  |
| to th   | e serial I/O1 transmit/receive interrupt request bit.<br>Interrupt request register 1 (IREQ1) [Address 3C16]<br>No serial I/O1 receive interrupt request issued<br>No serial I/O1 transmit interrupt request issued<br>en the interrupt is used, set "1" (interrupt enabled) to the serial I/O1 transmit/  |
| to th   | eserial I/O1 transmit/receive interrupt request bit.<br>Interrupt request register 1 (IREQ1) [Address 3C16]<br>No serial I/O1 receive interrupt request issued<br>No serial I/O1 transmit interrupt request issued<br>en the interrupt is used, set "1" (interrupt enabled) to the serial I/O1 transmit/<br>eive interrupt enable bit.   |
| to the  | <ul> <li>e serial I/O1 transmit/receive interrupt request bit.</li> <li>Interrupt request register 1 (IREQ1) [Address 3C16]</li> <li>No serial I/O1 receive interrupt request issued<br/>No serial I/O1 transmit interrupt request issued</li> <li>en the interrupt is used, set "1" (interrupt enabled) to the serial I/O1 transmit/<br/>eive interrupt enable bit.</li> </ul>  |
| to th<br><sup>b7</sup><br>Process 7: Who<br>rece                  | e serial I/O1 transmit/receive interrupt request bit.          b0       Interrupt request register 1 (IREQ1) [Address 3C16]         Image: Serial I/O1 receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 transmit interrupt request issued         No serial I/O1 transmit interrupt request issued         en the interrupt is used, set "1" (interrupt enabled) to the serial I/O1 transmit/         eive interrupt enable bit.         Image: Serial I/O1 receive interrupt enabled   |
| to th<br><sup>b7</sup><br>Process 7: Who<br>rece                  | the serial I/O1 transmit/receive interrupt request bit.<br>$\begin{array}{c c c c c c c c c c c c c c c c c c c $  |
| to th<br><sup>b7</sup><br>Process 7: Who<br>rece                  | e serial I/O1 transmit/receive interrupt request bit.          b0       Interrupt request register 1 (IREQ1) [Address 3C16]         Image: Serial I/O1 receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 transmit interrupt request issued         No serial I/O1 transmit interrupt request issued         en the interrupt is used, set "1" (interrupt enabled) to the serial I/O1 transmit/         eive interrupt enable bit.         Image: Serial I/O1 receive interrupt enabled   |
| to th<br><sup>b7</sup><br>Process 7: Who<br>rece                  | e serial I/O1 transmit/receive interrupt request bit.          b0       Interrupt request register 1 (IREQ1) [Address 3C16]         Image: Serial I/O1 receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 transmit interrupt request issued         No serial I/O1 transmit interrupt request issued         en the interrupt is used, set "1" (interrupt enabled) to the serial I/O1 transmit/         eive interrupt enable bit.         Image: Serial I/O1 receive interrupt enabled   |
| to th<br><sup>b7</sup><br>Process 7: Who<br>rece<br><sup>b7</sup> | e serial I/O1 transmit/receive interrupt request bit.          b0       Interrupt request register 1 (IREQ1) [Address 3C16]         Image: Serial I/O1 receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 transmit interrupt request issued         No serial I/O1 transmit interrupt request issued         en the interrupt is used, set "1" (interrupt enabled) to the serial I/O1 transmit/         eive interrupt enable bit.         Image: Serial I/O1 receive interrupt enabled   |
| to th<br><sup>b7</sup><br>Process 7: Who<br>rece<br><sup>b7</sup> | e serial I/O1 transmit/receive interrupt request bit.          i <td< td=""></td<>         |
| to th<br><sup>b7</sup><br>Process 7: Who<br>rece<br><sup>b7</sup> | e serial I/O1 transmit/receive interrupt request bit.          Image: Display to the serial I/O1 transmit/receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 transmit interrupt request issued         No serial I/O1 transmit interrupt request issued         No serial I/O1 transmit interrupt request issued         en the interrupt is used, set "1" (interrupt enabled) to the serial I/O1 transmit/         En the interrupt enable bit.         Image: Display to the serial I/O1 transmit/         Serial I/O1 receive interrupt enabled         Transmit/Receive buffer register 1 (TB1/RB1) [Address 1816]  |
| to th<br><sup>b7</sup><br>Process 7: Who<br>rece<br><sup>b7</sup> | The serial I/O1 transmit/receive interrupt request bit.          Image: b0       Interrupt request register 1 (IREQ1) [Address 3C16]         Image: b0       Interrupt request register 1 (IREQ1) [Address 3C16]         Image: b0       No serial I/O1 receive interrupt request issued         No serial I/O1 transmit interrupt request issued         No serial I/O1 transmit interrupt request issued         Image: b0         Image |
| to the  | e serial I/O1 transmit/receive interrupt request bit.          Image: Display to the serial I/O1 transmit/receive interrupt request issued         No serial I/O1 receive interrupt request issued         No serial I/O1 transmit interrupt request issued         No serial I/O1 transmit interrupt request issued         No serial I/O1 transmit interrupt request issued         en the interrupt is used, set "1" (interrupt enabled) to the serial I/O1 transmit/         En the interrupt enable bit.         Image: Display to the serial I/O1 transmit/         Serial I/O1 receive interrupt enabled         Transmit/Receive buffer register 1 (TB1/RB1) [Address 1816]  |





## 3.3 Communication Using UART of Serial I/O (Transmit/Receive)

**Outline** : 2-byte data is transmitted and received, using UART. Port P0<sub>0</sub> is used for communication control.

Specifications : •The Serial I/O1 (UART selected ) is used.

- •Transfer bit rate : 9600 bps ( $f(X_{IN}) = 4.9152$  MHz divided by 512)
- •Communication control using port P0<sub>0</sub> (output level of port P0<sub>0</sub> is controlled by software)
- •2-byte data is transferred from the transmitter to the receiver at 10 ms intervals which the timer generates.

Figure 3 shows a connection diagram, Figure 4 shows a timing chart, Figure 5 shows the control procedure of transmitter, and Figure 6 shows an example of control procedure of receiver.

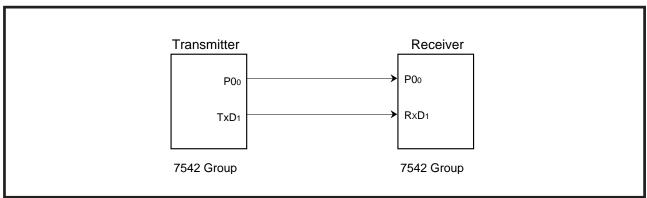


Figure 3 Connection diagram

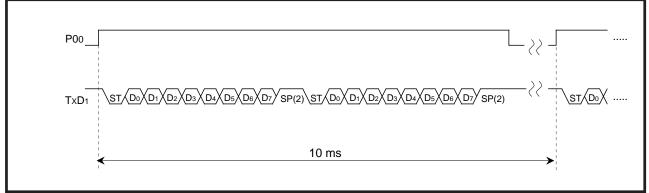


Figure 4 Timing chart



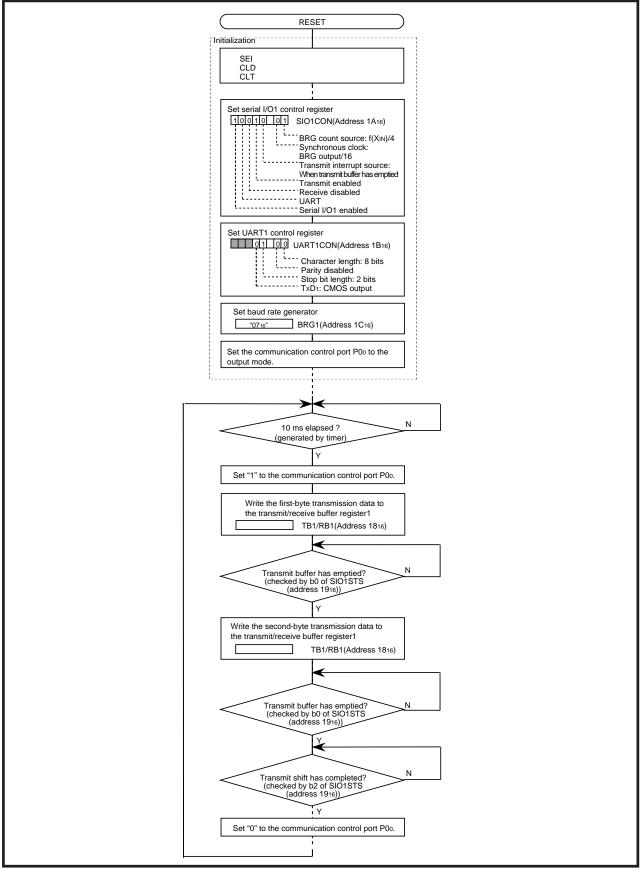


Figure 5 Control procedure of transmitter



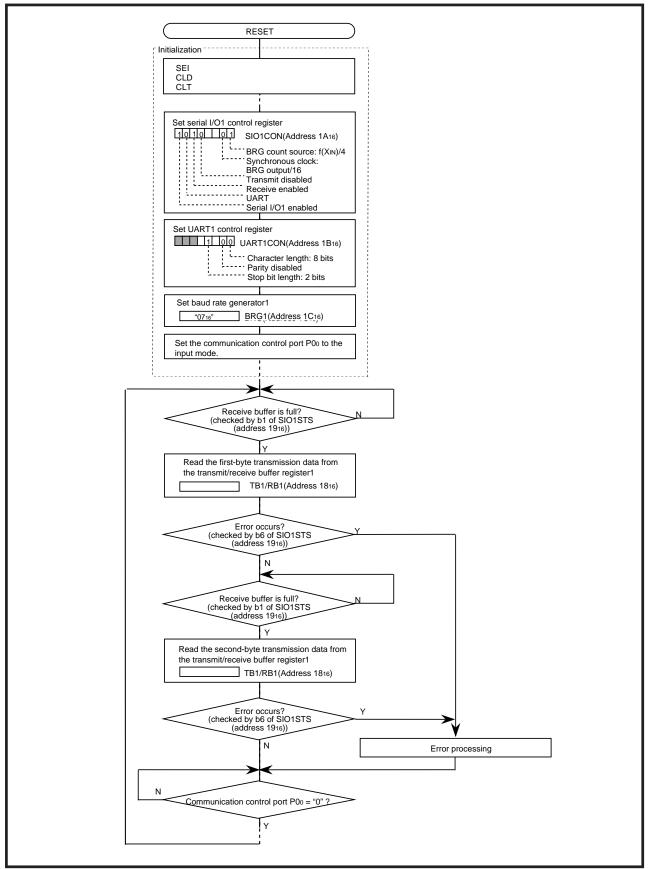


Figure 6 Control procedure of receiver



#### 4. Reference

Data Sheet 7542 Group Data sheet

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| Rev. | Date         | Description |                                  |
|------|--------------|-------------|----------------------------------|
| Nev. |              | Page        | Summary                          |
| 1.00 | Apr 01, 2003 | -           | First Edition issued             |
| 2.00 | Jul 01, 2005 | 2           | 3.Contents: Description revised. |
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