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April 1st, 2010
Renesas Electronics Corporation

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7542Group

Input Capture

1. Abstract

The following article introduces and shows an application example of input capture.

2. Introduction

The explanation of this issue is applied to the following condition:

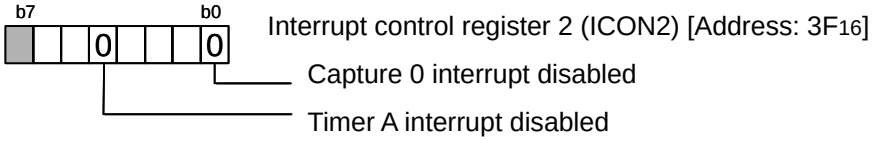
Applicable MCU: 7542 Group

3. Input Capture Setting Method

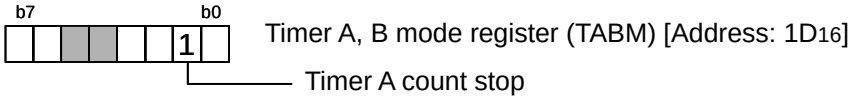
Figure 1, Figure 2 and Figure 3 shows the setting method for input capture 0.

Also, when input capture 1 is used, the procedure is the same.

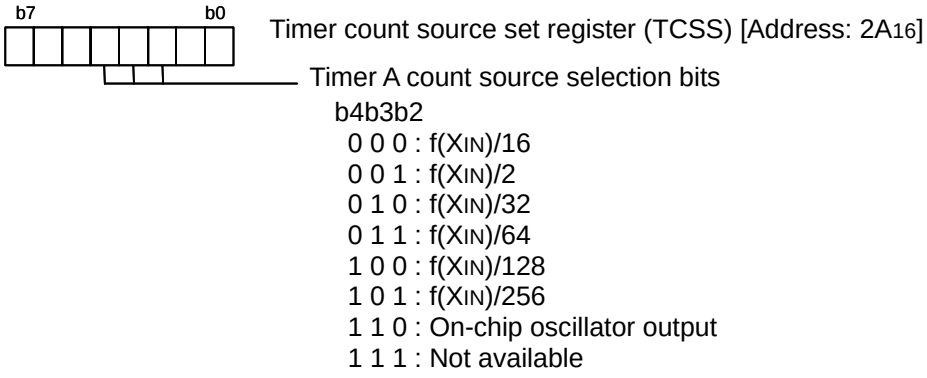
Process 1: Disable timer A interrupt and capture 0 interrupt.



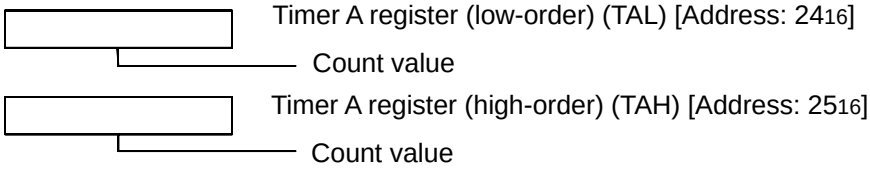
Process 2: Stop timer A counting.



Process 3: Set timer count source set register.



Process 4: Set the count value to timer A.



Note: When setting the value to timer, set in order of low-order byte and high-order byte following.

Process 5: Select timer source for capture.

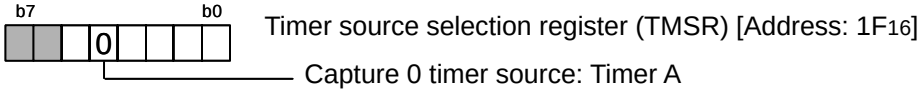
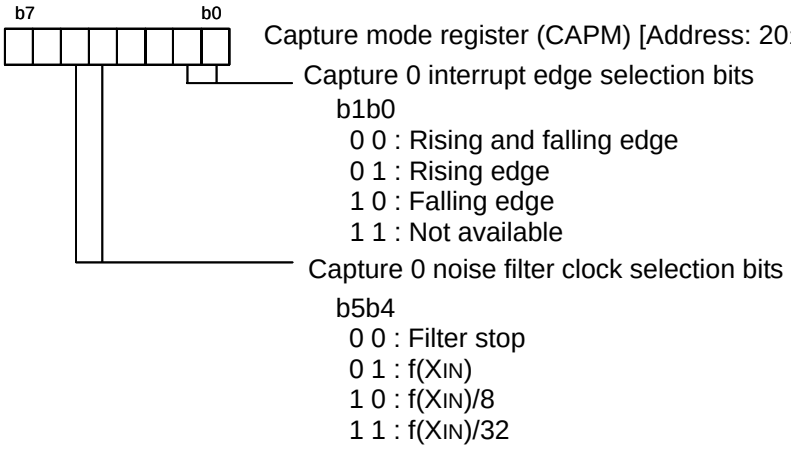
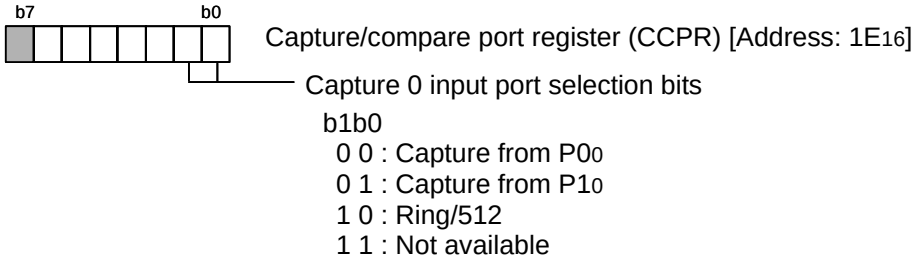


Figure 1 Setting method for input capture (1)

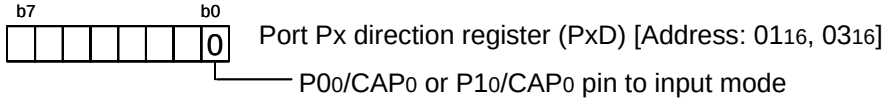
Process 6: Set capture mode register.



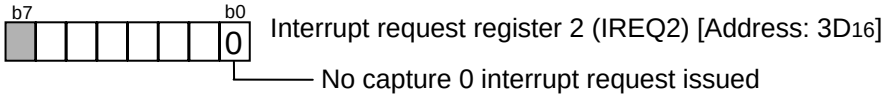
Process 7: Set capture 0 input port selection bits.



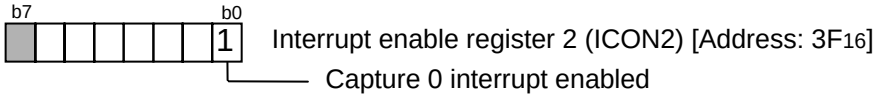
Process 8: Set capture 0 input port to input mode.



Process 9: In order not to execute the unrequested interrupt processing, set “0” (no request) to the capture 0 interrupt request bit.



Process 10: When using the capture interrupt, set “1” (interrupt enabled) to the capture 0 interrupt enable bit.



Process 11: Start counting timer A.

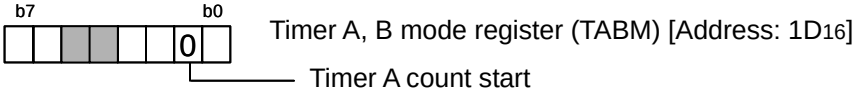


Figure 2 Setting method for input capture (2)

The capture input circuit retains the count value of selected timer to the capture latch when external trigger is input. The timer count value is retained to the capture latch x0 when rising edge of the external trigger is input and is retained to the capture latch x1 when falling edge of the external trigger is input.

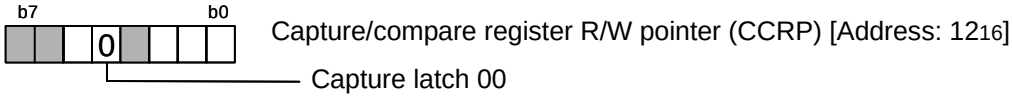
The count value of timer can be retained by software by capture y (y = 00, 01, 10, 11) software trigger bit too.
When “1” is set to this bit, count value of timer is retained to the corresponded capture latch.

The latest status of capture latch can be confirmed by reading of the capture x status bit.
This bit indicates the capture latch (x0 or x1) which latest data is in.

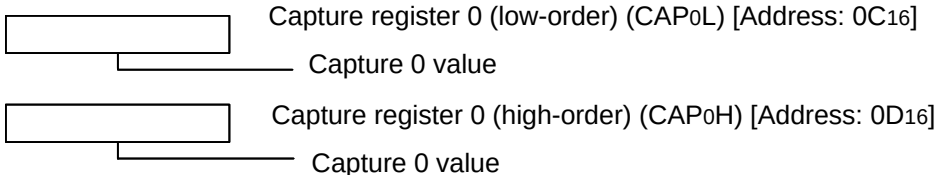
Capture 0 interrupt occurs when CAP_0 pin captures rising or falling edge.
Read out the capture 0 value as follows after capture interrupt occurs;

<When rising edge is selected as the capture 0 interrupt edge>

Process a: Set “0” (capture latch 00 selected) to capture register R/W pointer .

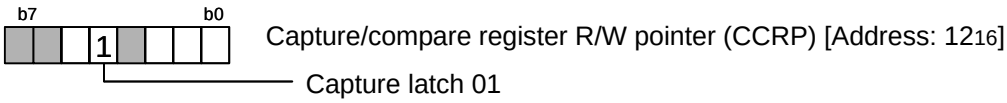


Process b: Read out capture 0 value from capture latch 00.



<When falling edge is selected as the capture 0 interrupt edge>

Process c: Set “1” (capture latch 01 selected) to capture register R/W pointer .



Process d: Read out capture 0 value from capture latch 01.

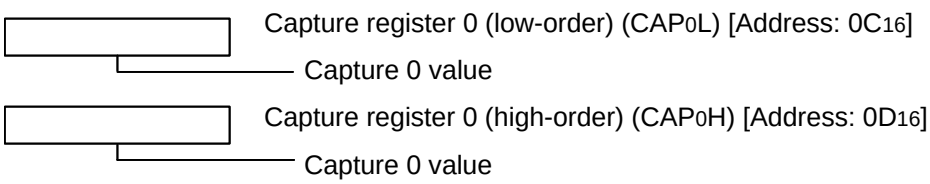


Figure 3 Setting method for input capture (3)

4. Application Example of Input Capture

Outline

The waveform generated in the timer X pulse output mode is input to the input capture 0 input pin (P00/CAP0) and its pulse width is measured.

Specifications

The square waveform that clock f(XIN) = 1.8432 MHz is divided to 1.00 Hz is output from P14/CNTR0 pin.

The output waveform is input to P00/CAP0 pin and its "H" pulse width is measured by the input capture.

Reading out the capture latch register and the calculation of pulse width are performed in the capture 0 interrupt processing routine (falling edge trigger).

4.1 Peripheral circuit example

Figure 4 shows the peripheral circuit example.

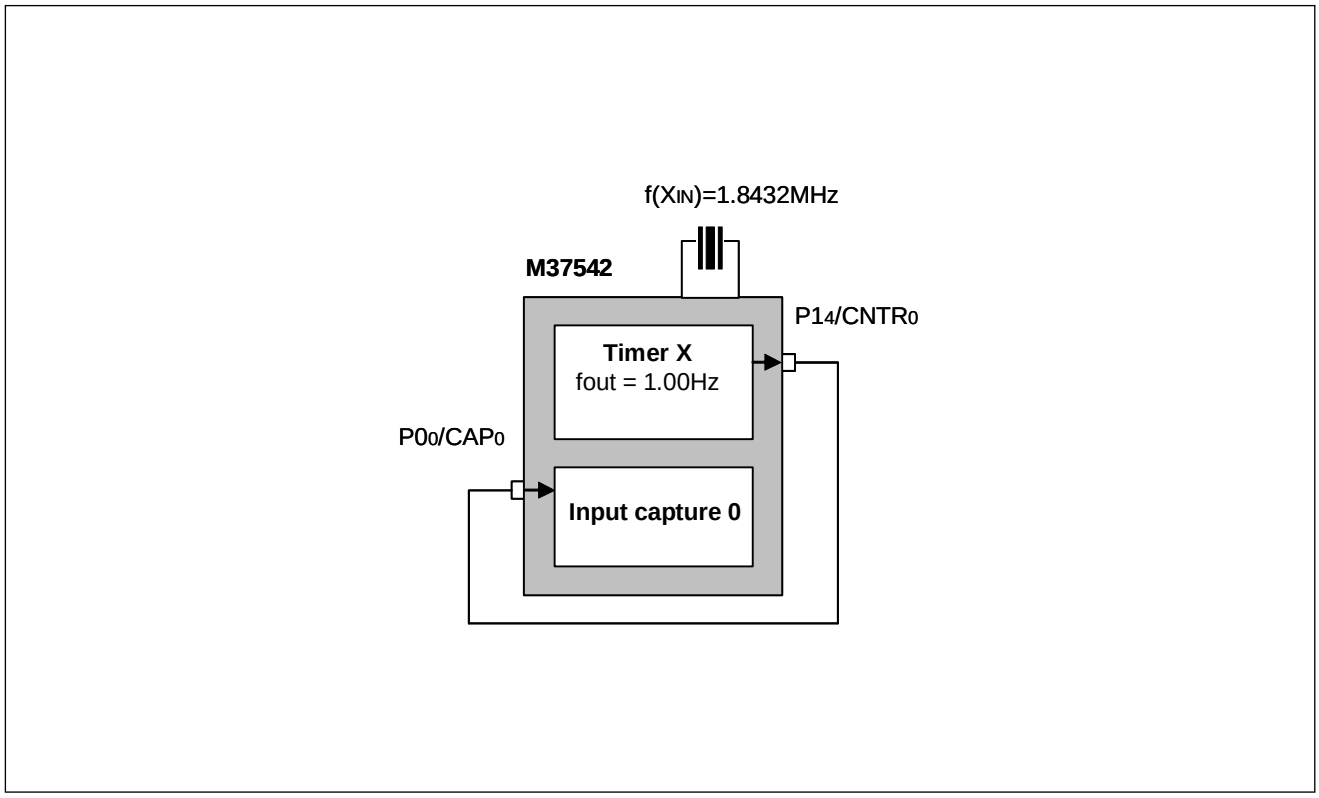
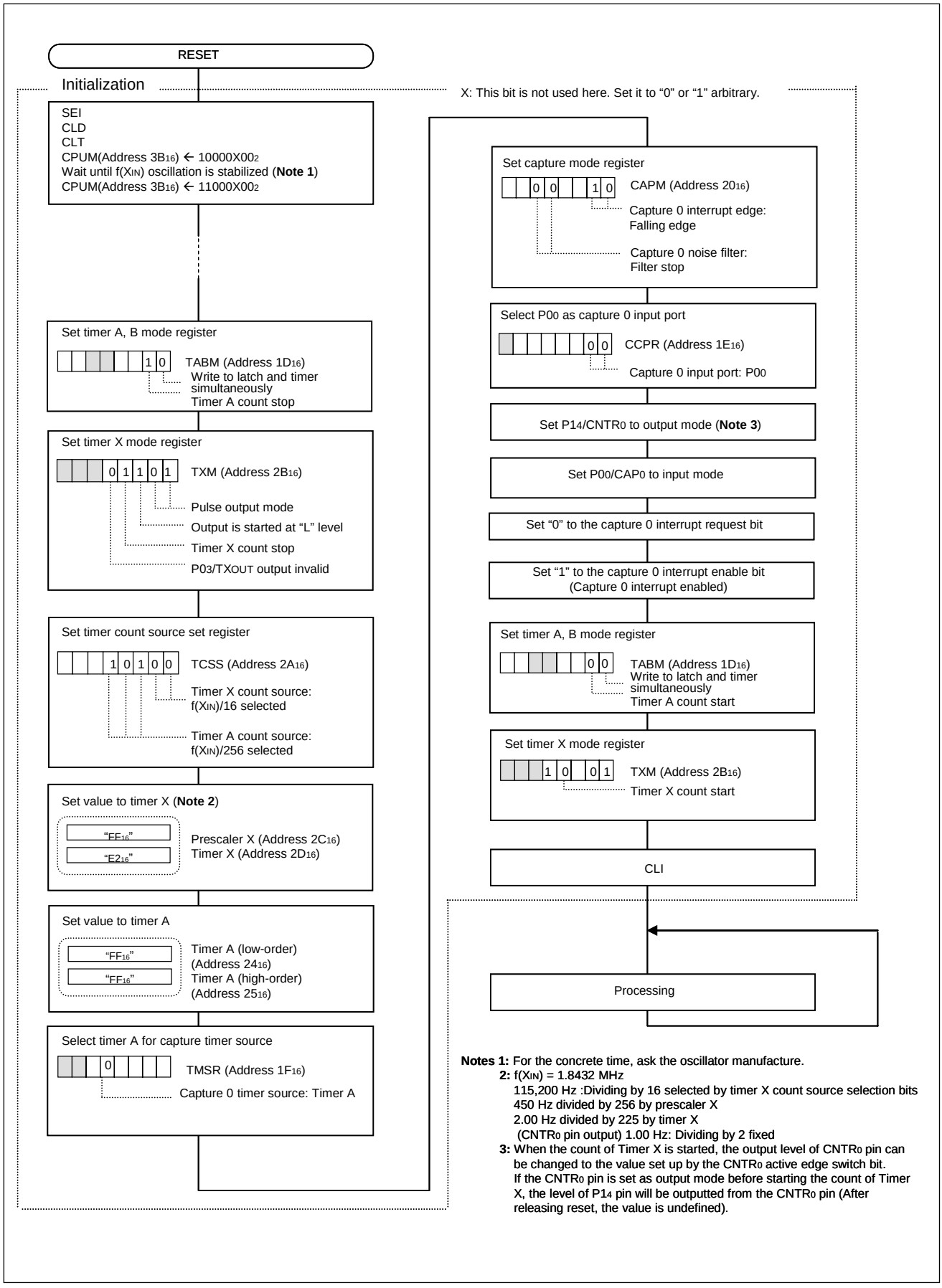


Figure 4 Peripheral circuit example

4.2 Example of control procedure

Figure 5 and Figure 6 shows the circuit example.



Notes 1: For the concrete time, ask the oscillator manufacture.

2: f(XIN) = 1.8432 MHz
115,200 Hz :Dividing by 16 selected by timer X count source selection bits
450 Hz divided by 256 by prescaler X
2.00 Hz divided by 225 by timer X
(CNTR0 pin output) 1.00 Hz: Dividing by 2 fixed

3: When the count of Timer X is started, the output level of CNTR0 pin can be changed to the value set up by the CNTR0 active edge switch bit.
If the CNTR0 pin is set as output mode before starting the count of Timer X, the level of P14 pin will be outputted from the CNTR0 pin (After releasing reset, the value is undefined).

Figure 5 Example of control procedure (1)

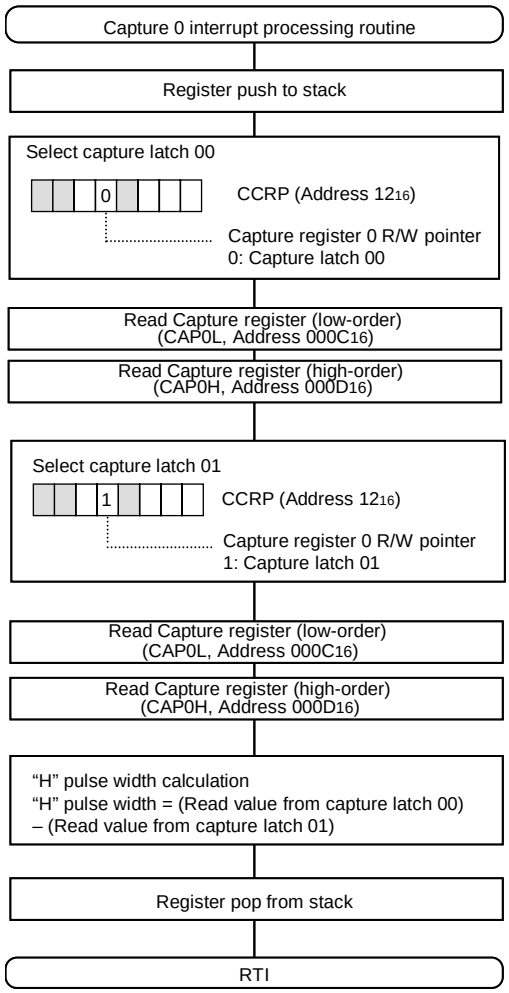


Figure 6 Example of control procedure (2)

5. Reference Document

Data Sheet
7542 Group Data sheet
Download the latest version from the Renesas Technology website.

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jun.18.03	—	First edition issued
2.00	Jul.01.04	All pages	Words standardized
		6	Fig.5: Note 2 revised.
3.00	Aug.29.06	3	Interrupt setting of timer A deleted.

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