IDT's PES12N3/PES12NT3 PCI Express® Switch Performance with External Cabling

Application Note AN-533

Notes

By Derek Huang

Overview

With the accelerating adoption of PCI Express® (PCIe®) as the primary I/O expansion and system interconnect switching protocol in demanding server, storage, communications and embedded applications, system architects and designers often seek solutions to extend and drive the PCIe protocol over distances greater than those supported by existing backplane trace connectivity. External cabling and connectors can be used to address these market segments. The PCI Special Interest Group (PCI-SIG®) Cabling Working Group (CWG) has defined a specification for external cabling used in PCIe systems. This application note introduces the PCI External Cabling Specification and discuss the performance of IDT's 89HPES12N3 (PES12N3) and 89HPES12NT3 (PES12NT3) 12-lane, 3-port PCI Express switch, as it relates to this specification at 2.5 Gb/s.

Introduction

The PCI-SIG Cabling Working Group has defined a low-cost connector interface to meet the requirements for the first-generation (2.5 Gb/s). The specification focuses on the following areas:

- *Standard cable connectors (x1, x4, x8, and x16)*
- *Copper cabling attributes and electrical characteristics*
- *Connector retention*
- *Identification and labeling*

Revision 1.0 of the specification, released in February, 2007 sought to meet the following objectives:

- *Define PCI Express external cables and associated connectors*
- *Support PCI Express data rates of 2.5 GT/s*
- *Support standard PCI Express 1.1 silicon*
- *Allow for future scalability*
- *Maximize cable interoperability for user flexibility*
- *Enable Hot-plug as a native function*
- *Allow revolutionary partitioning of the PC architecture*
- *Allow for upgradeability*

The CWG has also identified several PCI Express Cabling Usage Models as follows:

- *Expansion I/O*
- *Split-system (disaggregate) desktop*
- *Tethered docking for mobile platforms*
- *External graphics controllers*
- *Communication equipment*
- *Printers and other office equipment*
- *Test and measurement equipment*
- *Embedded applications*

PCI Express external cabling allows flexibility in interconnecting systems and extends the reach of the protocol. In contrast to the traditional "inside the box" system architecture, external cabling can connect the motherboard to add-in cards or a chassis located many feet away.

Figure 1 is an example of a single chassis containing a CPU, storage, video card, and I/O devices connecting the endpoint cards. PCIe cables allow the endpoints to be located outside the chassis. Optional PCI Express repeaters can be added to the transmit and receive paths to further extend the reach. An example of this type of application, shown in Figure 2, would be a blade server using PCI Express cables to connect to racks of hard drives.

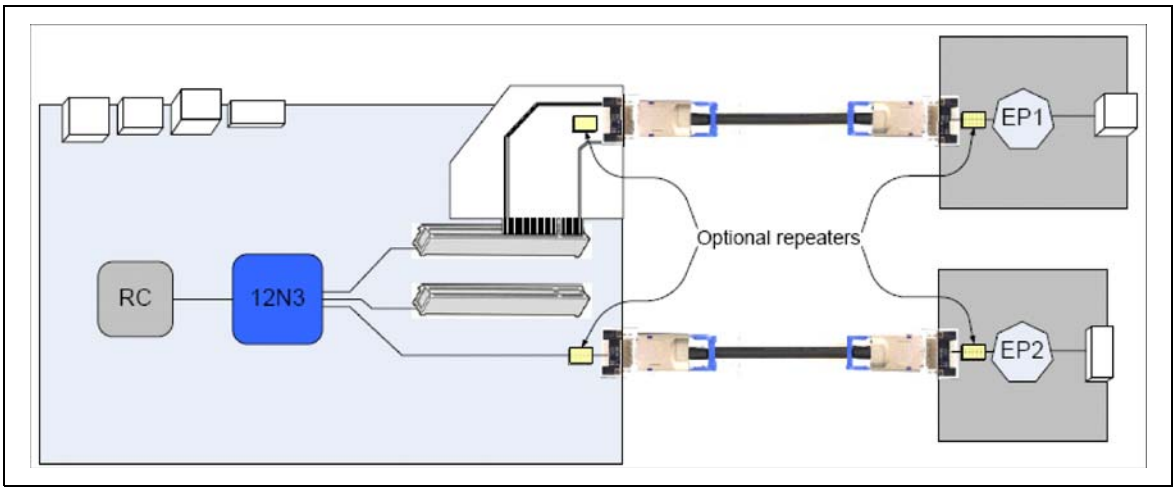

Figure 1 Chassis-to-Board Configuration

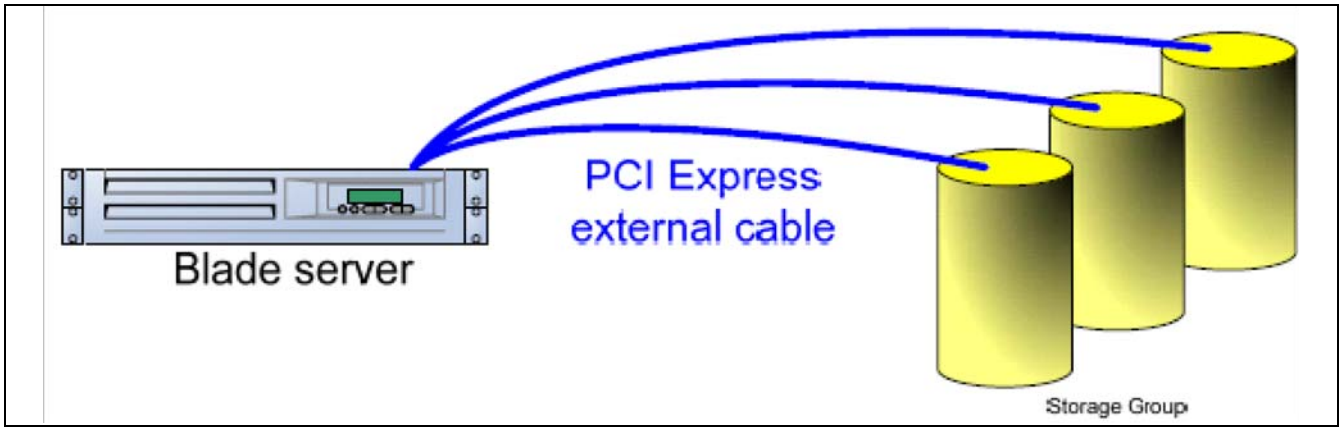

Figure 2 Example of Blade Server Connecting to Storage Group via PCI Express External Cable

Figure 3 is an example of a host computer with a limited PCIe bus (such as a notebook computer) using PCIe cables for additional connectivity. The box in the middle represents a generic docking station that provides additional I/O ports such as IEEE 1394 (FireWire), SATA, USB, Ethernet, KVM, and a monitor. By using PCI Express external cabling, third-party docking stations can be designed to work with any computer.

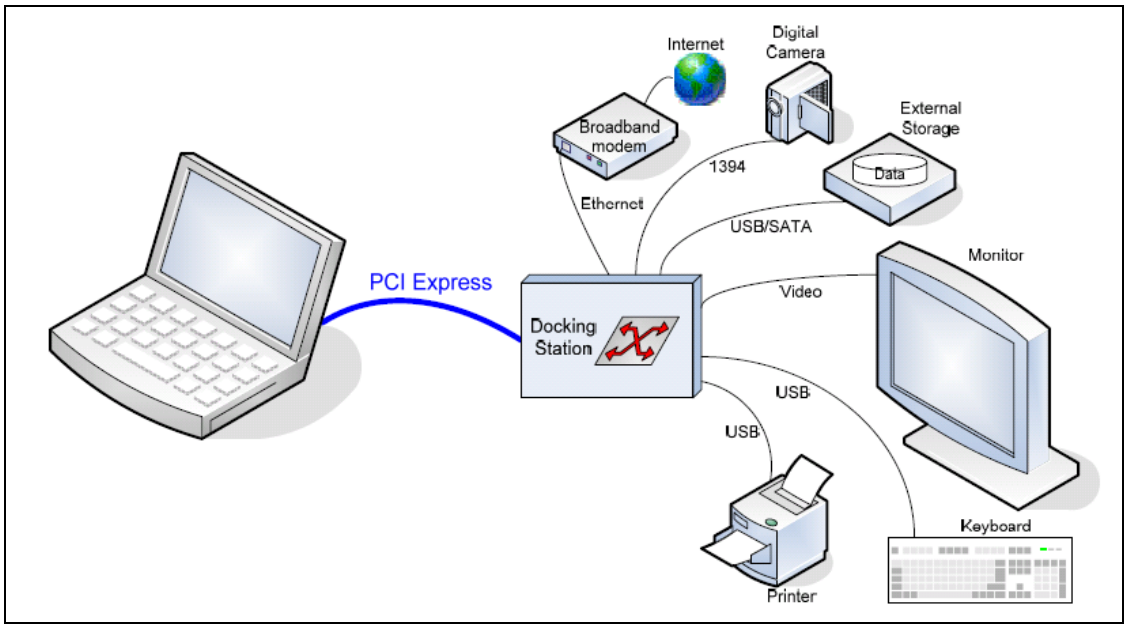

Figure 3 Example of Application Utilizing PCI Express Cable Connecting a Notebook to an I/O Expansion Docking Station

Figure 4 is a summary of the minimum sensitivity for the Subsystem's Receiver path compliance published by the PCI-SIG. It can be used as a reference to compare against the test results presented later in this document.

Parameter	Value
Vrx_A	≥ 208 mV
Vrx_A_d	≥ 192 mV
Trx_A @ BER 10^{-12}	≥ 234 ps
Trx_A @ 10^6 Samples	≥ 247 ps

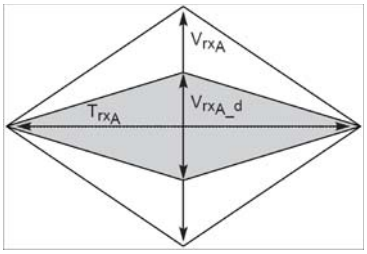

Figure 4 Receiver Path Compliance Eye Requirements and Eye Diagram (from Section 3.3.2 of the External Cabling Specification Rev. 1.0)

The remainder of this application note deals with the signal integrity of serial data links based on cable length and quality.

Tests and Measurements with PES12N3/PES12NT3

The eye diagram measurements that are reported in the following sections were performed using the PES12N3/PES12NT3 PCI Express Switch with various lengths and types of cable. In all conducted tests, the compliance pattern (defined by PCI Express 1.1 base specification) is transmitted from the PES12N3/PES12NT3 and the differential signal measurement is taken at the SMA connectors on the PCI-SIG's Compliance Base Board. The PES12N3/PES12NT3 can be configured to increase the transmitter output in order to drive longer lengths of cable without introducing a repeater in the path.

Test 1: No Cable

The transmit eye diagram measurements for test 1 were made without a cable to serve as a reference for later measurements. The test setup is shown in Figure 5.

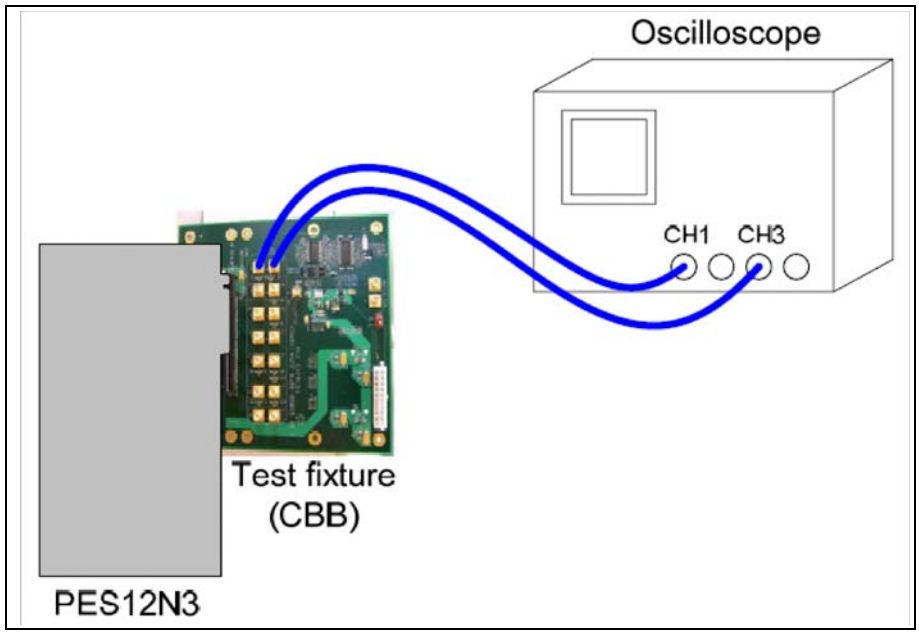

Figure 5 Test 1 Setup

The following equipment was used in this test:

- *Oscilloscope, TDS7704B, 6 GHz system BW for 2.5 Gb/s SerDes measurement*
  Includes Tektronix's RT-Eye software with PCI Express Compliance module option (1.1 base specification eye mask selected)
  Uses two SMA TekConnect Adapters and one pair matched SMA cables as probing option for transmitter testing.
- *Compliance Base Board (CBB) from PCI-SIG which provides breakout from transmitter to differential SMA connectors and generates a reference clock to the PES12N3/PES12NT3 board*
- *IDT PES12N3/PES12NT3 Evaluation Board, plugged directly into the CBB slot connector.*

The compliance test pattern transmitted by the SerDes is measured by connecting the TCA-SMA inputs using SMA cables (Ch1 and Ch3). An ideal reference clock and a 12V power supply are sourced by the CBB and transmitted to the PES12N3/PES12NT3 Evaluation Board via a ribbon cable. The compliance test results were measured using an oscilloscope and the CBB test fixture. The Tektronix RT-Eye software with PCI Express Compliance Module option was used to generate the eye diagrams and all measurement results.

The PES12N3/PES12NT3 SerDes default transmit settings of -3.35dB de-emphasis, scale factor of 1, 20mA nominal drive current, and nominal Tx termination value of 50 ohms were used. The eye diagrams appear in Figure 6 and the measurements are listed in Table 1.

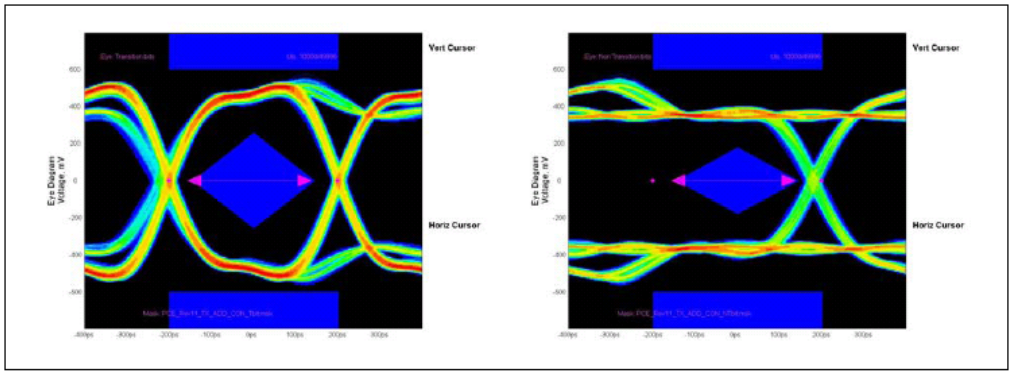

Figure 6 Transmitter Eye Diagrams of PES12N3/PES12NT3 on CBB (no cable) with Default Tx Setting (-3.35dB de-emphasis, Scale Factor of 1, 20mA Nominal Drive Current, Nominal tx Termination Value of 50 ohms)

Measurement		Value
Eye Width	Min	0.8061 UI
Eye H: Non-Tr Bits	Min	625.94 mV
Eye H: Trans Bits	Min	813.38 mV
TIE Jitter	Max	0.0750 UI
	Min	-0.1189 UI
Jitter: Total (TJ)	Max	0.2680 UI
Diff Peak Voltage	Max	1.1384 V

Table 1 Differential Transmitter (Tx) Output Measurement with No External Cable

Test 2: Flex (Ribbon) Cable

Test 2 uses a flex (ribbon) cable of lengths 0.5, 1, and 2 meters. The test setup is shown in Figure 7.

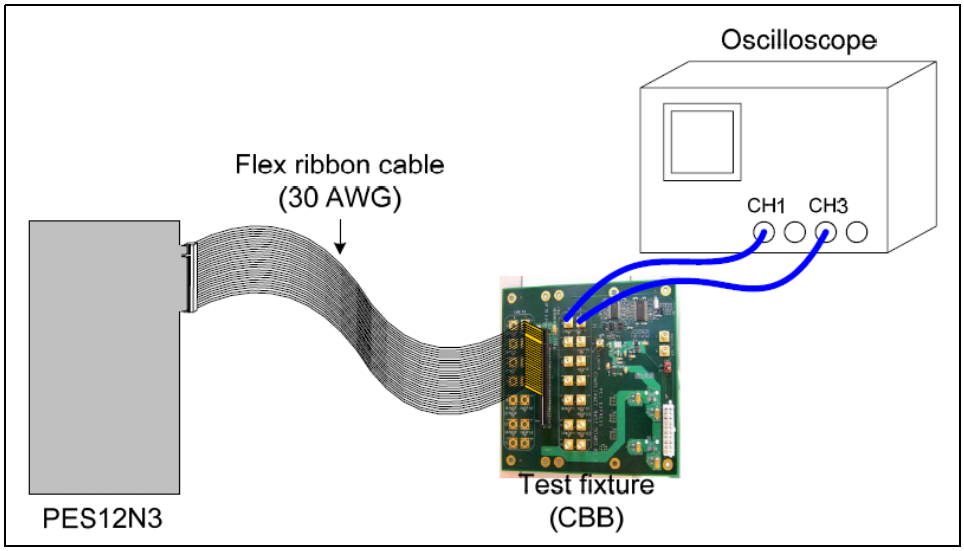

Figure 7 Test 2 Setup

The following equipment was used in this test:

- *Oscilloscope, TDS7704B, 6 GHz system BW for 2.5 Gb/s SerDes measurement*
  Includes Tektronix's RT-Eye software with PCI Express Compliance module option (1.1 base specification eye mask selected)
  Uses two SMA TekConnect Adapters and one pair matched SMA cables as probing option for transmitter/receiver testing
- *Compliance Base Board (CBB) from PCI-SIG which provides a breakout from transmitter to differential SMA connectors and generates a reference clock to the PES12N3/PES12NT3 board*
- *IDT PES12N3/PES12NT3 Evaluation Board*
- *30 AWG ribbon cables.*

The PES12N3/PES12NT3 SerDes default transmit settings of -3.35dB de-emphasis, scale factor of 1, 20mA nominal drive current, and nominal Tx termination value of 50 ohms are used. The PES12N3/PES12NT3 transmitter with the default setting demonstrates an ability to drive cable length up to 2 meters of flex cable (the compliance test failed at 2.5 meters) as shown in Figure 8. The eye measurement associated with each length is listed in Table 2.

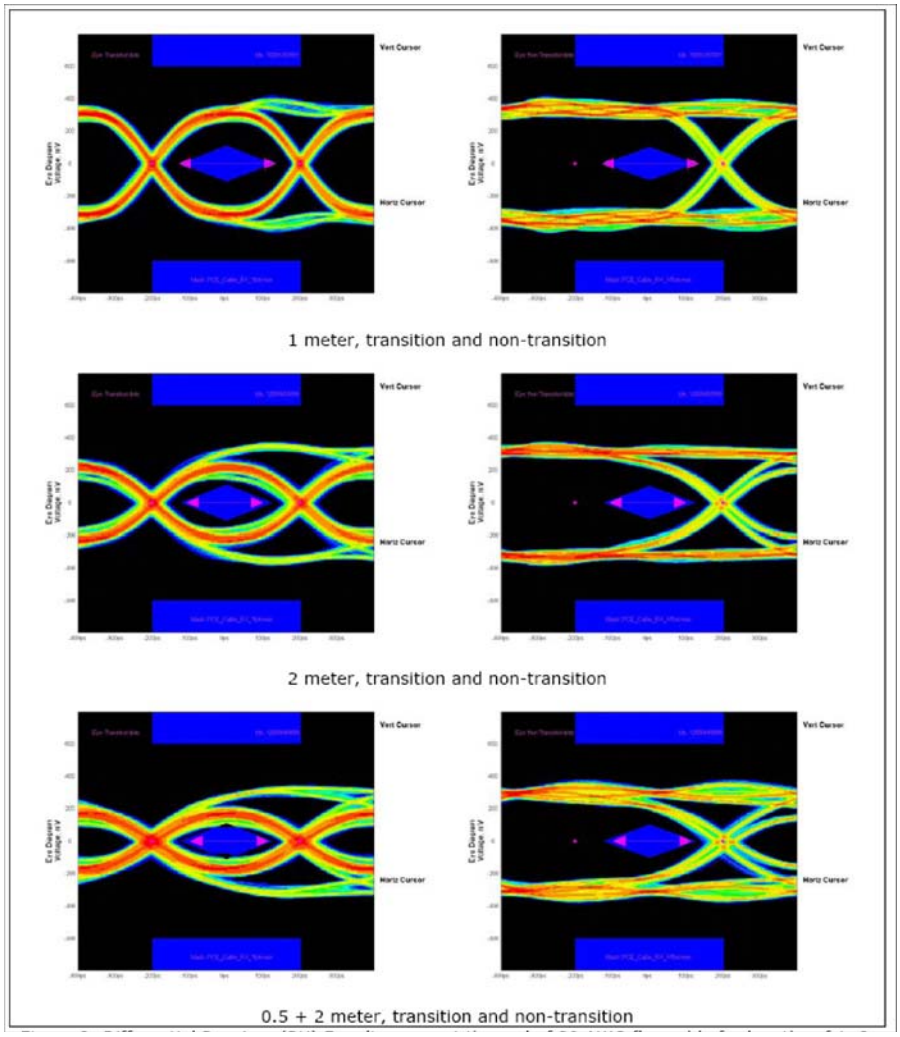

Figure 8 Differential Receiver (Rx) Eye Diagrams at the End of 30 AWG Flex Cable for Lengths of 1, 2 and 2.5 Meters with Default Tx Setting (-3.35dB De-emphasis, Scale Factor of 1, 20mA Nominal Drive Current, Nominal Tx Termination Value of 50 ohms)

Cable Length		No Cable	1m	2m	2.5m
Eye Width	Min	0.8061 UI	0.8067 UI	0.7274 UI	0.6760 UI
Eye H: Non-Tr Bits	Min	625.94 mV	545.81 mV	394.73 mV	388.30 mV
Eye H: Trans Bits	Min	813.38 mV	508.79 mV	283.06 mV	164.68 mV
TIE Jitter	Max	0.0750 UI	0.1019 UI	0.1146 UI	0.1772 UI
	Min	-0.1189 UI	-0.0914 UI	-0.1579 UI	-0.1468 UI
Jitter: Total (TJ)	Max	0.2680 UI	0.3446 UI	0.4833 UI	0.4715 UI
Diff Peak Voltage	Max	1.1384 V	842.80 mV	759.60 mV	756.68 mV

Table 2 Differential Receiver (Rx) Input Measurement for 30 AWG Flex Cable lengths of 1, 2, and 2.5 Meters. Differential Transmitter (Tx) Output Values are Included in the First Column to Show the Loss when Using an External Cable

Optimized Transmitter Setting for 30 AWG Flex Cable

The PES12N3/PES12NT3 transmitters can be configured to increase the driver output voltage by changing the drive current and de-emphasis/ equalization levels. Figure 9 shows optimized transmitter settings, which serve to open the eye opening for transition bits at the end of a 2 meter and 2.5 meter (interconnecting 0.5 and 2 meter cables) flex cable.

With a 2 meter cable, the resulting transition eye width is reduced by roughly 3% while the eye height is improved by about 21% for non-transition bits and 5% for transition bits. Total jitter increases by approximately 5% and differential peak voltage increases by 36%.

The 2.5 meter cable measurement used a 0.5 and a 2 meter cable. Eye height is reduced by 5% for non-transition bits but is increased by 54% for transition bits. Eye width is reduced by 3%. Total jitter is reduced by 4% and differential peak voltage is increased by 14%. The measured data is shown in Table 3.

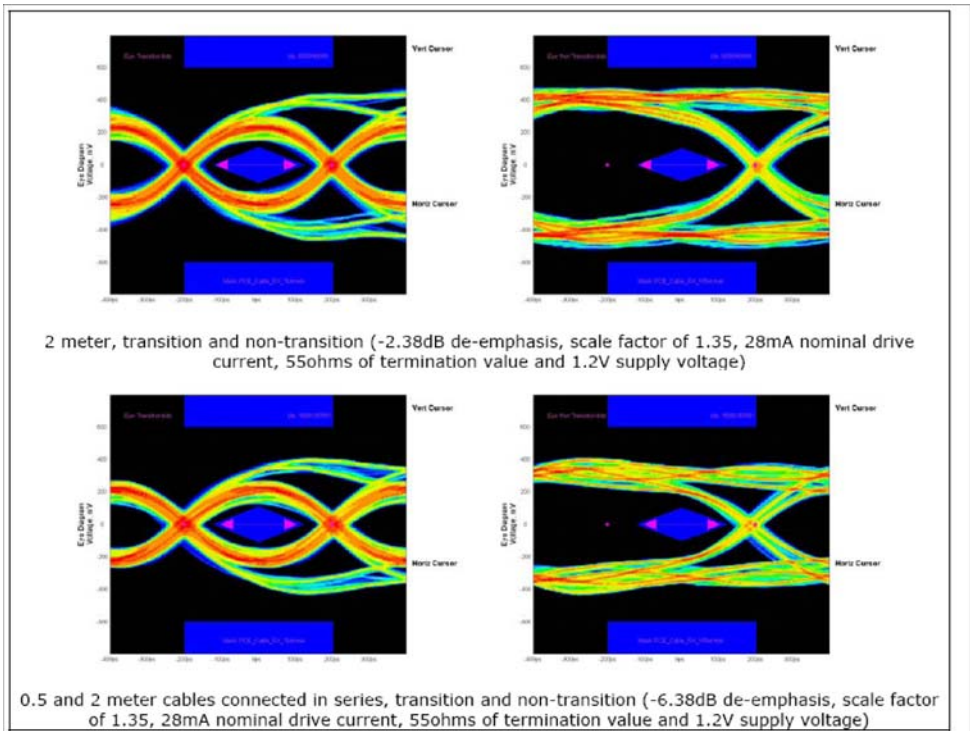

Figure 9 Differential Receiver (Rx) Eye Diagrams at the End of 30 AWG 2 and 2.5 Meters Ribbon Cables with Optimized Tx Settings

Cable Length		2m	2.5m
Eye Width	Min	0.7069 UI	0.6586 UI
Eye H: Non-Tr Bits	Min	476.34 mV	369.98 mV
Eye H: Trans Bits	Min	296.19 mV	253.50 mV
TIE Jitter	Max	0.1752 UI	0.1597 UI
	Min	-0.1565 UI	-0.1817 UI
Jitter: Total (TJ)	Max	0.4606 UI	0.4898 UI
Diff Peak Voltage	Max	1.0353 V	861.20 mV

Table 3 Differential Receiver (Rx) Input Measurement for 30 AWG Cable Lengths of 2 and 2.5 Meters with Optimized Tx Settings

Test 3: Infiniband Cable

Test 3 uses Infiniband cables of 0.5, 3, 7, 10, and 15 meters. The test setup is shown in Figure 10.

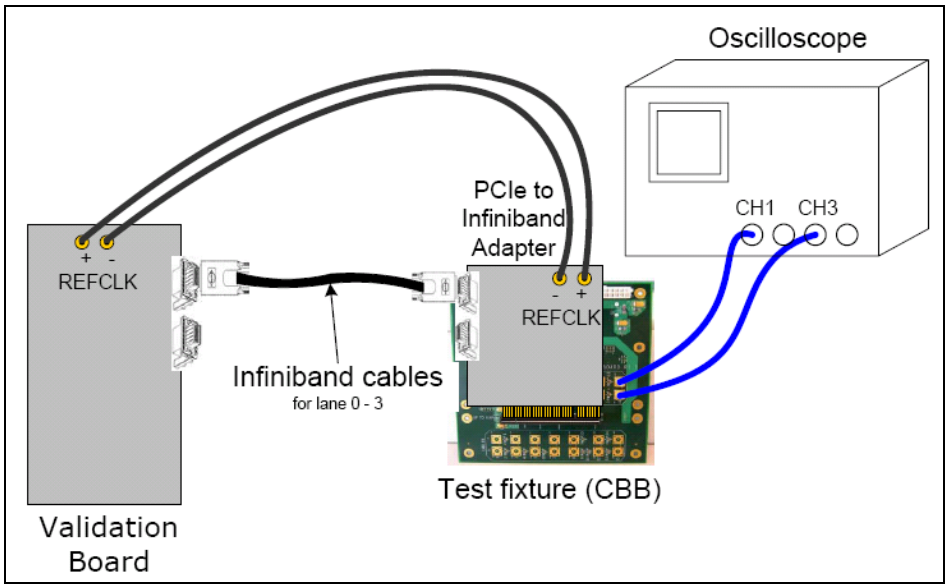

Figure 10 Test 3 Setup

The following equipment was used in this test:

- *Oscilloscope, TDS7704B, 6 GHz system BW for 2.5 Gb/s SerDes measurement*
  Includes Tektronix's RT-Eye software with PCI Express Compliance module option (1.1 base specification eye mask selected)
  Uses two SMA TekConnect Adapters and one pair matched SMA cables as probing option for transmitter/receiver testing
- *Compliance Base Board (CBB) from PCI-SIG which provides breakout from transmitter to differential SMA connectors and generates a reference clock to PES12N3/PES12NT3 board*
- *PCI Express to Infiniband Adaptor Board*
- *IDT PES12N3/PES12NT3 Validation Board*
- *Infiniband cables for data*
- *SMA cables for reference clock.*

The PES12N3/PES12NT3 SerDes default transmit settings of -3.35dB de-emphasis, scale factor of 1, 20mA nominal drive current, and nominal Tx termination value of 50 ohms are used. The eye diagrams based on a 0.5 meter Infiniband cable are shown in Figure 11 and the measurements are listed in Table 4.

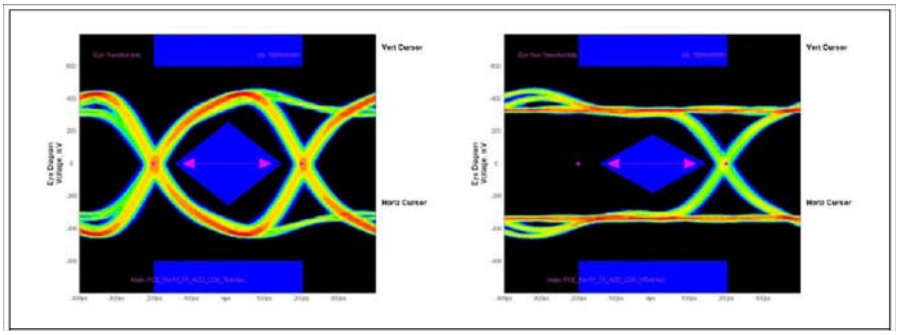

Figure 11 Transmit Eye Diagrams of PES12N3/PES12NT3 Through a 0.5 Meter Infiniband Cable with Default Tx Setting (-3.35dB De-emphasis, Scale Factor of 1, 20mA Nominal Drive Current, Nominal Tx Termination Value of 50 ohms)

Measurement Statistic		Value
Eye Width	Min	0.7848 UI
Eye H: Non-Tr Bits	Min	577.45 mV
Eye H: Trans Bits	Min	645.60 mV
TIE Jitter	Max	0.0937 UI
	Min	-0.1215 UI
Jitter: Total (TJ)	Max	0.4018 UI
Diff Peak Voltage	Max	940.80 mV

Table 4 Differential Transmitter (Tx) Output Measurement at the End of a 0.5 Meter Infiniband Cable

The eye patterns for 3, 7, and 10 meter Infiniband cables are shown in Figure 12 and the measurements listed in Table 5. The Infiniband cables have a better shielding and heavier gauge than the flex cables used in Test 2. As expected, the Infiniband cable is able to carry PCI Express signals at a longer cable run. The results show that the compliance test passed using a 7 meter cable but failed using a 10 meter cable.

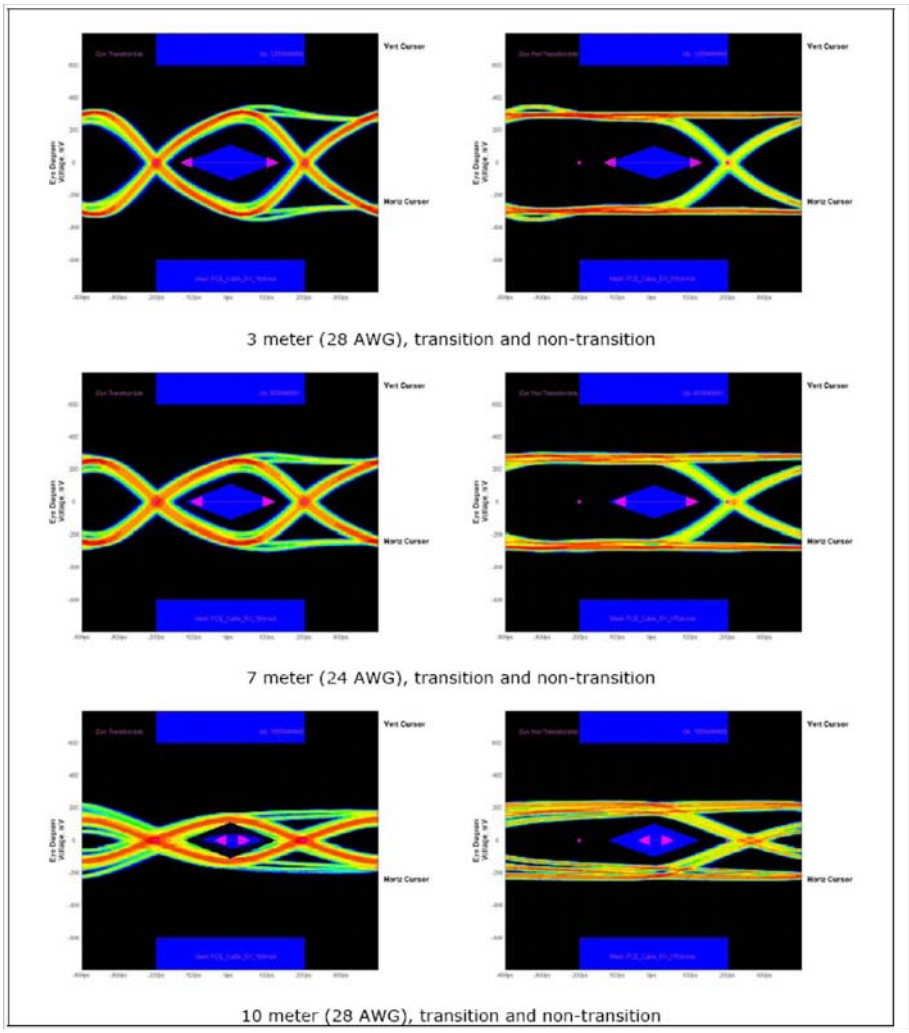

Figure 12 Differential Receiver (Rx) Eye Diagrams at the End of an Infiniband Cable for Lengths of 3, 7, and 10 Meters with Default Tx Setting (-3.35dB De-emphasis, Scale Factor of 1, 20mA Nominal Drive Current, Nominal Tx Termination Value of 50 ohms)

Cable Length		0.5m(Tx)	3m	7m	10m
Eye Width	Min	0.7965 UI	0.7240 UI	0.7779 UI	0.4409 UI
Eye H: Non-Tr Bits	Min	561.38 mV	436.82 mV	489.71 mV	293.43 mV
Eye H: Trans Bits	Min	629.95 mV	328.08 mV	443.82 mV	86.456 mV
TIE Jitter	Max	0.1124 UI	0.1393 UI	0.1303 UI	0.3131 UI
	Min	-0.0911 UI	-0.1367 UI	-0.0917 UI	-0.2460 UI
Jitter: Total (TJ)	Max	0.3574 UI	0.4290 UI	0.3374 UI	0.7589 UI
Diff Peak Voltage	Max	935.60 mV	623.60 mV	727.60 mV	496.40 mV

Table 5 Differential Receiver (Rx) Input Measurement for Cable Lengths of 3, 7, and 10 Meters. Differential Transmitter (Tx) Output Values for .5 Meter Cable Length in the First Column to Show the Loss of Using a Longer Cable Length.

Optimized Transmitter Settings

The PES12N3/PES12NT3 transmitters can be configured to increase the driver output voltage by changing the drive current and de-emphasis/equalization levels. Figure 13 shows optimized transmitter settings, which serve to open the eye opening for transition bits at the end of 7, 10, and 15 meters of Infiniband cable.

For the 7 meter cable, the resulting transition eye width and height is improved by roughly 2% and 7% respectively. The eye height for non-transition bits is reduced by about 8%. Total jitter increases by approximately 8% and differential peak voltage increases by 2%.

The transmitter driver output is maximized for 10 and 15 meters of Infiniband cables. As a result, the 10 meter cable passed the compliance test by significantly improving the eye width and height for transition and non-transition bits by 63% and 158% respectively. Total jitter is reduced by 44% and differential peak voltage is reduced by 12%. The 15 meter cable passed the non-transition compliance test but did not pass the transition compliance test. Table 6 compares the statistics among various lengths and transmitter settings.

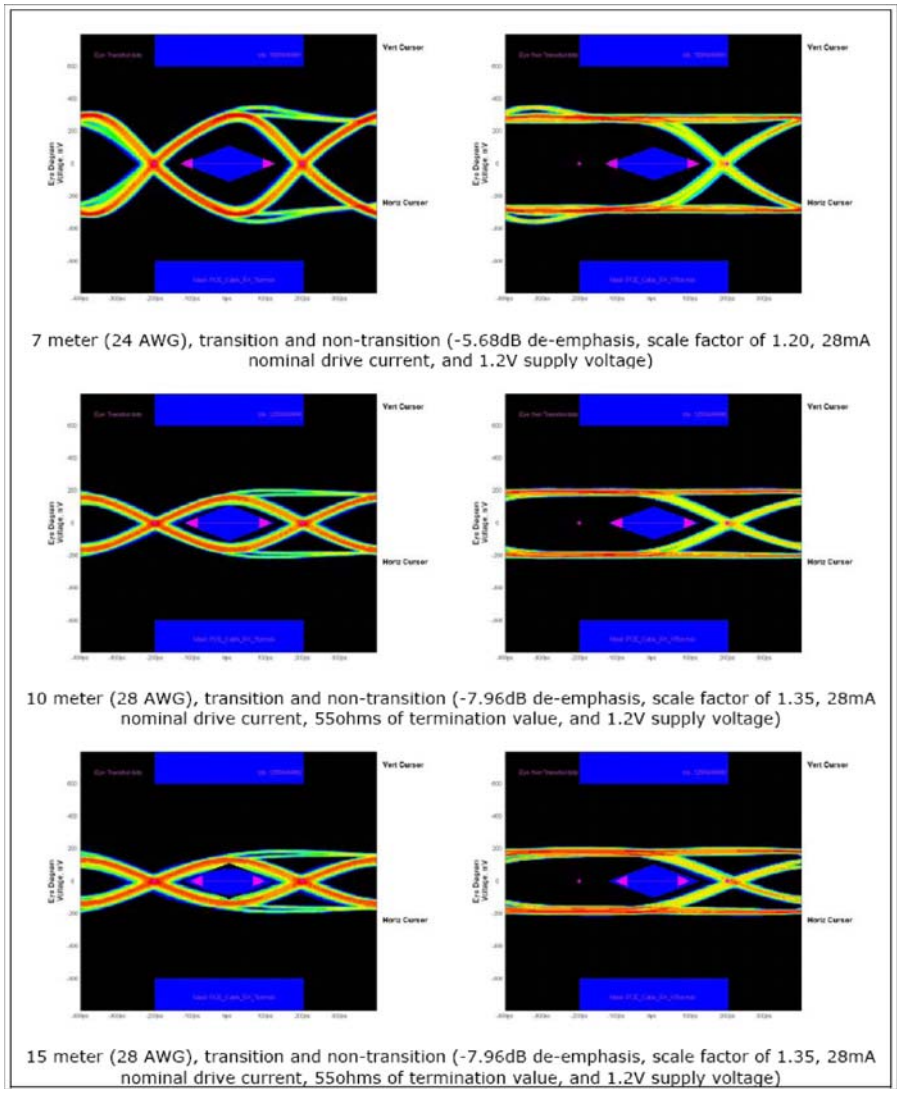

Figure 13 Differential Receiver (Rx) Eye Diagrams at the End of Infiniband 7, 10, and 15 Meter Cables with Optimized Tx Settings

Cable Length		7m	10m	15m
Eye Width	Min	0.7952 UI	0.7209 UI	0.6385 UI
Eye H: Non-Tr Bits	Min	449.60 mV	293.19 mV	258.27 mV
Eye H: Trans Bits	Min	477.35 mV	223.32 mV	160.8 mV
TIE Jitter	Max	0.0898 UI	0.1451 UI	0.1799 UI
	Min	-0.1150 UI	-0.1340 UI	-0.1816 UI
Jitter: Total (TJ)	Max	0.3653 UI	0.4230 UI	0.5008 UI
Diff Peak Voltage	Max	743.20 mV	436.00 mV	428.00 mV

Table 6 Differential Receiver (Rx) Input Measurement for Infiniband Cable Lengths of 7, 10, and 15 Meters

PCI Express Reference Clock over Cable

The reference clock is a critical aspect of the design since it is used as input to a transceiver containing a PLL (10X or 25X) to generate higher frequencies for transmitting and receiving data at high rates. It is critical for the reference clock to have a low jitter level to achieve system jitter compliance. For measuring the phase jitter of the PCI Express Reference Clock, the test shown in Figure 14 uses the PCI-SIG Compliance Load Board (CLB) with the PES12N3/PES12NT3. The clock period trend is measured with a Tektronix TDS7704B real time oscilloscope and differential probe, P7350, connected to one channel. The differential signal is sampled at a rate of 20 GS/s and 16 Meg of record length for the proper bit error rate (BER). Data was captured by the Tektronix TDS-JIT3 Advanced Jitter software package and saved in a file for post-processing with PCI-SIG's PCI Express Clock Phase Jitter Test Software, ClockTool version 1.0, to calculate the reference clock phase jitter.

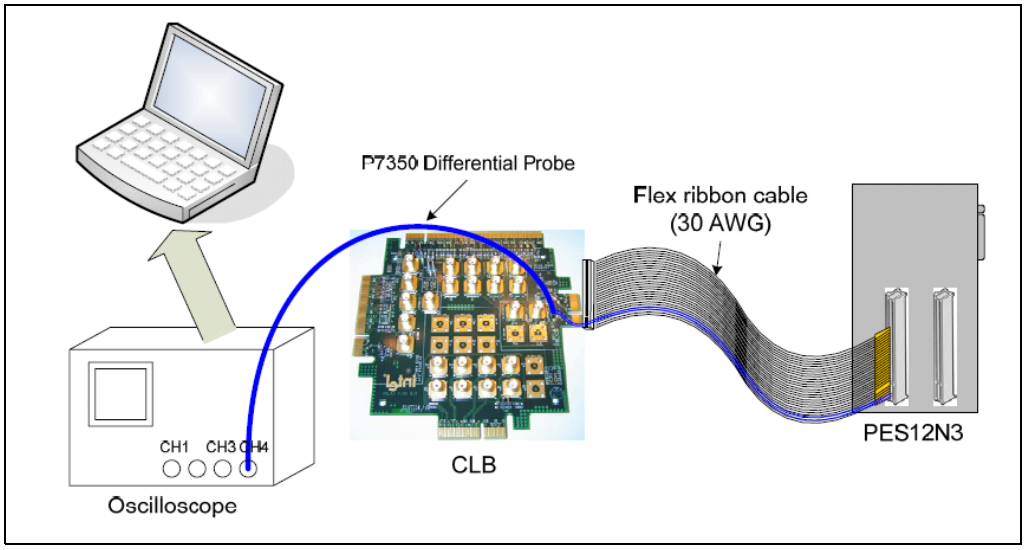

Figure 14 Reference Clock Jitter Test Configuration

The PCI Express Card Electromechanical Specification Rev. 1.1 specifies a maximum allowed peak-peak phase jitter value of 86 ps at a Bit Error Ratio of 10^{-6}. The experiment was first performed at the connector on one of the downstream ports to validate the jitter level from the onboard oscillator and clock buffer. The PES12N3/PES12NT3 downstream port reference clock jitter was measured at 59.63ps. A flex cable was then added, and jitter was measured again. As shown in Table 7, total jitter level falls below the maximum value of 86ps for cable lengths up to 2 meters.

Cable Length	TJ @ 6 BER (ps)
No Cable (Slot)	59.63
0.5m	61.80
1m	70.36
2m	74.52

Table 7 Clock Jitter Tool Post-processing Results

Conclusion

The PES12N3/PES12NT3 transmitter with default settings is able to drive external cables up to 7 meters for Infiniband and 2 meters for flex cable, while still meeting the receiver side requirements of the External Cabling Specification. In addition, PCI Express reference clock signals over flex cable up to 2 meters in length meets PCI-SIG's Jitter requirements. The PES12N3/PES12NT3 transmitter can also be configured to optimize key signal characteristics, such as eye width, eye height, and jitter, which further improves the reach — up to 10 meters for Infiniband cables and up to 2.5 meters for flex cables. As a result, the PES12N3/PES12NT3 transmitters allow inexpensive external cabling, without the need for repeaters, to be used in applications where chassis-to-chassis, rack-to-rack, and even room-to-room connectivity are desired, resulting in lower system costs.

Note: Although the PES12N3/PES12NT3 is capable of driving PCI Express signals over cables up to certain lengths (depending on the cable type and quality), the actual cable length used in a system will be limited by the following factors — cable assembly, optional repeaters, subsystem loss, and jitter budget — which must meet the PCI Express parameters (compliance eye diagrams and reference clock jitter) defined by PCI Express Base Specification 1.1, Card Electromechanical Specification 1.1, and External Cabling Specification 1.0.

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