Hot-Plug Implementation in the IDT 89HPES12N3 12-lane, 3-port PCI Express® Switch

Application Note AN-509

Notes

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Introduction

The PCI Express architecture is designed to natively support both hot-add and hot-removal ("hot-plug") of adapters and provides a "toolbox" of mechanisms that allow different user/operator models to be supported using a self-consistent infrastructure. PCI Express defines the registers necessary to support the integration of a Hot PlUg Controller within individual root and switch ports. Under Hot-Plug software control, the Hot-Plug controllers and the associated port interface within the root or switch port must control the card interface signals to ensure orderly power down and power up as cards are removed and replaced. The standard Hot-Plug controller signaling interface includes PWRLED#, ATNLED#, PWREN, REFCLKEN#, PERST#, PRSNT1#, PRSNT2#, PWRFLT#, AUXEN, MRL# AND BUTTON#.

This application note describes how to implement two PCI Express hot-plug slots using the IDT PES12N3 12-lane, 3-port PCI Express switch.

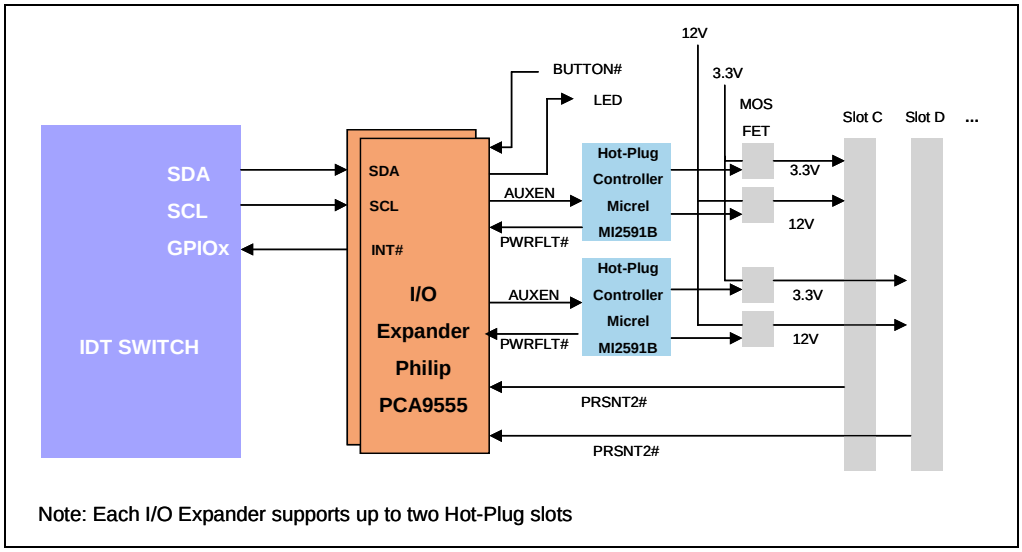

Figure 1 Hot-Plug Block Diagram

I/O Expander

The PES12N3 utilizes an external SMBus/I2C-bus I/O expander connected to the master SMBus interface for hot-plug related signals associated with downstream ports. It is designed to work with Phillips PCA9555 compatible I/O expanders. See the Phillips PCA9555 data sheet for details on the operation of this device. The external SMBus I/O expander provides 16 I/O pins that may be configured as inputs or outputs. In a three-port application, the mapping of downstream ports' hot-plug signals, listed in Table 2, to these I/O pins is shown in Table 3.

Notes

Signal	Type	Name Description
PxAPN	I	Port x Attention Push button Input
PxPDN	I	Port x Presence Detect Input
PxPFN	I	Port x Power Fault Input
PxMRLN	I	Port x Manually-Operated Retention Latch (MFL) Input
PxAIN	O	Port x Attention Indicator Output
PxPIN	O	Port x Power Indicator Output
PxPEP	O	Port x Power Enable Output
PxINTERLOOCKP	O	Port x Electromechanical Interlock

Table 1 Downstream Ports B and C Hot-Plug Signals

SMBUS I/O Expander	Type	Signal
0 (I/O0.0)	I	PBAPN
1 (I/O 0.1)	I	PBPDN
2 (I/O 0.2)	I	PBPFN
3 (I/O 0.3)	I	PBMRLN
4 (I/O 0.4)	O	PBAIN
5 (I/O 0.5)	O	PBPIN
6 (I/O 0.6)	O	PBPEP
7 (I/O 0.7)	O	PBINTERLOCK
8 (I/O 1.0)	O	PCAPN
9 (I/O 1.1)	O	PCPDN
10 (I/O 1.2)	I	PCPFN
11 (I/O 1.3)	I	PCMRLN
12 (I/O 1.4)	O	PCAIN
13 (I/O 1.5)	O	PCPIN
14 (I/O 1.6)	O	PCPEP
15 (I/O 1.7)	O	PCINTERLOCKP

Table 2 SMBus I/O Expander Signals

During configuration of the PES12N3, the SMBus/I2C-bus address of the hot-plug I/O expander should be written to the hot-plug I/O Expander Master SMBus Address (IOEADDR) field in the SMBus status (PA_SMBUSSTS) register. SMBus write transactions are issued to the I/O expander by the PES12N3 to configure the device whenever the value of the IOEADDR field is modified. Outputs for downstream ports that are disabled are set to their negated value (e.g., the power indicator is turned off).

Notes

The I/O expander configuration sequence issued by the PES12N3 is as follows:

- *write value 0x50 to I/O expander register 2*
- *write value 0x50 to I/O expander register 3*
- *write value 0x0 to I/O expander register 4 (no inversion in IO-0)*
- *write value 0x0 to I/O expander register 5 (no inversion in IO-1)*
- *write value 0x0F to I/O expander register 6 (bits 4, 5, 6 and 7 are outputs of IO-0)*
- *write value 0x0F to I/O expander register 7 (bits 4, 5, 6 and 7 are outputs of IO-1)*
- *read value of I/O expander register 0 to obtain the current state of the I/O IO-0 inputs.*
- *read value of I/O expander register 1 to obtain the current state of the I/O IO-I inputs.*

Whenever a hot-plug output from port B or C needs to change state, a master SMBus transaction is initiated to update the state of the I/O expander. This write operation causes the I/O expander to change the state of its output(s). Port B output values are written to I/O expander register 2 and Port C values are written to I/O expander register 3.

The I/O expander has an open drain interrupt output that is asserted when a pin configured as an input changes state from the value previously read. The interrupt output from the SMBus I/O expander should be connected to GPIO[2], and GPIO[2] should be initialized during configuration to operate in alternate function mode as the Hot-plug I/O expander interrupt input. Whenever a input to the I/O expander changes state from the value previously read, the interrupt output of the I/O expander connected to GPIO[2] is asserted. This causes the PES12N3 to issue a master SMBus transaction to read the updated state of the I/O expander inputs.

Port B input values are read from I/O expander register 0 and Port C values are read from I/O expander register 1. The I/O expander interrupt request output is negated whenever the input values are read or when the input pin changes state back to the value previously read. Any errors detected during I/O expander SMBus read or write transactions is reflected in the status bits of the SMBus Status (PA_SMBUSSTS) register. The I/O Expander Interface (PA_IOEXPINTF) register allows direct testing and debugging of the I/O expander functionality. The Port B Hot-Plug Signals (PBHPS) and the Port C Hot-Plug Signals (PCHPS) fields in the PA_IOEXPINTF register reflect the current state, as viewed by the PES12N3, of all of the I/O expander inputs and outputs.

Writing a 1 to the Reload I/O Expander Signals (RELOADIOEX) bit in the PA_IOEXPINTF register causes the PES12N3 to generate SMBus write and read transactions to the I/O expander, causing the value in the PBHPS and PCHPS fields to reflect the state of the I/O expander signals. This feature may be used to aid in debugging the hot-plug operation. For example, a user who neglects to configure GPIO[2] as an alternate function may use this feature to determine that master SMBus transactions to the I/O expander function properly and that the issue is with the interrupt logic. The I/O Expander Test Mode (IOEXTM) bit in the PA_IOEXPTINF register allows an I/O expander test mode to be entered. Normally, hot-plug outputs which are generated by ports B and C first update the PBHPS and PCHPS fields before being written to the I/O expander. When this bit is set, these hot-plug outputs are blocked from updating the fields. Instead, values written directly to the PBHPS and PCHPS fields will be sent to the I/O expander. In this mode, the PES12N3 issues a transaction to update the state of the I/O expander whenever a bit corresponding to a hot-plug controller output in these fields changes state due to a configuration write.

Power Controller

When circuit boards are inserted into systems carrying live supply voltages (“hot-plugged”), high inrush currents often result due to the charging of bulk capacitance that resides across the circuit board’s supply pins. This transient inrush current can cause the system’s supply voltages to temporarily go out of regulation, causing data loss or system lock-up. In more extreme cases, the transients occurring during a hotplug event may cause permanent damage to connectors or on-board components. The MIC2591B addresses these issues by limiting the inrush currents to the load (PCI Express Board), and thereby controlling the rate at which the load’s circuits turn-on. In addition to this inrush current control, the MIC2591B offers input and output voltage supervisory functions and current limiting to provide robust protection for both the system and circuit board.

Notes

The Power Enable output (PEP) pins from the I/O Expander will be used to enable the 12V, 3.3V and 3.3VAUX to the downstream slots. The outputs can be switched only after the Vstby input supply is valid and stable.

REFCLKEN#

The REFCLK# to the hot-plug slot will be driven by an external clock generator.

BUTTON#

The Attention Button can be connected directly to IO Expander.

PWRLED# and ATNLED)#

The power LED indicator and attention LED indicator are driven by IO Expander.

Related Hot-Plug Configuration Registers

Register	Bit	Description
PCI Express Capability (0x40h)	24	Slot Implemented.
PCI Express Device Capabilities (0x44h)	12	Attention Button Present
	13	Attention Indicator Present
PCI Express Slot Capabilities (0x54h)	0	Attention Button Present
	1	Power Control Present
	2	MRL Sensor Present
	3	Attention Indicator Present
	6	Hot-Plug Capable
	17	Electromechanical Interlock Present
PCI Express Slot Control (0x58h)	0	Attention Button Present Enable
	1	Power Fault Detected Enable
	2	MRL Sensor Change enable
	3	Presence Detected Changed Enable
	5	Hot-Plug Interrupt Enable
	7:6	Attention Indicator Control
	9:8	Power Indicator Control
	10	Power Controller Control
	11	Electromechanical Interlock Control
PCI Express Slot Status (0x5A)	0	Attention Button Pressed
	1	Power Fault Detected
	2	MRL Sensor Changed
	3	Presence Detected Changed
	5	MRL Sensor State

Table 3 Hot-Plug Configuration Registers

Notes

Register	Bit	Description
	6	Presence Detect State
	7	Electromechanical Interlock Status
SMBus Status (0xAC)	23:17	Hot-Plug I/O Expander Master SMBus Address
I/O Expander Interface (0xB0)	7:0	Port B Hot-Plug Signals
	15:8	Port C Hot-Plug Signals

Table 3 Hot-Plug Configuration Registers

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