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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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4571 Group

Timers

1. Abstract

This document shows an example of how to set the timers of the 4571 group of Renesas microcomputers and an application example for using those timers.

2. Introduction

The application example explained in this document is applied for use with the microcomputers and under the conditions described below.

- Microcomputer: 4571 group
- Oscillation frequency: 4 MHz
- System clock: Through mode (not frequency divided)

Please note that some sample programs available from Renesas involve manipulating the bits of unused functions for reasons of bit arrangement in the control registers. The values of these bits in a user system should be set to suit the usage condition of the system.

In this application note, explanation is made of an example of timer setting method and an application example with respect to the following:

- CNTR0 output operation: Buzzer output
- CNTR0 input operation: Event count
- Timer operation: Timer start by external input
- Watchdog timer

3. Related Registers

3.1 Interrupt Control Register V1

Table 3.1 shows the Bit Configuration of Interrupt Control Register V1.

For write to the register V1, first set a value in the register A and then use the TV1A instruction.

Furthermore, the TAV1 instruction may be used to transfer the content of the register V1 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V1

Interrupt Control Register V1		When reset: 0000_2	When RAM backed-up: 0000_2	R/W TAV1/TV1A
$V1_3$	Timer 2 interrupt enable bit	0	Disables interrupt generation (SNZT2 instruction is valid)	
		1	Enables interrupt generation (SNZT2 instruction is invalid)	
$V1_2$	Timer 1 interrupt enable bit	0	Disables interrupt generation (SNZT1 instruction is valid)	
		1	Enables interrupt generation (SNZT1 instruction is invalid)	
$V1_1$	External 1 interrupt enable bit	0	Disables interrupt generation (SNZ1 instruction is valid)	
		1	Enables interrupt generation (SNZ1 instruction is invalid)	
$V1_0$	External 0 interrupt enable bit	0	Disables interrupt generation (SNZ0 instruction is valid)	
		1	Enables interrupt generation (SNZ0 instruction is invalid)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: : Unused bits during timer setting

3.2 Interrupt Control Register V2

Table 3.2 shows the Bit Configuration of Interrupt Control Register V2.

For write to the register V2, first set a value in the register A and then use the TV2A instruction.

Furthermore, the TAV2 instruction may be used to transfer the content of the register V2 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register V2

Interrupt Control Register V2		When reset: 0000_2	When RAM backed-up: 0000_2	R/W TAV2/TV2A
$V2_3$	Voltage down detection circuit interrupt enable bit	0	Disables interrupt generation (SNZVD instruction is valid)	
		1	Enables interrupt generation (SNZVD instruction is invalid)	
$V2_2$	Unused	0	This bit has no functions, but can be accessed for read/write.	
		1		
$V2_1$	Unused	0	This bit has no functions, but can be accessed for read/write.	
		1		
$V2_0$	Timer 3 interrupt enable bit	0	Disables interrupt generation (SNZT3 instruction is valid)	
		1	Enables interrupt generation (SNZT3 instruction is invalid)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: : Unused bits during timer setting

3.3 Interrupt Control Register I1

Table 3.3 shows the Bit Configuration of Interrupt Control Register I1.

For write to the register I1, first set a value in the register A and then use the TI1A instruction.

Furthermore, the TAI1 instruction may be used to transfer the content of the register I1 to the register A.

Table 3.3 Bit Configuration of Interrupt Control Register I1

Interrupt Control Register I1		When reset: 0000_2	When RAM backed-up: State retained	R/W TAI1/TI1A
$I1_3$	INT0 pin input control bit Note 2	0	Disables input	
		1	Enables input	
$I1_2$	INT0 pin interrupt active waveform/ return level select bit Note 2	0	Falling waveform/low level (SNZI0 instruction recognizes low level on INT0 pin)	
		1	Rising waveform/high level (SNZI0 instruction recognizes high level on INT0 pin)	
$I1_1$	INT0 pin edge detection circuit control bit	0	Detects one edge	
		1	Detects both edges	
$I1_0$	INT0 pin timer 1 control enable bit	0	Disables timer 1 control	
		1	Enables timer 1 control	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When the contents of these bits ($I1_2$ or $I1_3$) are changed, the external interrupt request flag (EXF0) may be set.

Note 3: : Unused bits during timer setting

3.4 Timer Control Register PA

Table 3.4 shows the Bit Configuration of Timer Control Register PA.

For write to the register PA, first set a value in the register A and then use the TPAA instruction.

Table 3.4 Bit Configuration of Timer Control Register PA

Timer Control Register PA		When reset: 00_2	When RAM backed-up: 00_2	W TPAA
PA_1	Prescaler count source select bit	0	Instruction clock (INSTCK)	
		1	Divide-by-4 signal of instruction clock (INSTCK)	
PA_0	Prescaler control bit	0	Stop (state retained)	
		1	Operating	

Note 1: The letter W denotes “writable.”

3.5 Timer Control Register W1

Table 3.5 shows the Bit Configuration of Timer Control Register W1.

For write to the register W1, first set a value in the register A and then use the TW1A instruction.

Furthermore, the TAW1 instruction may be used to transfer the content of the register W1 to the register A.

Table 3.5 Bit Configuration of Timer Control Register W1

Timer Control Register W1		When reset: 0000_2		When RAM backed-up: State retained	R/W TAW1/TW1A
$W1_3$	Timer 1 count auto stop circuit select bit Note 2	0	Does not select timer 1 count auto stop circuit		
		1	Selects timer 1 count auto stop circuit		
$W1_2$	Timer 1 control bit	0	Stop (state returned)		
		1	Operating		
$W1_1$	Timer 1 count source select bit	$W1_1$	$W1_0$	Count source	
		0	0	PWM signal (PWMOUT)	
		0	1	Prescaler output (ORCLK)	
$W1_0$		1	0	System clock (STCK)	
		1	1	CNTR0 input	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: This function is usable only when INT0 pin timer 1 control is enabled ($I1_0$ = 1) and the timer 1 count start sync circuit is selected ($W5_3$ = 1).

3.6 Timer Control Register W2

Table 3.6 shows the Bit Configuration of Timer Control Register W2.

For write to the register W2, first set a value in the register A and then use the TW2A instruction.

Furthermore, the TAW2 instruction may be used to transfer the content of the register W2 to the register A.

Table 3.6 Bit Configuration of Timer Control Register W2

Timer Control Register W2		When reset: 0000_2		When RAM backed-up: State retained	R/W TAW2/TW2A
$W2_3$	CNTR0 pin function select bit	0	Divide-by-2 output of time 1 underflow signal		
		1	Divide-by-2 output of time 2 underflow signal		
$W2_2$	Timer 2 control bit	0	Stop (state returned)		
		1	Operating		
$W2_1$	Timer 2 count source select bit	$W2_1$	$W2_0$	Count source	
		0	0	PWM signal (PWMOUT)	
		0	1	Prescaler output (ORCLK)	
$W2_0$		1	0	System clock (STCK)	
		1	1	Time 1 underflow signal (T1UDF)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

3.7 Timer Control Register W3

Table 3.7 shows the Bit Configuration of Timer Control Register W3.

For write to the register W3, first set a value in the register A and then use the TW3A instruction.

Furthermore, the TAW3 instruction may be used to transfer the content of the register W3 to the register A.

Table 3.7 Bit Configuration of Timer Control Register W3

Timer Control Register W3		When reset: 0000_2	When RAM backed-up: 0000_2	R/W TAW3/TW3A
$W3_3$	CNTR1 pin output control bit	0	Disables CNTR1 pin output	
		1	Enables CNTR1 pin output	
$W3_2$	PWM signal high period extension function control bit	0	Disables PWM signal high period extension function	
		1	Enables PWM signal high period extension function	
$W3_1$	Timer 3 control bit	0	Stop (state retained)	
		1	Operating	
$W3_0$	Timer 3 count source select bit	0	X_{IN} input	
		1	Divide-by-2 signal of prescaler output (ORCLK)	

Note 1: The letter R denotes "readable," and the letter W denotes "writable."

3.8 Timer Control Register W5

Table 3.8 shows the Bit Configuration of Timer Control Register W5.

For write to the register W5, first set a value in the register A and then use the TW5A instruction.

Furthermore, the TAW5 instruction may be used to transfer the content of the register W5 to the register A.

Table 3.8 Bit Configuration of Timer Control Register W5

Timer Control Register W5		When reset: 0000_2	When RAM backed-up: State retained	R/W TAW5/TW5A
$W5_3$	Timer 1 count start sync circuit select bit Note 2	0	Does not select timer 1 count start sync circuit	
		1	Selects timer 1 count start sync circuit	
$W5_2$	CNTR0 pin input count edge select bit	0	Falling edge	
		1	Rising edge	
$W5_1$	CNTR1 pin output auto control circuit select bit	0	Does not select CNTR1 pin output auto control circuit	
		1	Selects CNTR1 pin output auto control circuit	
$W5_0$	D_4/CNTR0 pin function select bit	0	D_4 input-output/CNTR0 input	
		1	D_4 input/CNTR0 output	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: This function is usable only when INT0 pin timer 1 control is enabled ($I1_0$ = 1).

4. Timer Application Example

4.1 CNTR0 Output Operation: Buzzer Output

Point: The square wave output from timer 2 can be used for buzzer output as its application.

Specification: When system clock frequency = 4 MHz, a square wave of approximately 4 kHz in frequency is output from the CNTR0 pin.

Figure 4.1 shows an Example of a Peripheral Circuit. Figure 4.3 shows an Example of CNTR0 Output Setting.

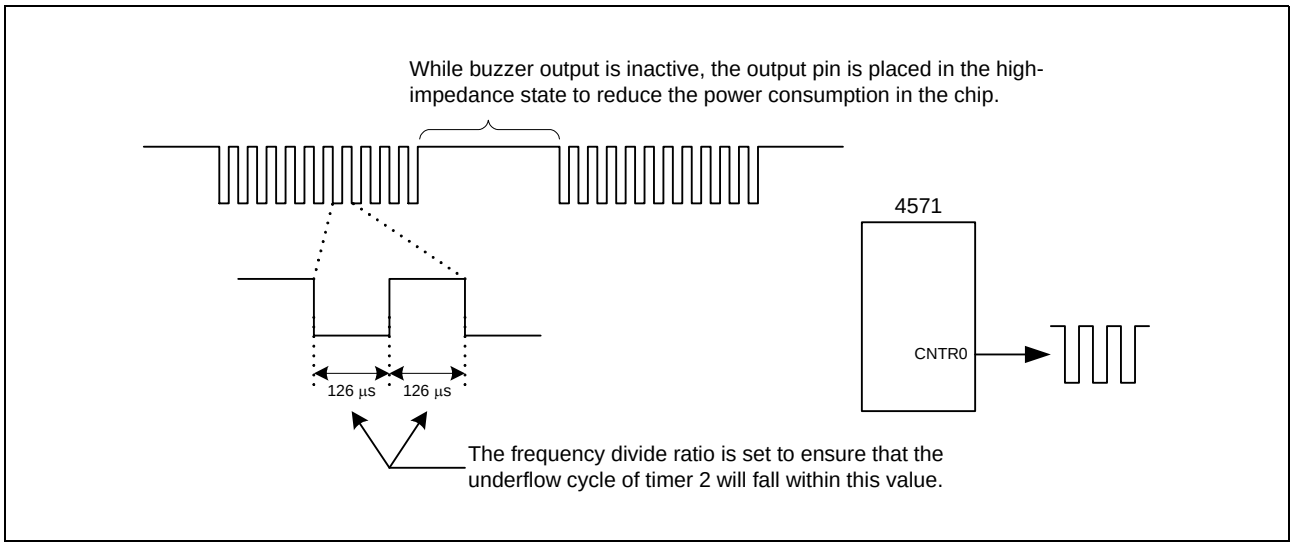


Figure 4.1 Example of a Peripheral Circuit

4.2 CNTR0 Input Operation: Event Count

Point: A signal (rising waveform) input from the CNTR0 pin can be used as an event for count operation.

Specification: Low-frequency pulses are input as the count source for timer 1 from an external source to the CNTR0 pin, and a timer 1 interrupt is generated every 100 pulses counted.

Figure 4.4 shows an Example of CNTR0 Input Setting.

4.3 Timer Operation: Timer Start by External Input

Point: A fixed length of time can be measured using external input.

Specification: Timer 1 is triggered to start counting by INT0 input and generates an interrupt 1 ms later.

Figure 4.5 shows an Example of Settings for Timer 1 Start by External 0 Input.

4.4 Watchdog Timer

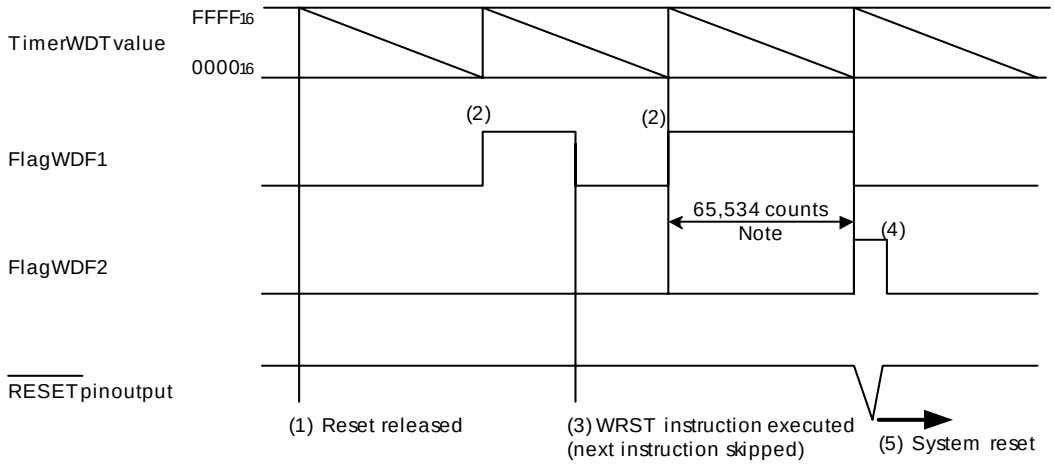
The watchdog timer function offers a means for restoring the chip into a reset state when, for example, a program has gone wild and could not be executed normally.

When the watchdog timer function is enabled, always make sure that the WRST instruction is executed at intervals equal to or less than 65,534 counts of a 16-bit timer (i.e., at intervals equal to or less than 65,534 machine cycles).

Point: While operating normally, the WRST instruction is always executed within 65,534 counts of a 16-bit timer. If the program goes wild, the WRST instruction will no longer be executed, causing the chip to be reset.

Specification: Using a system clock frequency of 4.0 MHz, this function detects program runaway by executing the WRST instruction within 49 ms.

Figure 4.2 schematically shows the Watchdog Timer Function. Figure 4.6 shows an Example of Using the Watchdog Timer.



(1) After reset (after program start), the timer WDT starts counting down.
(2) When the timer WDT underflows upon reaching the minimum count, the flag WDF1 is set to 1.
(3) When the WRST instruction is executed, the flag WDF1 is cleared to 0 and the next instruction is skipped.
(4) If the timer WDT underflows while the flag WDF1 = 1, the flag WDF2 is set to 1 and a watchdog reset signal is output.
(5) The watchdog reset signal causes the output transistor of the $\overline{\text{RESET}}$ pin to turn on, thereby generating a system reset.

Note: Since the count source for the timer WDT is the instruction clock, the number of counts is the same as the number of machine cycles.

Figure 4.2 Watchdog Timer Function

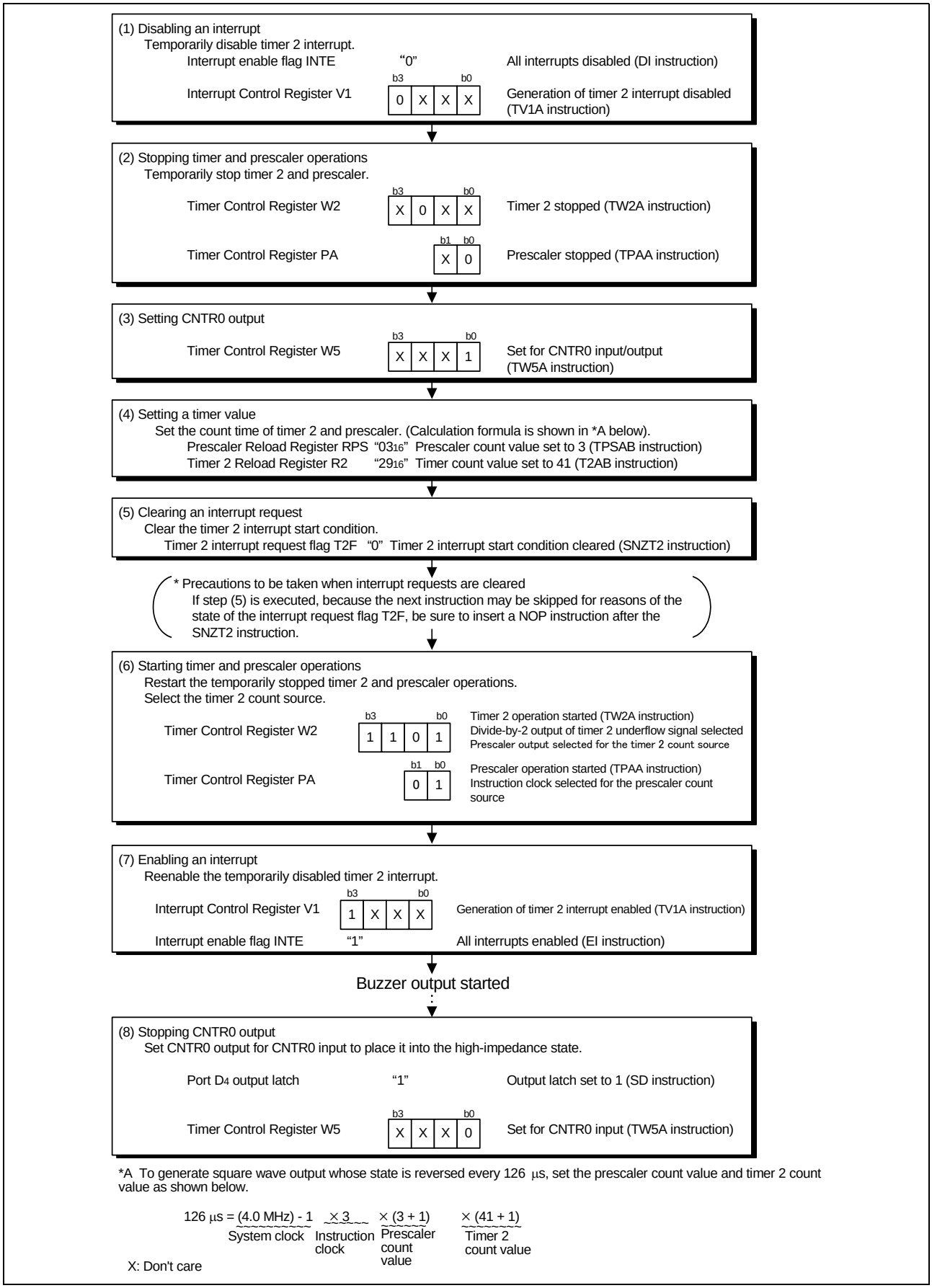


Figure 4.3 Example of CNTR0 Output Setting

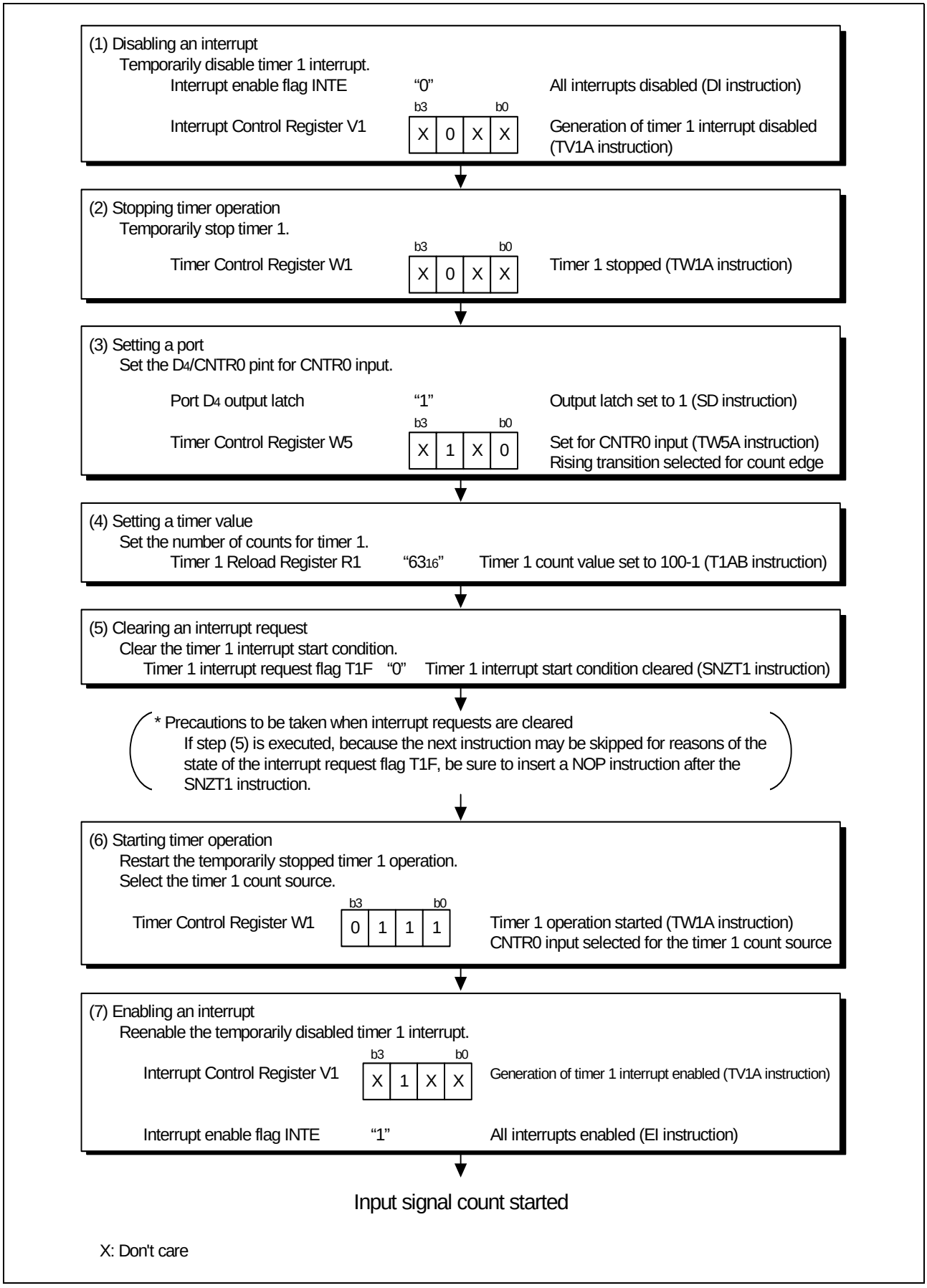


Figure 4.4 Example of CNTR0 Input Setting

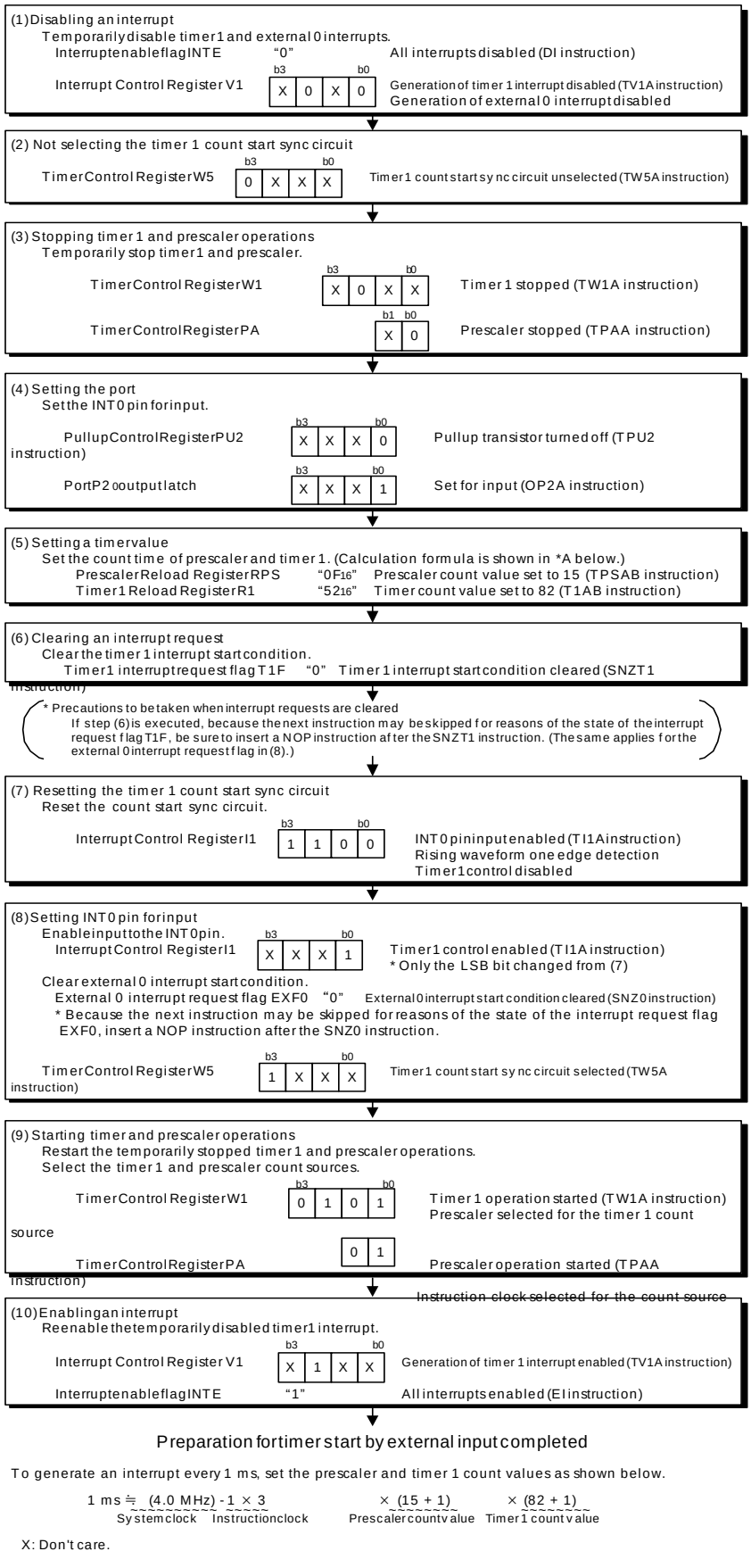


Figure 4.5 Example of Settings for Timer 1 Start by External 0 Input

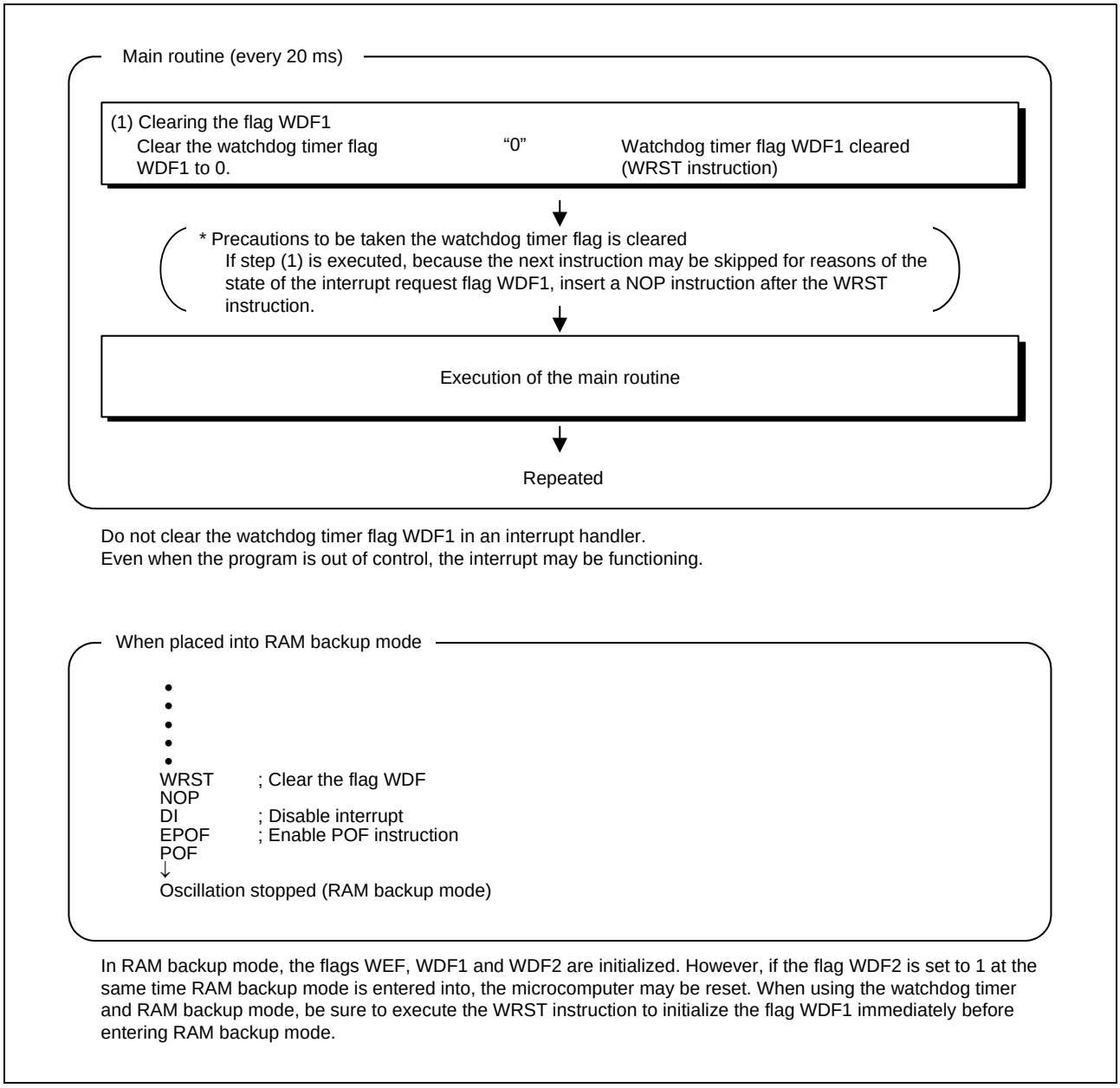


Figure 4.6 Example of Using the Watchdog Timer

5. Sample Programs

Sample programs are available from the Renesas Technology Web site.
To download one, click the screen menu "Application Note" on the left side of 4571 Group Web page.

6. Reference Documents

Data sheet
4571 Group Data sheet

The latest version is available from the Renesas Technology Web site.

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Renesas Technology Web site:
http://japan.renesas.com/

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Revision history	4571 Group Timers Application Note

Rev.	Date	Description	
		Page	Points
1.00	2006.08.01	-	First edition issued

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