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# 4571 Group

## Carrier Output

### 1. Abstract

This document shows an example of how to set the carrier output of the 4571 group of Renesas microcomputers and an application example for using it.

### 2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

- Microcomputer : 4571 group
- Oscillator frequency : 4 MHz as main clock  $f(\text{XCIN})$ , however
- System clock : Used in through mode (not frequency divided)

Please note that the sample program for the 4571 group may somewhere in it manipulate the bits of unused functions for reasons of bit arrangement in the control registers. The values of these bits in a user system should be set to suit the usage condition of the system.

### 3. Related Registers

#### 3.1 Interrupt Control Register V1

Table 3.1 shows the bit configuration of Interrupt Control Register V1.

For write to the register V1, first set a value in the register A and then use the TV1A instruction.

Furthermore, the TAV1 instruction may be used to transfer the content of register V1 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V1

Interrupt Control Register V1		When reset: 0000 <sub>2</sub>	When RAM backed-up: 0000 <sub>2</sub>	R/W TAV1/TV1A
V13	Timer 2 interrupt enable bit	0	Disables interrupt generation (SNZT2 instruction effective)	
		1	Enables interrupt generation (SNZT2 instruction has no effect)	
V12	Timer 1 interrupt enable bit	0	Disables interrupt generation (SNZT1 instruction effective)	
		1	Enables interrupt generation (SNZT1 instruction has no effect)	
V11	External 1 interrupt enable bit	0	Disables interrupt generation (SNZ1 instruction effective)	
		1	Enables interrupt generation (SNZ1 instruction has no effect)	
V10	External 0 interrupt enable bit	0	Disables interrupt generation (SNZ0 instruction effective)	
		1	Enables interrupt generation (SNZ0 instruction has no effect)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2:  : Unused bits during carrier output setting.

#### 3.2 Interrupt Control Register V2

Table 3.2 shows the bit configuration of Interrupt Control Register V2.

For write to the register V2, first set a value in the register A and then use the TV2A instruction.

Furthermore, the TAV2 instruction may be used to transfer the content of register V2 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register V2

Interrupt Control Register V2		When reset: 0000 <sub>2</sub>	When RAM backed-up: 0000 <sub>2</sub>	R/W TAV2/TV2A
V23	Voltage down detection circuit interrupt enable bit	0	Disables interrupt generation (SNZVD instruction effective)	
		1	Enables interrupt generation (SNZVD instruction has no effect)	
V22	Unused	0	This bit has no functions assigned, but can be read/written.	
		1		
V21	Unused	0	This bit has no functions assigned, but can be read/written.	
		1		
V20	Timer 3 interrupt enable bit	0	Disables interrupt generation (SNZT3 instruction effective)	
		1	Enables interrupt generation (SNZT3 instruction has no effect)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2:  : Unused bits during carrier output setting.

### 3.3 Timer Control Register W1

Table 3.3 shows the bit configuration of Timer Control Register W1.

For write to the register W1, first set a value in the register A and then use the TW1A instruction.

Furthermore, the TAW1 instruction may be used to transfer the content of register W1 to the register A.

Table 3.3 Bit Configuration of Timer Control Register W1

Timer Control Register W1		When reset: 0000 <sub>2</sub>		When RAM backed-up: State retained	R/W TAW1/TW1A
W1 <sub>3</sub>	Timer 1 count auto stop circuit select bit Note 2	0	Deselects timer 1 count auto stop circuit		
		1	Selects timer 1 count auto stop circuit		
W1 <sub>2</sub>	Timer 1 control bit	0	Stop (state retained)		
		1	Start		
W1 <sub>1</sub>	Timer 1 count source select bit	W1 <sub>1</sub>	W1 <sub>0</sub>	Count source	
		0	0	PWM signal (PWMOUT)	
		0	1	Prescaler output (ORCLK)	
		1	0	System clock (STCK)	
W1 <sub>0</sub>		1	1	CNTR0 input	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: This function is usable only when INT0 pin timer 1 control is enabled (I10 = 1) and the timer 1 count start synchronizing circuit is selected (W53 = 1).

### 3.4 Timer Control Register W3

Table 3.4 shows the bit configuration of Timer Control Register W3.

For write to the register W3, first set a value in the register A and then use the TW3A instruction.

Furthermore, the TAW3 instruction may be used to transfer the content of register W3 to the register A.

Table 3.4 Bit Configuration of Timer Control Register W3

Timer Control Register W3		When reset: 0000 <sub>2</sub>		When RAM backed-up: 0000 <sub>2</sub>	R/W TAW3/TW3A
W3 <sub>3</sub>	CNTR1 pin output control bit	0	Disables CNTR1 pin output		
		1	Enables CNTR1 pin output		
W3 <sub>2</sub>	PWM signal high period extend function control bit Timer	0	Disables PWM signal high period extend function		
		1	Enables PWM signal high period extend function		
W3 <sub>1</sub>	Timer 3 control bit	0	Stop (state retained)		
		1	Start		
W3 <sub>0</sub>	Timer 3 count source select bit	0	XIN input		
		1	Prescaler output (ORCLK) divided by 2		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

### 3.5 Timer Control Register W5

Table 3.5 shows the bit configuration of Timer Control Register W5.

For write to the register W5, first set a value in the register A and then use the TW5A instruction.

Furthermore, the TAW5 instruction may be used to transfer the content of register W5 to the register A.

Table 3.5 Bit Configuration of Timer Control Register W5

Timer Control Register W5		When reset: 0000 <sub>2</sub>	When RAM backed-up: State retained	R/W TAW5/TW5A
W5 <sub>3</sub>	Timer 1 count start synchronizing circuit select bit <small>Note 2</small>	0	Deselects timer 1 count start synchronizing circuit	
		1	Selects timer 1 count start synchronizing circuit	
W5 <sub>2</sub>	CNTR0 pin input count edge select bit	0	Falling edge	
		1	Rising edge	
W5 <sub>1</sub>	CNTR1 pin output auto control circuit select bit	0	Deselects CNTR1 pin output auto control circuit	
		1	Selects CNTR1 pin output auto control circuit	
W5 <sub>0</sub>	D4/CNTR0 pin function select bit	0	D4 input/output or CNTR0 input	
		1	D4 input or CNTR0 input/output	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: This function is usable only when INT0 pin timer 1 control is enabled (I10 = 1).

Note 3: : Unused bits during carrier output setting.

## 4. Timer Application Example

### 4.1 Carrier Output

- Point :
- Timer 3 is used to generate a PWM signal (remote control carrier).
  - Timer 1 is used to control whether or not to output a PWM signal from the CNTR1 pin.
  - Each time timer 1 underflows after reaching the terminal count, PWM output from the CNTR1 pin is switched on and off
  - Timer 1 uses the PWM signal as its count source. The interval time for which PWM output from the CNTR1 pin is turned on or off can be changed by altering the set value of timer 1.
  - Even when no PWM signals are output from the CNTR1 pin, the chip is generating a PWM signal internally in it.

Specification : PWM signal: Approx. 33.3 kHz, 1/2 duty cycle

CNTR output: Basic duration  $T = 0.55$  ms; Output on for  $8T$ , output off for  $4T$ , and output on for  $T$

Figure 4.1 shows automatic control of CNTR1 output. Figure 4.2 shows an example of carrier output setting (example 1). Figure 4.3 shows an example of carrier output setting (example 2).

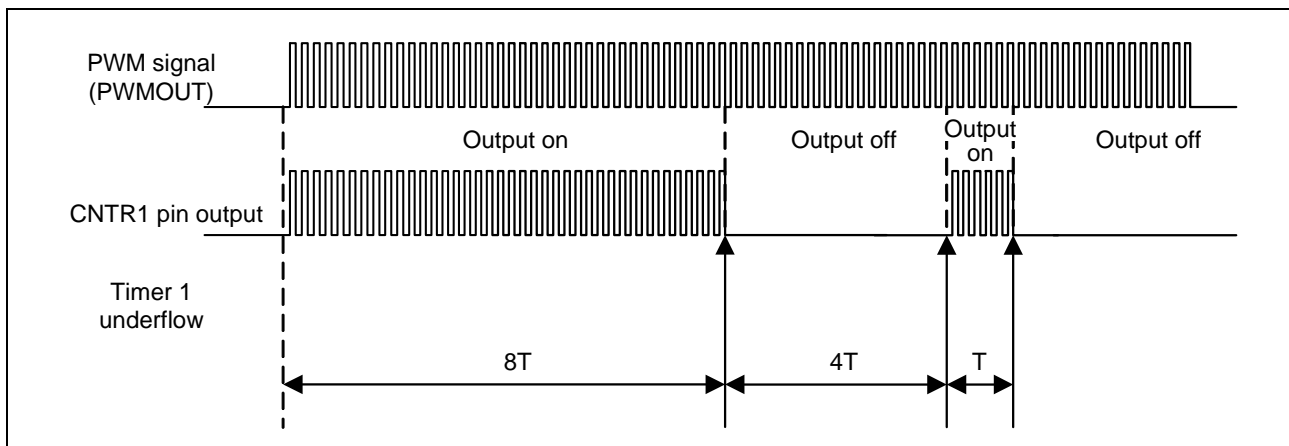
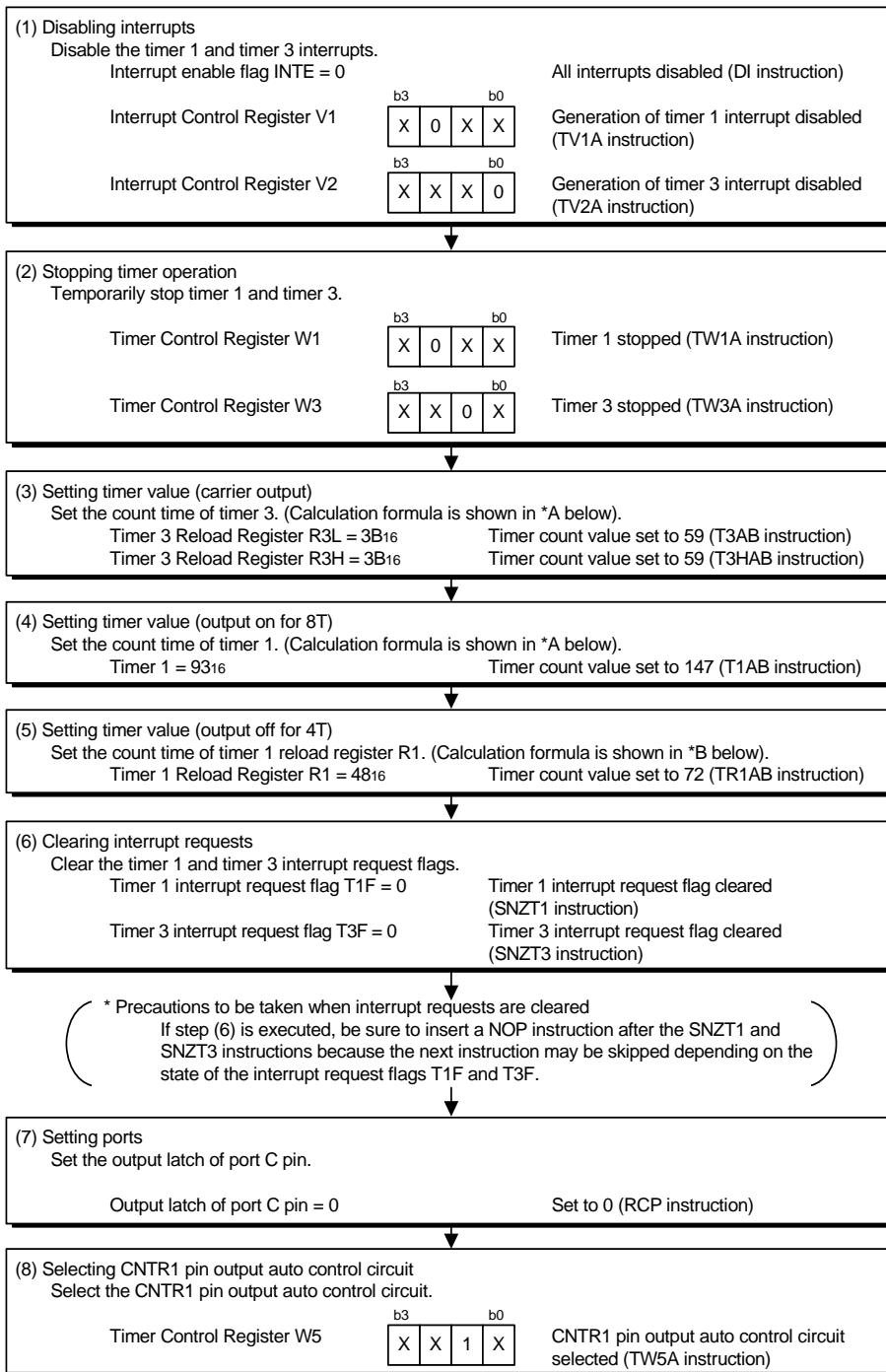


Figure 4.1 Automatic Control of CNTR Output



Go to example 2 for carrier output setting

\*A For carrier output, set the count values of timer 1 and timer 3 as shown below.

$$\text{Timer 3: } 15 \mu\text{s} = \frac{(4.0\text{MHz}) - 1}{\text{Main clock } f(\text{Xin})} \times (59+1)$$

Timer 2 count value

$$\text{Timer 1: } 4,400 \mu\text{s} = \frac{(15 \mu\text{s} + 15 \mu\text{s})}{\text{PWM period}} \times (147)$$

Timer 1 count value

\*B For carrier output, set the count value of timer 1 as shown below.

$$\text{Timer 1: } 2,200 \mu\text{s} = \frac{(15 \mu\text{s} + 15 \mu\text{s})}{\text{PWM period}} \times (72+1)$$

Timer 1 count value

X: Don't care

Figure 4.2 Example 1 for Carrier Output Setting



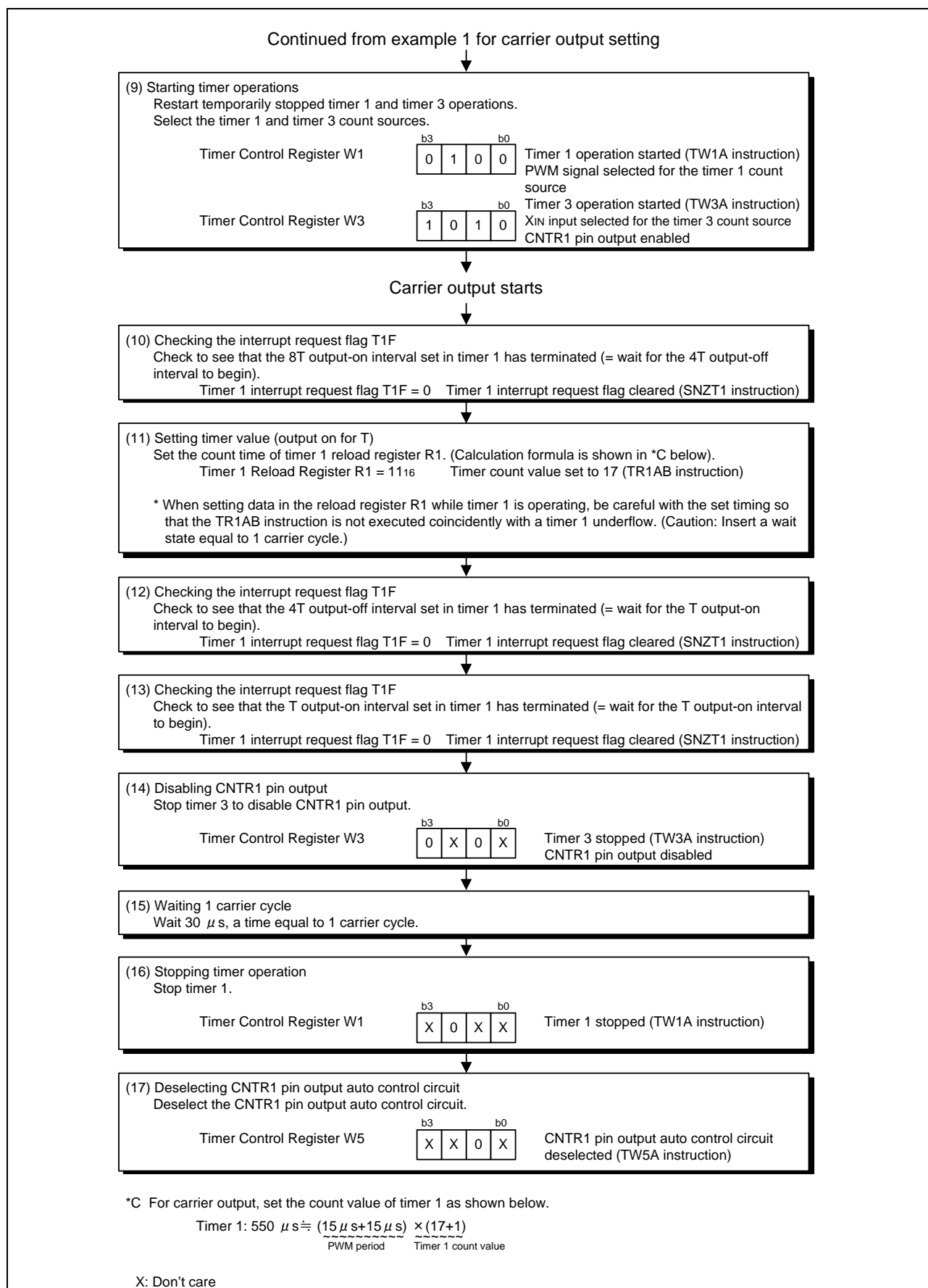


Figure 4.3 Example 2 for Carrier Output Setting

## 5. Sample Programs

Sample programs are available from the Renesas Technology Web site. To download one, click the screen menu “Application Note” on the left side of 4571 group Web page.

## 6. Reference Documents

Data sheet

4571 Group Data Sheet

The latest version is available from the Renesas Technology Web site.

## 7. Renesas Web Site and Where to Contact

Renesas Technology Web site:

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Revision history	4571 Group Carrier Output Application Note
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Rev.	Date	Description	
		Page	Points
1.00	2006.11.01	–	First edition issued

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