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# 4559 Group

## Timers

## 1. Abstract

This document shows an example of how to set the timers of the 4559 group of Renesas microcomputers and an application example for using those timers.

## 2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

- Microcomputer : 4559 group
- Oscillation frequency : 4 MHz as f(XIN), however; 32.768 kHz as f(XCIN), however
- System clock : Used in through mode (not frequency divided)

Please note that the sample program for the 4559 group may somewhere in it manipulate the bits of unused functions for reasons of bit arrangement in the control registers. The values of these bits in a user system should be set to suit the usage condition of the system.

In this application note, explanation is made of an example of timer setting method and an application example with respect to the following:

- CNTR output operation: Buzzer output
- CNTR input operation: Event count
- Timer operation: Timer start by external input
- Timer operation: Fixed-cycle counter
- Watchdog timer

# 3. Related Registers

## 3.1 Interrupt Control Register V1

Table 3.1 shows the bit configuration of Interrupt Control Register V1.
For write to the register V1, first set a value in the register A and then use the TV1A instruction.
Furthermore, the TAV1 instruction may be used to transfer the content of register V1 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V1

| Interrupt Control Register V1 | | When reset: $0000_2$ | When powered down: $0000_2$ | R/W TAV1/TV1A |
|---|---|---|---|---|
| $V1_3$ | Timer 2 interrupt enable bit | 0 | Disables interrupt generation (SNZT2 instruction effective) | |
| | | 1 | Enables interrupt generation (SNZT2 instruction has no effect) | |
| $V1_2$ | Timer 1 interrupt enable bit | 0 | Disables interrupt generation (SNZT1 instruction effective) | |
| | | 1 | Enables interrupt generation (SNZT1 instruction has no effect) | |
| $V1_1$ | Unused | 0 | This bit has no functions assigned, but can be read/written. | |
| | | 1 | | |
| $V1_0$ | External 0 interrupt enable bit | 0 | Disables interrupt generation (SNZ0 instruction effective) | |
| | | 1 | Enables interrupt generation (SNZ0 instruction has no effect) | |

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: : Unused bits during timer setting.

## 3.2 Interrupt Control Register V2

Table 3.2 shows the bit configuration of Interrupt Control Register V2.
For write to the register V2, first set a value in the register A and then use the TV2A instruction.
Furthermore, the TAV2 instruction may be used to transfer the content of register V2 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register V2

| Interrupt Control Register V2 | | When reset: $0000_2$ | When powered down: $0000_2$ | R/W TAV2/TV2A |
|---|---|---|---|---|
| $V2_3$ | Unused | 0 | This bit has no functions assigned, but can be read/written. | |
| | | 1 | | |
| $V2_2$ | Unused | 0 | This bit has no functions assigned, but can be read/written. | |
| | | 1 | | |
| $V2_1$ | Unused | 0 | This bit has no functions assigned, but can be read/written. | |
| | | 1 | | |
| $V2_0$ | Timer 3 interrupt enable bit | 0 | Disables interrupt generation (SNZT3 instruction effective) | |
| | | 1 | Enables interrupt generation (SNZT3 instruction has no effect) | |

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: : Unused bits during timer setting.

## 3.3 Interrupt Control Register I1

Table 3.3 shows the bit configuration of Interrupt Control Register I1.

For write to the register I1, first set a value in the register A and then use the TI1A instruction.

Furthermore, the TAI1 instruction may be used to transfer the content of register I1 to the register A.

Table 3.3 Bit Configuration of Interrupt Control Register I1

| Interrupt Control Register I1 | | When reset: $0000_2$ | | When powered down: State retained | R/W<br>TAI1/TI1A |
|---|---|---|---|---|---|
| $I1_3$ | INT pin input control bit Note 2 | 0 | Disables input | | |
| | | 1 | Enables input | | |
| $I1_2$ | INT pin interrupt active waveform/ return level select bit Note 2 | 0 | Falling waveform/low level (SNZI0 instruction recognizes low level) | | |
| | | 1 | Rising waveform/high level (SNZI0 instruction recognizes high level) | | |
| $I1_1$ | INT pin edge detection circuit control bit | 0 | Detects one edge | | |
| | | 1 | Detects both edges | | |
| $I1_0$ | INT pin timer 1 count start synchronizing circuit select bit | 0 | Deselects timer 1 count start synchronizing circuit | | |
| | | 1 | Selects timer 1 count start synchronizing circuit | | |

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When the contents of these bits ($I1_2$ or $I1_3$) are changed, the external interrupt request flag (EXF0) may be set.

## 3.4 Timer Control Register PA

Table 3.4 shows the bit configuration of Timer Control Register PA.

For write to the register PA, first set a value in the register A and then use the TPAA instruction.

Table 3.4 Bit Configuration of Timer Control Register PA

| Timer Control Register PA | | When reset: $0_2$ | | When powered down: $0_2$ | W<br>TPAA |
|---|---|---|---|---|---|
| $PA_0$ | Prescaler control bit | 0 | Stop (state retained) | | |
| | | 1 | Start | | |

Note 1: The letter W denotes “writable.”

## 3.5 Timer Control Register W1

Table 3.5 shows the bit configuration of Timer Control Register W1.

For write to the register W1, first set a value in the register A and then use the TW1A instruction.

Furthermore, the TAW1 instruction may be used to transfer the content of register W1 to the register A.

Table 3.5 Bit Configuration of Timer Control Register W1

| Timer Control Register W1 | | When reset: $0000_2$ | | When powered down: State retained | R/W TAW1/TW1A |
|---|---|---|---|---|---|
| $W1_3$ | Timer 1 count auto stop circuit select bit Note 2 | 0 | Deselects timer 1 count auto stop circuit | | |
| | | 1 | Selects timer 1 count auto stop circuit | | |
| $W1_2$ | Timer 1 control bit | 0 | Stop (state returned) | | |
| | | 1 | Start | | |
| $W1_1$ | Timer 1 count source select bit Note 3 | $W1_1$ | $W1_0$ | Count source | |
| | | 0 | 0 | PWM signal (PWMOUT) | |
| | | 0 | 1 | Prescaler output (ORCLK) | |
| $W1_0$ | | 1 | 0 | Timer 3 underflow signal (T3UDF) | |
| | | 1 | 1 | CNTR input | |

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: This function is usable only when timer 1 count start synchronizing circuit is selected ($I1_0 = 1$).
Note 3: If CNTR input is selected for the timer 1 count source, port C output is disabled.

## 3.6 Timer Control Register W2

Table 3.6 shows the bit configuration of Timer Control Register W2.

For write to the register W2, first set a value in the register A and then use the TW2A instruction.

Furthermore, the TAW2 instruction may be used to transfer the content of register W2 to the register A.

Table 3.6 Bit Configuration of Timer Control Register W2

| Timer Control Register W2 | | When reset: $0000_2$ | When powered down: $0000_2$ | R/W TAW2/TW2A |
|---|---|---|---|---|
| $W2_3$ | CNTR pin output control bit | 0 | Disables CNTR pin output | |
| | | 1 | Enables CNTR pin output | |
| $W2_2$ | PWM signal high period extend function control bit | 0 | Disables PWM signal high period extend function | |
| | | 1 | Enables PWM signal high period extend function | |
| $W2_1$ | Timer 2 control bit | 0 | Stop (state retained) | |
| | | 1 | Start | |
| $W2_0$ | Timer 2 count source select bit | 0 | $X_{IN}$ input | |
| | | 1 | Prescaler output (ORCLK) divided by 2 | |

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

## 3.7 Timer Control Register W3

Table 3.7 shows the bit configuration of Timer Control Register W3.

For write to the register W3, first set a value in the register A and then use the TW3A instruction.

Furthermore, the TAW3 instruction may be used to transfer the content of register W3 to the register A.

Table 3.7 Bit Configuration of Timer Control Register W3

| Timer Control Register W3 | | When reset: $0000_2$ | | When powered down: State retained | R/W TAW3/TW3A |
|---|---|---|---|---|---|
| $W3_3$ | Timer 3 count source select bit | 0 | $X_{CIN}$ input | | |
| | | 1 | Prescaler output (ORCLK) divided by 2 | | |
| $W3_2$ | Timer 3 control bit | 0 | Stop (initial state) | | |
| | | 1 | Start | | |
| $W3_1$ | Timer 3 count value select bit | $W3_1$ | $W3_0$ | Count value | |
| | | 0 | 0 | Generates underflow every 8,192 counts | |
| | | 0 | 1 | Generates underflow every 16,384 counts | |
| $W3_0$ | | 1 | 0 | Generates underflow every 32,768 counts | |
| | | 1 | 1 | Generates underflow every 65,536 counts | |

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

## 3.8 Timer Control Register W4

Table 3.8 shows the bit configuration of Timer Control Register W4.

For write to the register W4, first set a value in the register A and then use the TW4A instruction.

Furthermore, the TAW4 instruction may be used to transfer the content of register W4 to the register A.

Table 3.8 Bit Configuration of Timer Control Register W4

| Timer Control Register W4 | | When reset: $0000_2$ | When powered down: State retained | R/W TAW4/TW4A |
|---|---|---|---|---|
| $W4_3$ | Timer LC control bit | 0 | Stop (state retained) | |
| | | 1 | Start | |
| $W4_2$ | Timer LC count source select bit | 0 | Bit 4 of timer 3 ($T3_4$) | |
| | | 1 | System clock (STCK) | |
| $W4_1$ | CNTR pin output auto control circuit select bit | 0 | Deselects CNTR pin output auto control circuit | |
| | | 1 | Selects CNTR pin output auto control circuit | |
| $W4_0$ | CNTR pin input count edge select bit | 0 | Falling edge | |
| | | 1 | Rising edge | |

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during timer setting.

## 3.9 Port Output Mode Control Register FR2

Table 3.9 shows the bit configuration of Port Output Mode Control Register FR2.

For write to the register FR2, first set a value in the register A and then use the TFR2A instruction.

Table 3.9 Bit Configuration of Port Output Mode Control Register FR2

| Port Output Mode Control Register FR2 | | When reset: $0000_2$ | | When powered down: State retained | W<br>TFR2A |
|---|---|---|---|---|---|
| $FR2_3$ | Port $P3_2$ and $P3_3$ output mode select bit | 0 | N-channel open-drain output | | |
| | | 1 | CMOS output | | |
| $FR2_2$ | Port $P3_0$ and $P3_1$ output mode select bit | 0 | N-channel open-drain output | | |
| | | 1 | CMOS output | | |
| $FR2_1$ | Port $D_5$ output mode select bit | 0 | N-channel open-drain output | | |
| | | 1 | CMOS output | | |
| $FR2_0$ | Port $D_4$ output mode select bit | 0 | N-channel open-drain output | | |
| | | 1 | CMOS output | | |

Note 1: The letter W denotes “writable.”

Note 2: : Unused bits during timer setting.

# 4. Timer Application Example

## 4.1 CNTR Output Operation: Buzzer Output

Point : The square wave output from timer 2 can be used for buzzer output as its application.

Specification : When system clock frequency = 4 4MHz, a square wave in frequency of approximately 4 kHz is output from the CNTR pin. Also, a timer 2 interrupt is generated at the same time.

Figure 4.1 shows an example of a peripheral circuit. Figure 4.3 shows an example of how to set the registers for CNTR output.

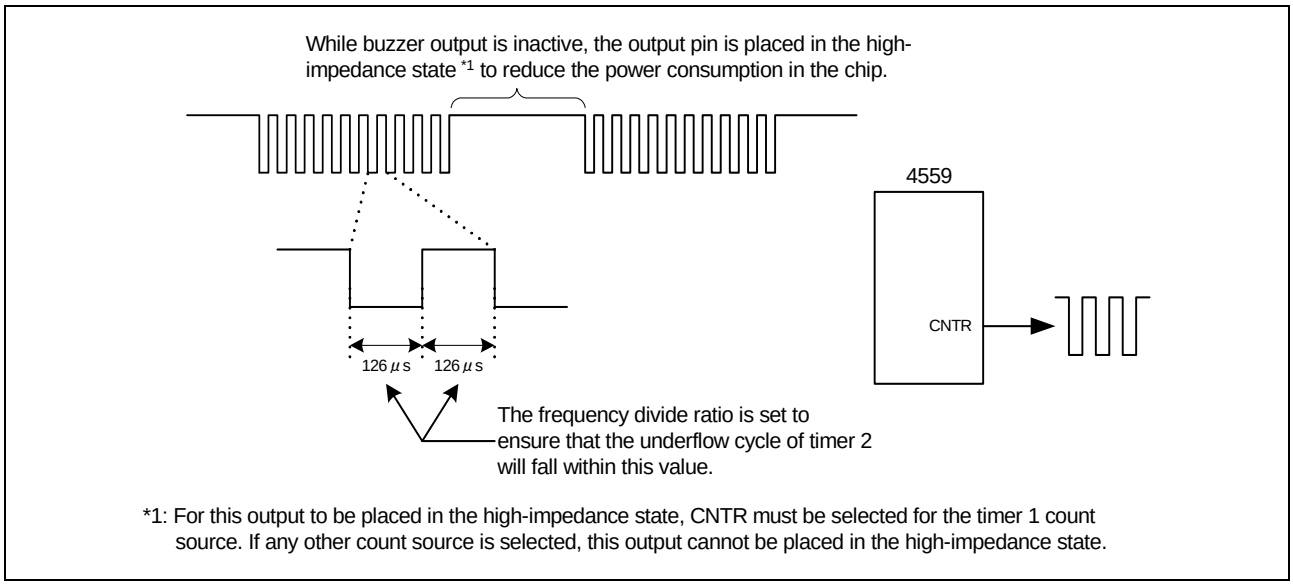



Figure 4.1 Example of a Peripheral Circuit

## 4.2 CNTR Input Operation: Event Count

Point : A signal (rising waveform) input from the CNTR pin can be used as an event for count operation.

Specification : Low-frequency pulses are input as the count source for timer 1 from the outside to the CNTR pin, and a timer 1 interrupt is generated every 100 counts.

Figure 4.4 shows an example of how to set the registers for CNTR input.

## 4.3 Timer Operation: Timer Start by External Input

Point : A fixed length of time can be measured using external input.

Specification : Timer 1 is triggered to start counting by INT input and an interrupt is generated 1 ms later.

Figure 4.5 shows an example of how to set the registers for timer 1 to be started by external 0 input.

## 4.4 Timer Operation: Fixed-cycle Counter by Timer 3

Point : Exact time can be measured using a 32.768 kHz crystal resonator, making it possible to create a highly accurate time-of-day clock.

Specification : A timer 3 interrupt is generated every 250 ms synchronously with the timing signal derived by dividing the sub-clock frequency (f(XCIN) = 32.768 kHz) with timer 3.

Figure 4.6 shows an example of how to set the registers for a fixed-cycle counter by timer 3.

## 4.5 Watchdog Timer

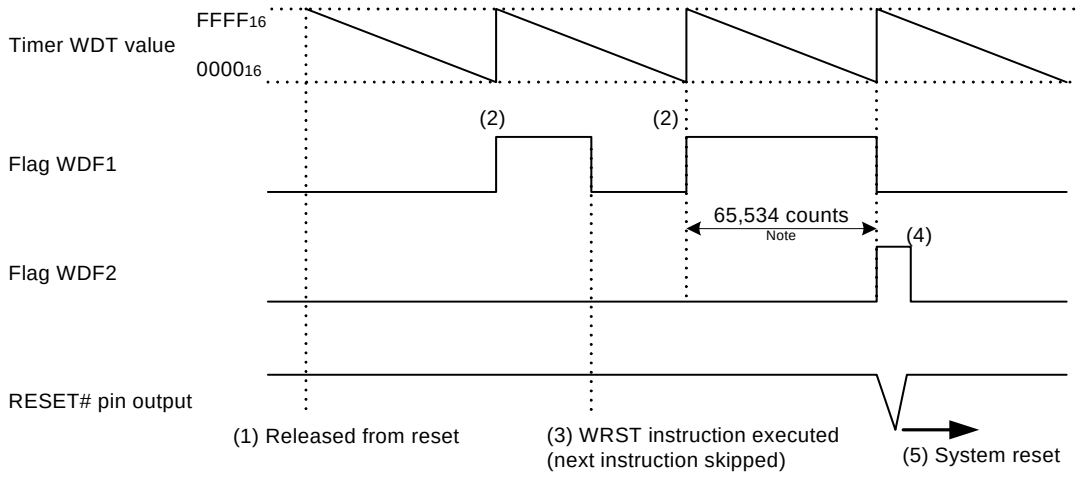
The watchdog timer function offers a means for restoring the chip into a reset state when, for example, a program has gone wild and could not be executed normally.

When the watchdog timer function is enabled, always be sure that the WRST instruction is executed at intervals equal to or less than 65,534 counts of a 16-bit timer (i.e., at intervals equal to or less than 65,534 machine cycles).

Point : While operating normally, the WRST instruction is always executed within 65,534 counts of a 16-bit timer. If the program goes wild, the WRST instruction will no longer be executed, causing the chip to be reset.

Specification : Using a system clock frequency of 4.0 MHz, this function detects program runaway by executing the WRST instruction within 49 ms.

Figure 4.2 schematically shows the watchdog timer function. Figure 4.7 shows an example for using the watchdog timer.




(1) After reset (after program start), the timer WDT starts counting down.
(2) When the timer WDT underflows upon reaching the minimum count, the flag WDF1 is set to 1.
(3) When the WRST instruction is executed, the flag WDF1 is cleared to 0 and the next instruction is skipped.
(4) If the timer WDT underflows while the flag WDF1 = 1, the flag WDF2 is set to 1 and a watchdog reset signal is output.
(5) The watchdog reset signal causes the output transistor of the RESET# pin to turn on, thereby generating a system reset.

Note: Since the count source for the timer WDT is the instruction clock, the number of counts is the same as the number of machine cycles.

Figure 4.2 Watchdog Timer Function

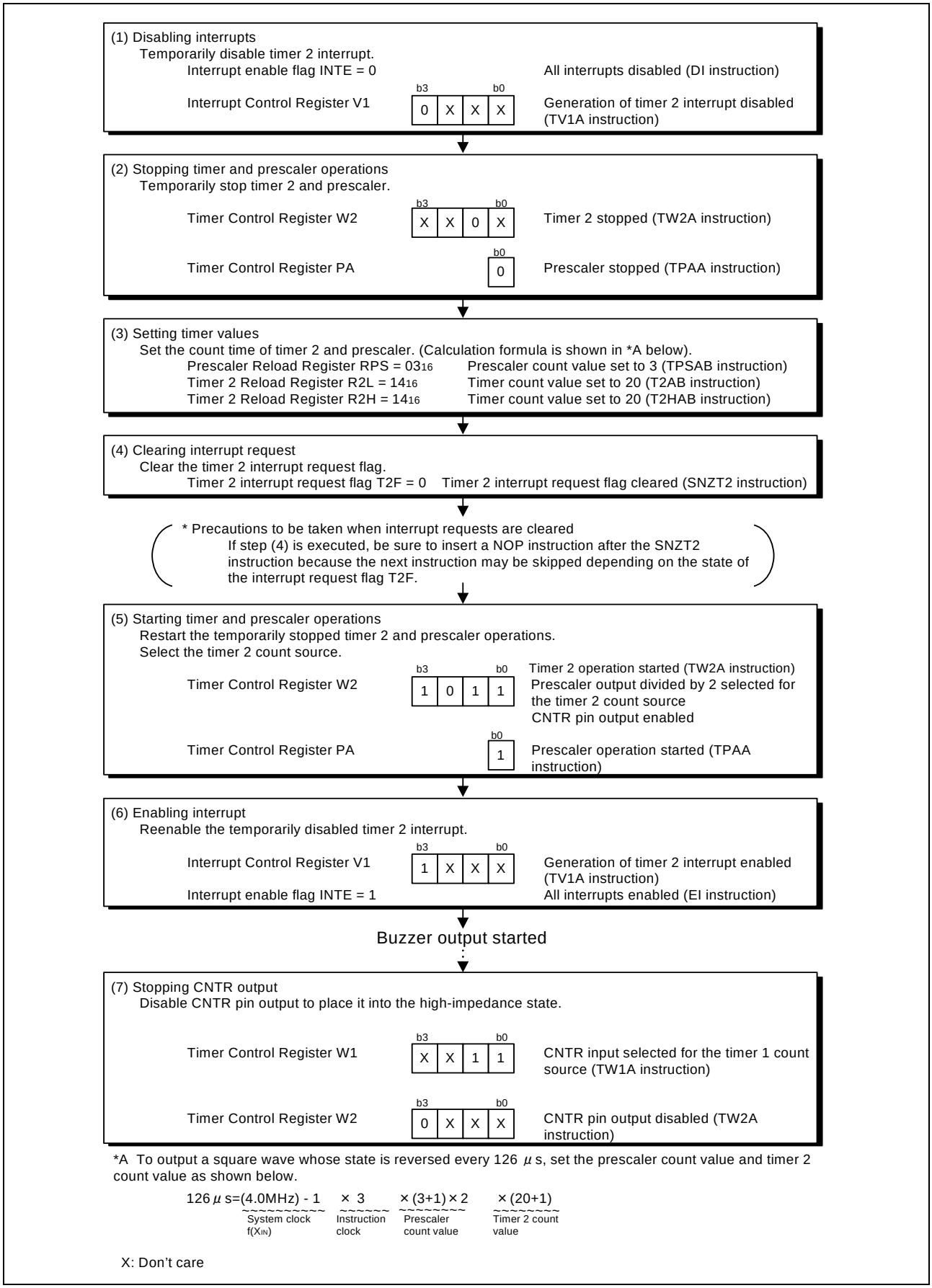



Figure 4.3 Example of CNTR Output Setting

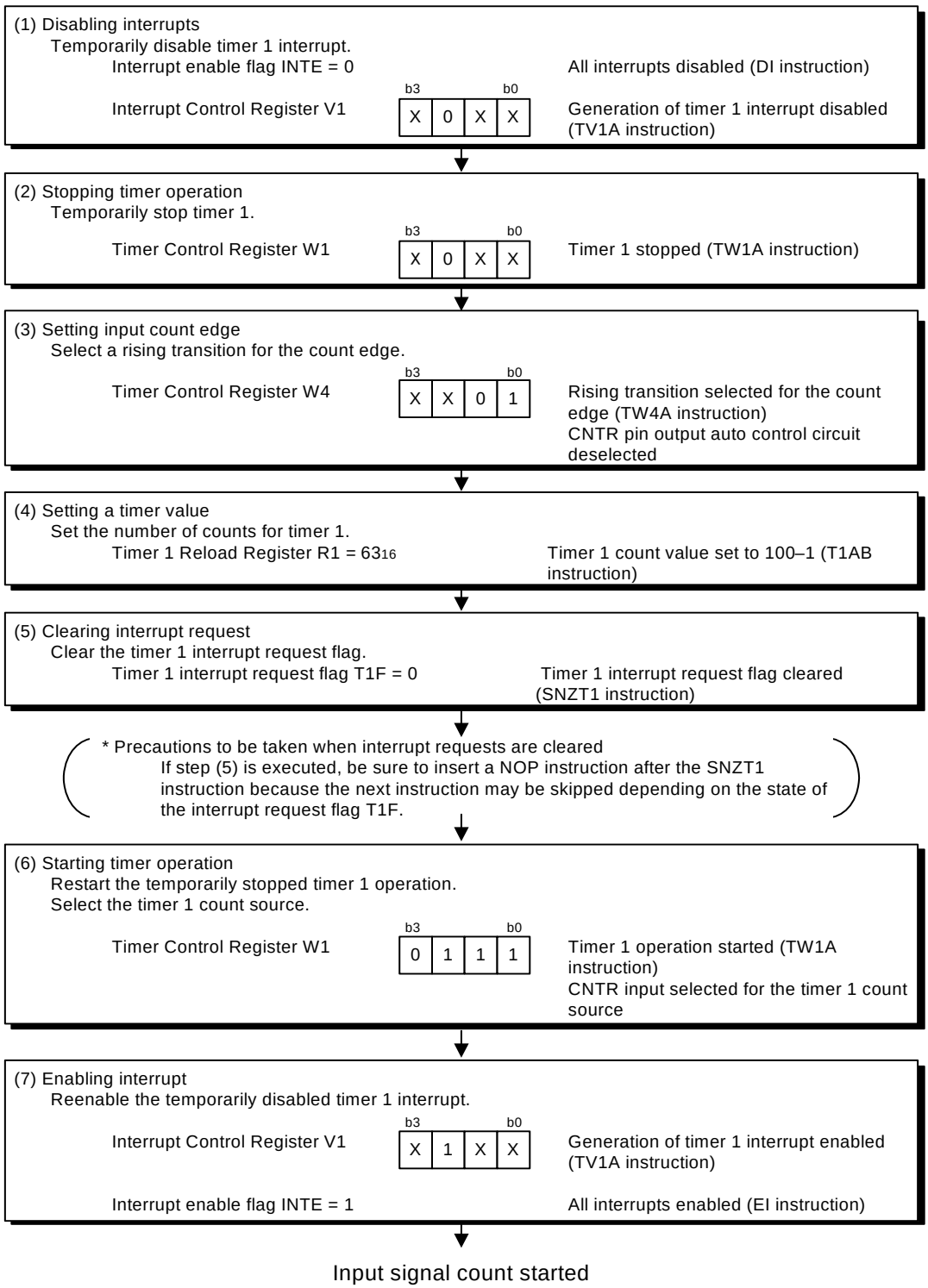



Figure 4.4 Example of CNTR Input Setting

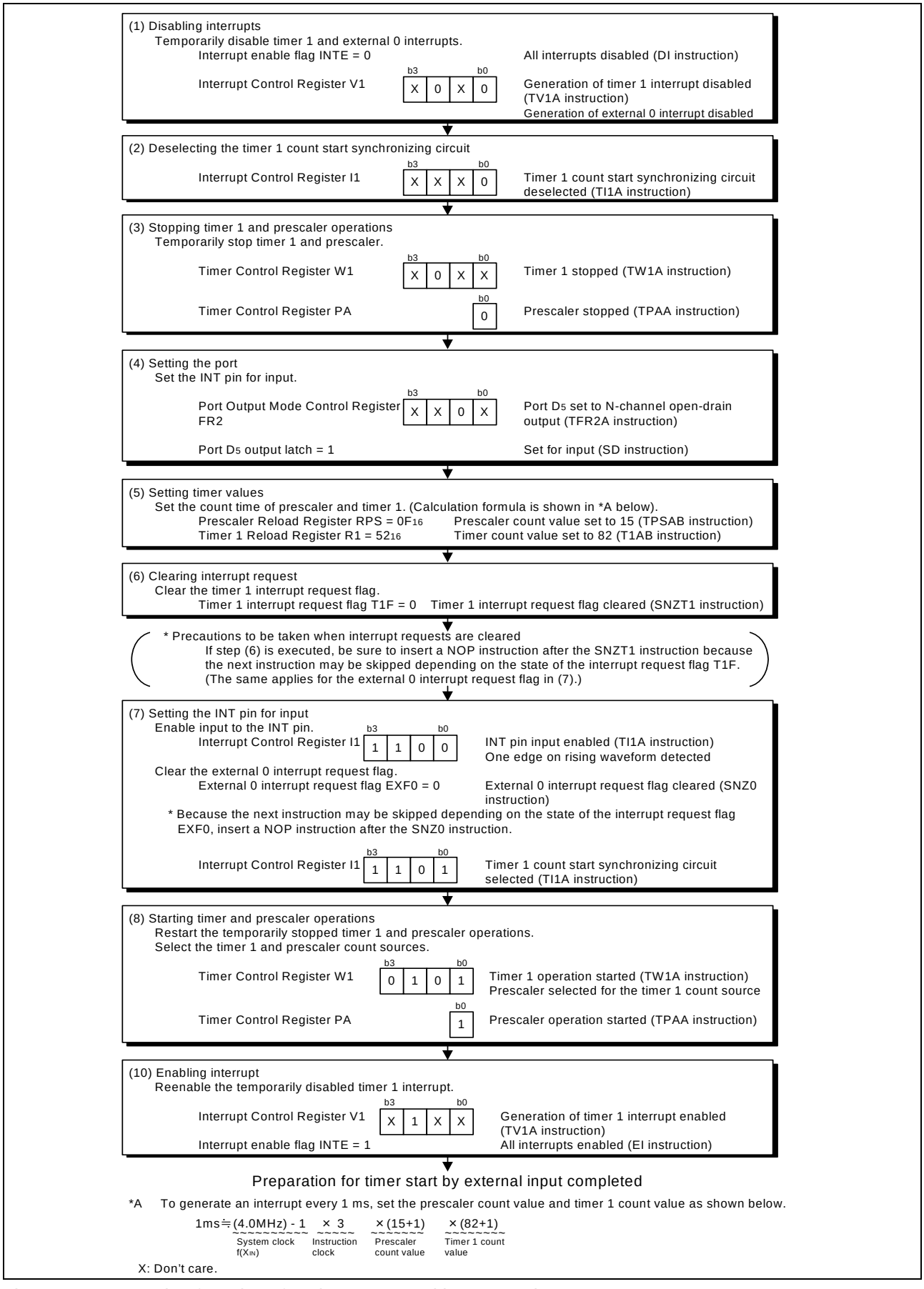



Figure 4.5 Example of Settings for Timer 1 Started by External 0 Input

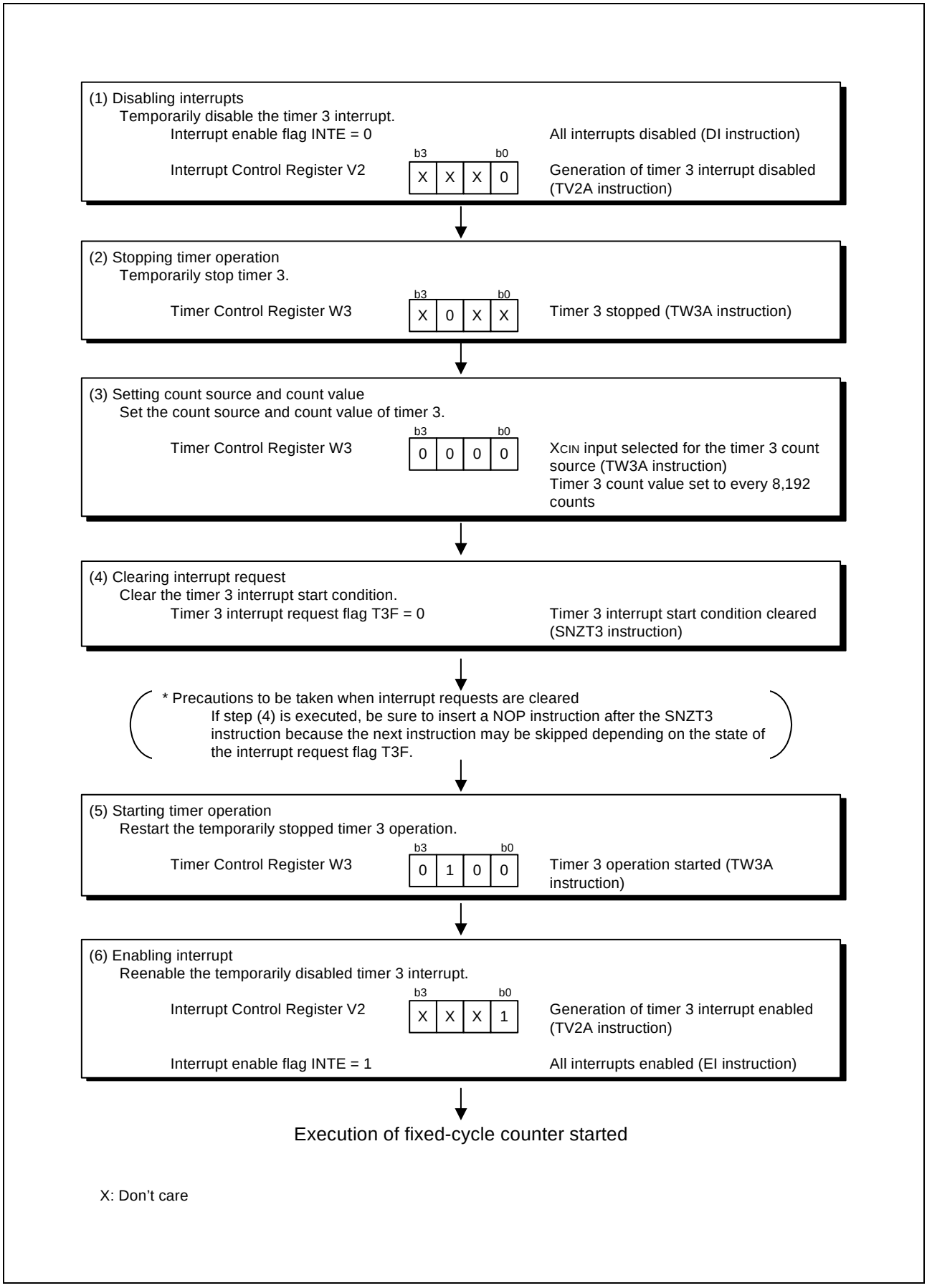



Figure 4.6 Example of Settings for Fixed-cycle Counter by Timer 3

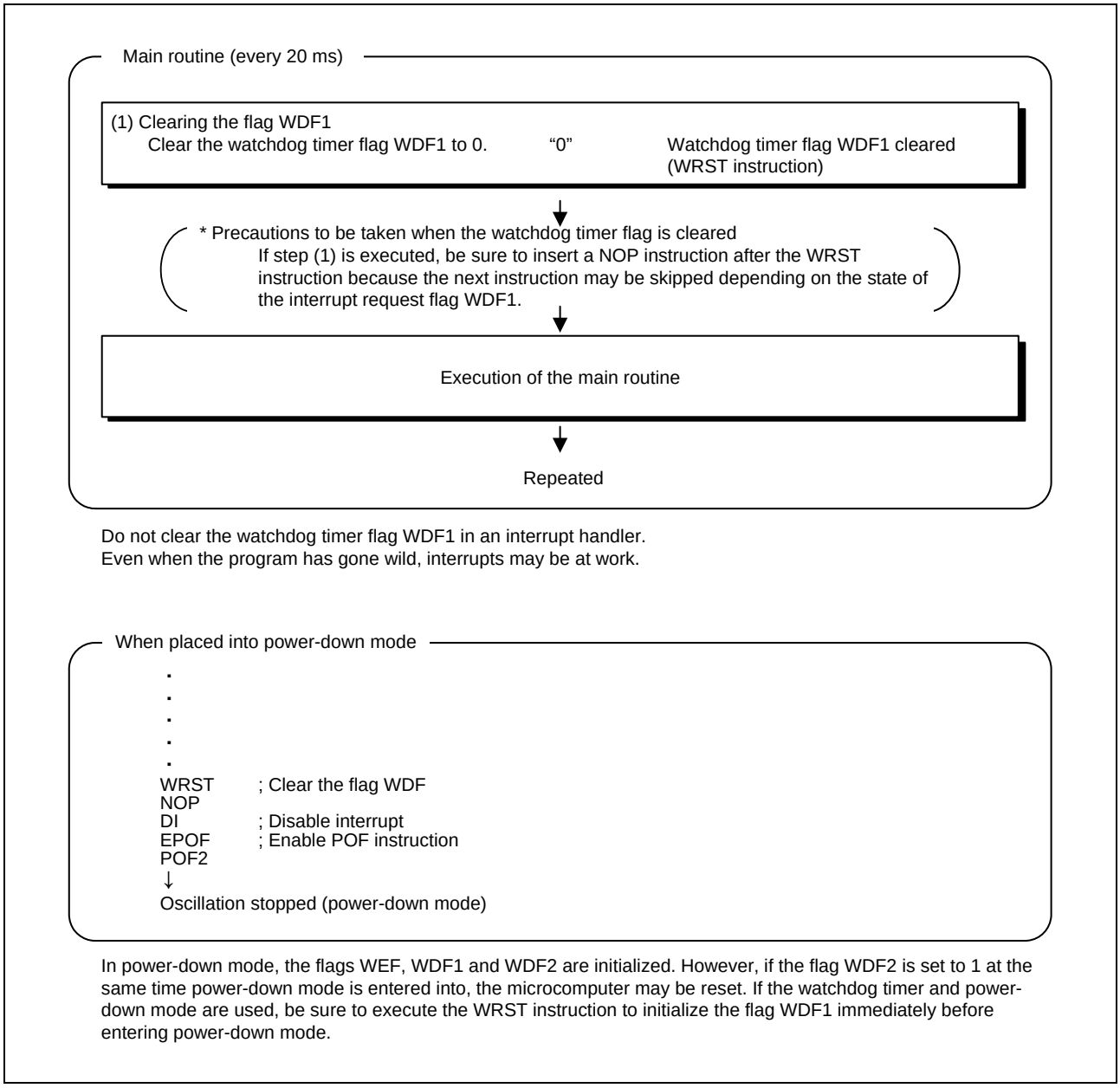



Figure 4.7 Example for Using the Watchdog Timer

## 5. Sample Programs

Sample programs are available from the Renesas Technology Web site. To download one, click the screen menu "Application Note" on the left side of 4559 group Web page.

## 6. Reference Documents

Data sheet
4559 Group Data Sheet

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