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4559 Group

Interrupts

1. Abstract

This document shows an example of how to set interrupts in the 4559 group of Renesas microcomputers and an application example for using those interrupts.

2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

- Microcomputer : 4559 group
- Oscillation frequency : 4 MHz (external 0, timer 1); 2 MHz (timer 2) as main clock f(X_{IN}), however; 32.768 kHz (timer 3) as sub-clock f(X_{CIN}), however
- System clock : Used in through mode (not frequency divided)

Please note that the sample program for the 4559 group may somewhere in it manipulate the bits of unused functions for reasons of bit arrangement in the control registers. The values of these bits in a user system should be set to suit the usage condition of the system.

In this application note, explanation is made of an example of interrupt setting method and an application example with respect to the following:

- External 0 interrupt
- Timer 1 interrupt
- Timer 2 interrupt
- Timer 3 interrupt

3. Related Registers

3.1 Interrupt Control Register V1

Table 3.1 shows the bit configuration of Interrupt Control Register V1.
For write to the register V1, first set a value in the register A and then use the TV1A instruction.
Furthermore, the TAV1 instruction may be used to transfer the content of register V1 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V1

Interrupt Control Register V1		When reset: 0000_2	When powered down: 0000_2	R/W TAV1/TV1A
$V1_3$	Timer 2 interrupt enable bit	0	Disables interrupt generation (SNZT2 instruction effective)	
		1	Enables interrupt generation (SNZT2 instruction has no effect)	
$V1_2$	Timer 1 interrupt enable bit	0	Disables interrupt generation (SNZT1 instruction effective)	
		1	Enables interrupt generation (SNZT1 instruction has no effect)	
$V1_1$	Unused	0	This bit has no functions assigned, but can be read/written.	
		1		
$V1_0$	External 0 interrupt enable bit	0	Disables interrupt generation (SNZ0 instruction effective)	
		1	Enables interrupt generation (SNZ0 instruction has no effect)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: : Unused bits during interrupt setting.

3.2 Interrupt Control Register V2

Table 3.2 shows the bit configuration of Interrupt Control Register V2.
For write to the register V2, first set a value in the register A and then use the TV2A instruction.
Furthermore, the TAV2 instruction may be used to transfer the content of register V2 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register V2

Interrupt Control Register V2		When reset: 0000_2	When powered down: 0000_2	R/W TAV2/TV2A
$V2_3$	Unused	0	This bit has no functions assigned, but can be read/written.	
		1		
$V2_2$	Unused	0	This bit has no functions assigned, but can be read/written.	
		1		
$V2_1$	Unused	0	This bit has no functions assigned, but can be read/written.	
		1		
$V2_0$	Timer 3 interrupt enable bit	0	Disables interrupt generation (SNZT3 instruction effective)	
		1	Enables interrupt generation (SNZT3 instruction has no effect)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: : Unused bits during interrupt setting.

3.3 Interrupt Control Register I1

Table 3.3 shows the bit configuration of Interrupt Control Register I1.

For write to the register I1, first set a value in the register A and then use the TI1A instruction.

Furthermore, the TAI1 instruction may be used to transfer the content of register I1 to the register A.

Table 3.3 Bit Configuration of Interrupt Control Register I1

Interrupt Control Register I1		When reset: 0000_2		When powered down: State retained	R/W TAI1/TI1A
$I1_3$	INT pin input control bit Note 2	0	Disables input		
		1	Enables input		
$I1_2$	INT pin interrupt active waveform/ return level select bit Note 2	0	Falling waveform/low level (SNZI0 instruction recognizes low level on INT pin)		
		1	Rising waveform/high level (SNZI0 instruction recognizes high level on INT pin)		
$I1_1$	INT pin edge detection circuit control bit	0	Detects one edge		
		1	Detects both edges		
$I1_0$	INT pin timer 1 count start synchronizing circuit select bit	0	Deselects timer 1 count start synchronizing circuit		
		1	Selects timer 1 count start synchronizing circuit		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When the contents of these bits ($I1_2$ or $I1_3$) are changed, the external interrupt request flag (EXF0) may be set.

3.4 Timer Control Register PA

Table 3.4 shows the bit configuration of Timer Control Register PA.

For write to the register PA, first set a value in the register A and then use the TPAA instruction.

Table 3.4 Bit Configuration of Timer Control Register PA

Timer Control Register PA		When reset: 0_2		When powered down: 0_2	W TPAA
PA_0	Prescaler control bit	0	Stop (state retained)		
		1	Start		

Note 1: The letter W denotes “writable.”

3.5 Timer Control Register W1

Table 3.5 shows the bit configuration of Timer Control Register W1.

For write to the register W1, first set a value in the register A and then use the TW1A instruction.

Furthermore, the TAW1 instruction may be used to transfer the content of register W1 to the register A.

Table 3.5 Bit Configuration of Timer Control Register W1

Timer Control Register W1		When reset: 0000_2		When powered down: State retained	R/W TAW1/TW1A
$W1_3$	Timer 1 count auto stop circuit select bit Note 2	0	Deselects timer 1 count auto stop circuit		
		1	Selects timer 1 count auto stop circuit		
$W1_2$	Timer 1 control bit	0	Stop (state retained)		
		1	Start		
$W1_1$	Timer 1 count source select bit Note 3	$W1_1$	$W1_0$	Count source	
		0	0	PWM signal (PWMOUT)	
		0	1	Prescaler output (ORCLK)	
$W1_0$		1	0	Timer 3 underflow signal (T3UDF)	
		1	1	CNTR input	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: This function is usable only when timer 1 count start synchronizing circuit is selected ($I1_0 = 1$).
Note 3: If CNTR input is selected for the timer 1 count source, port C output is disabled.

3.6 Timer Control Register W2

Table 3.6 shows the bit configuration of Timer Control Register W2.

For write to the register W2, first set a value in the register A and then use the TW2A instruction.

Furthermore, the TAW2 instruction may be used to transfer the content of register W2 to the register A.

Table 3.6 Bit Configuration of Timer Control Register W2

Timer Control Register W2		When reset: 0000_2	When powered down: 0000_2	R/W TAW2/TW2A
$W2_3$	CNTR pin output control bit	0	Disables CNTR pin output	
		1	Enables CNTR pin output	
$W2_2$	PWM signal high period extend function control bit	0	Disables PWM signal high period extend function	
		1	Enables PWM signal high period extend function	
$W2_1$	Timer 2 control bit	0	Stop (state retained)	
		1	Start	
$W2_0$	Timer 2 count source select bit	0	X_{IN} input	
		1	Prescaler output (ORCLK) divided by 2	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

3.7 Timer Control Register W3

Table 3.7 shows the bit configuration of Timer Control Register W3.

For write to the register W3, first set a value in the register A and then use the TW3A instruction.

Furthermore, the TAW3 instruction may be used to transfer the content of register W3 to the register A.

Table 3.7 Bit Configuration of Timer Control Register W3

Timer Control Register W3		When reset: 0000_2		When powered down: State retained	R/W TAW3/TW3A
$W3_3$	Timer 3 count source select bit	0	X_{CIN} input		
		1	Prescaler output (ORCLK) divided by 2		
$W3_2$	Timer 3 control bit	0	Stop (initial state)		
		1	Start		
$W3_1$	Timer 3 count value select bit	$W3_1$	$W3_0$	Count value	
		0	0	Generates underflow every 8,192 counts	
		0	1	Generates underflow every 16,384 counts	
$W3_0$		1	0	Generates underflow every 32,768 counts	
		1	1	Generates underflow every 65,536 counts	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

3.8 Port Output Mode Control Register FR2

Table 3.8 shows the bit configuration of Port Output Mode Control Register FR2.

For write to the register FR2, first set a value in the register A and then use the TFR2A instruction.

Table 3.8 Bit Configuration of Port Output Mode Control Register FR2

Port Output Mode Control Register FR2		When reset: 0000_2		When powered down: State retained	W TFR2A
$FR2_3$	Port $P3_2$ and $P3_3$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR2_2$	Port $P3_0$ and $P3_1$ output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR2_1$	Port D_5 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		
$FR2_0$	Port D_4 output mode select bit	0	N-channel open-drain output		
		1	CMOS output		

Note 1: The letter W denotes “writable.”

Note 2: : Unused bits during interrupt setting.

4. Application Example for Using the Interrupts

4.1 External 0 Interrupt

The INT pin is an external interrupt pin whose active waveform is selectable. A falling edge (high to low transition), rising edge (low to high transition) and both edges (high to low and low to high transitions) on this pin can be recognized.

Point : A falling edge (high to low transition), rising edge (low to high transition) or both edges (high to low and low to high transitions) can be used as a trigger for external 0 interrupt.

Specification : External 0 interrupt is generated by both edges (high to low and low to high transitions) of an external signal.

Figure 4.1 shows an example of external 0 interrupt operation. Figure 4.2 shows an example of external 0 interrupt setting.

4.2 Timer 1 Interrupt

Timer 1 permits a fixed-cycle interrupt to be used based on a set timer value.

Point : A fixed-cycle interrupt based on an underflow signal of timer 1 can be used.

Specification : A timer 1 interrupt is generated every 1 ms synchronously with the timing signal derived by dividing the system clock frequency (= 4.0 MHz) with the prescaler and timer 1.

Figure 4.3 shows an example of how to set a timer 1 fixed-cycle interrupt.

4.3 Timer 2 Interrupt

Timer 2 permits a fixed-cycle interrupt to be used based on a set timer value.

Point : A fixed-cycle interrupt based on an underflow signal of timer 2 can be used.

Specification : A timer 2 interrupt is generated every 0.125 ms synchronously with the timing signal derived by dividing the system clock frequency (= 2.0 MHz) with timer 2.

Figure 4.4 shows an example of how to set a timer 2 fixed-cycle interrupt.

4.4 Timer 3 Interrupt

Timer 3 permits a fixed-cycle interrupt to be used based on a set timer value.

Point : A fixed-cycle interrupt based on an underflow signal of timer 3 can be used.

Specification : A timer 3 interrupt is generated every 500 ms synchronously with the timing signal derived by dividing the sub-clock frequency (f(XCIN) = 32.768 kHz) with timer 3.

Figure 4.5 shows an example of how to set a timer 3 fixed-cycle interrupt.

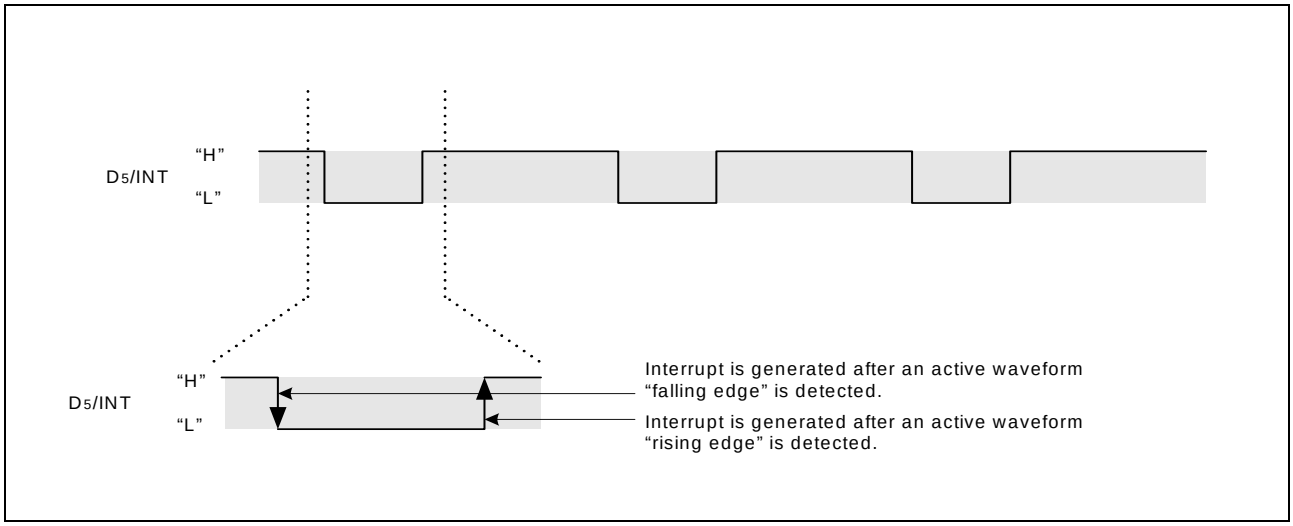

Figure 4.1 Example of External 0 Interrupt Operation

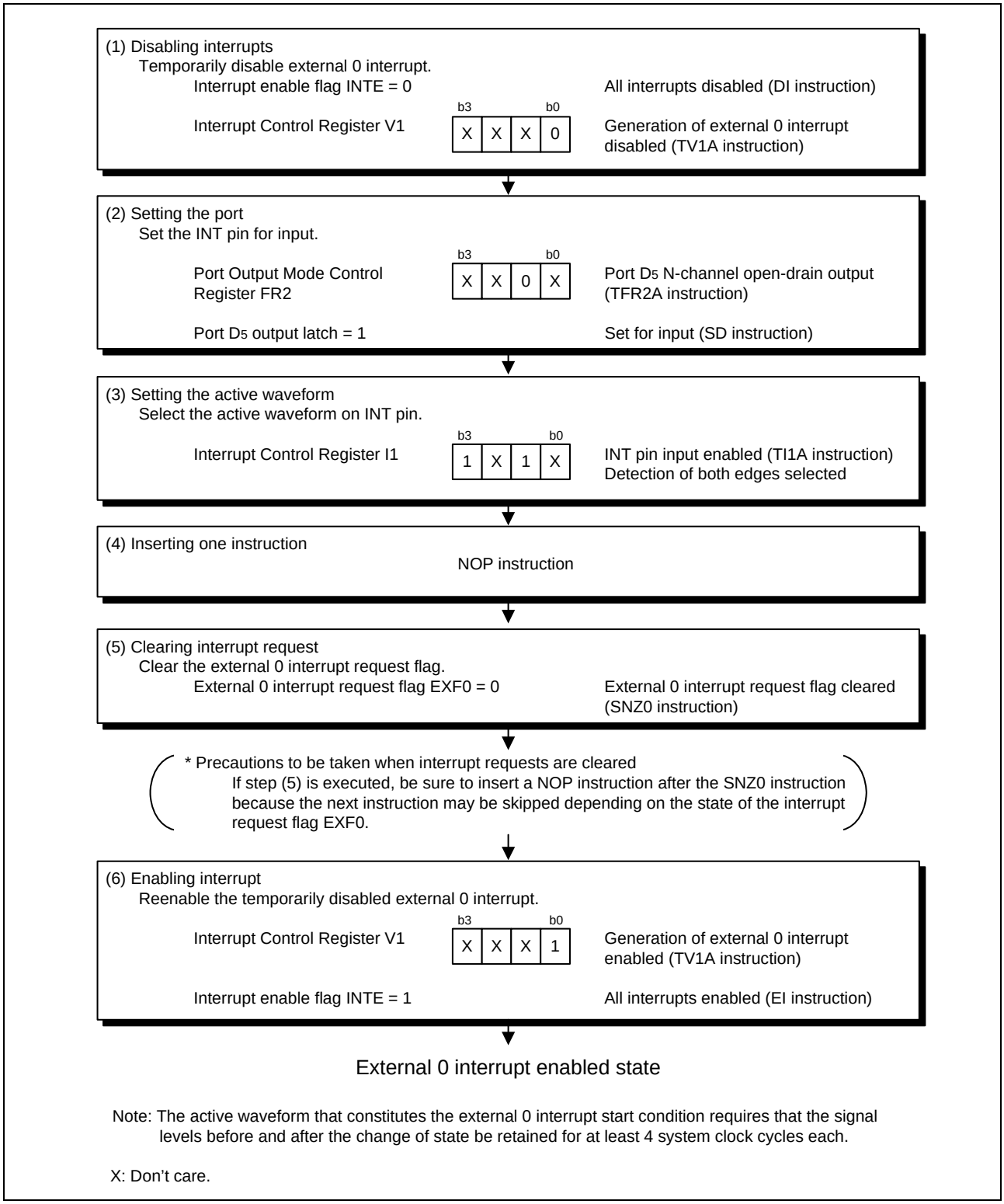

Figure 4.2 Example of External 0 Interrupt Setting

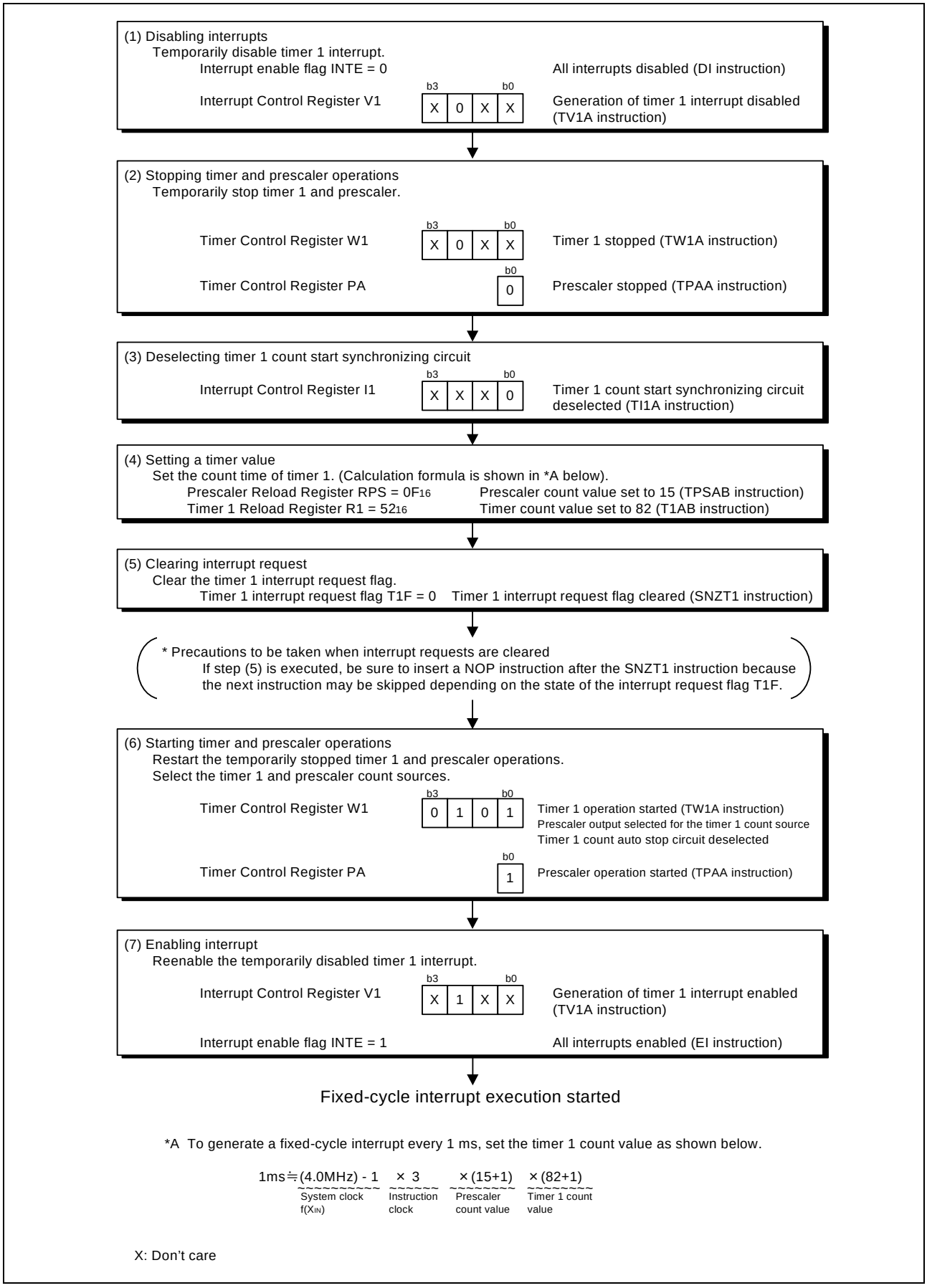

Figure 4.3 Example of Timer 1 Fixed-cycle Interrupt Setting

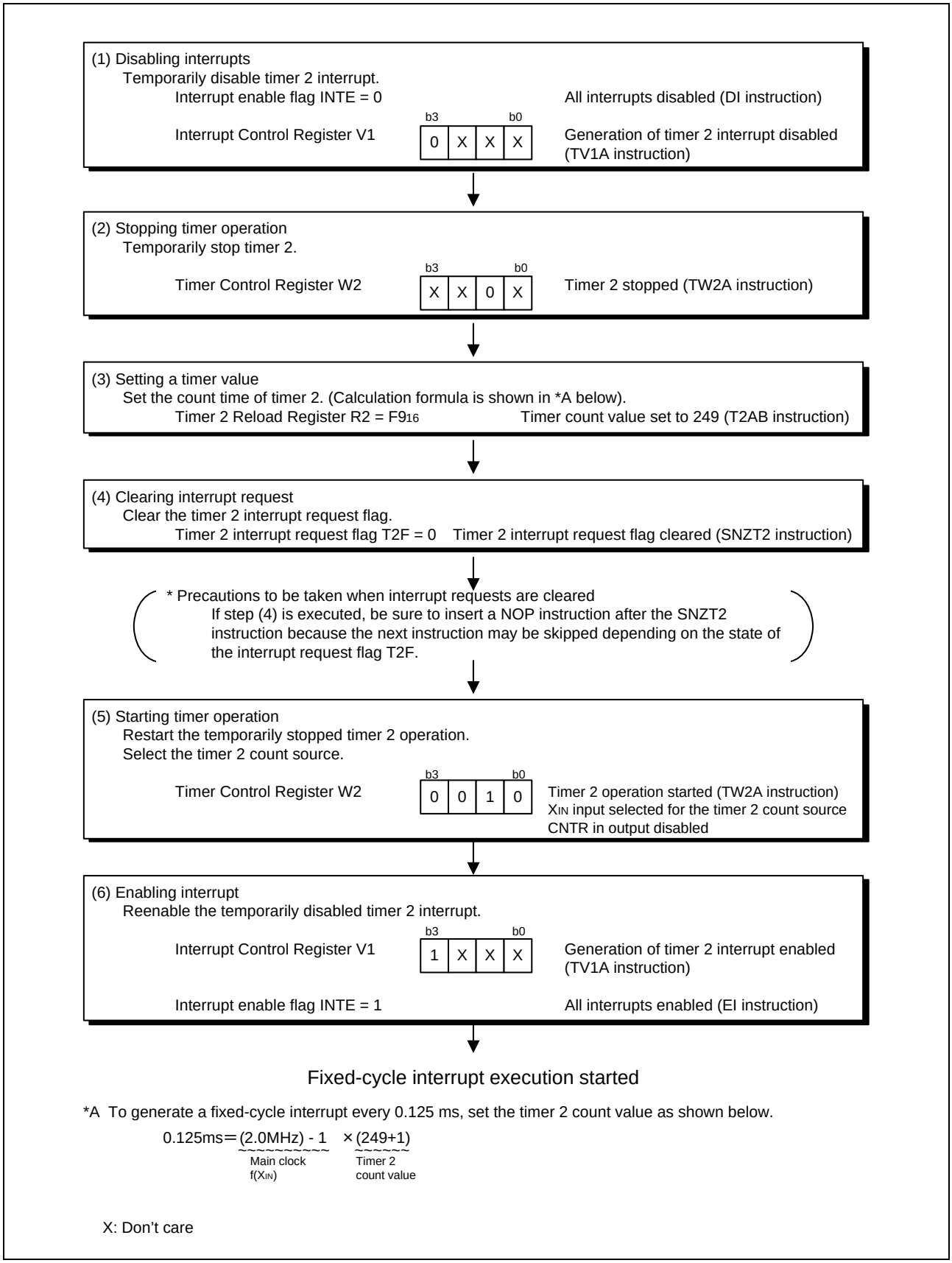

Figure 4.4 Example of Timer 2 Fixed-cycle Interrupt Setting

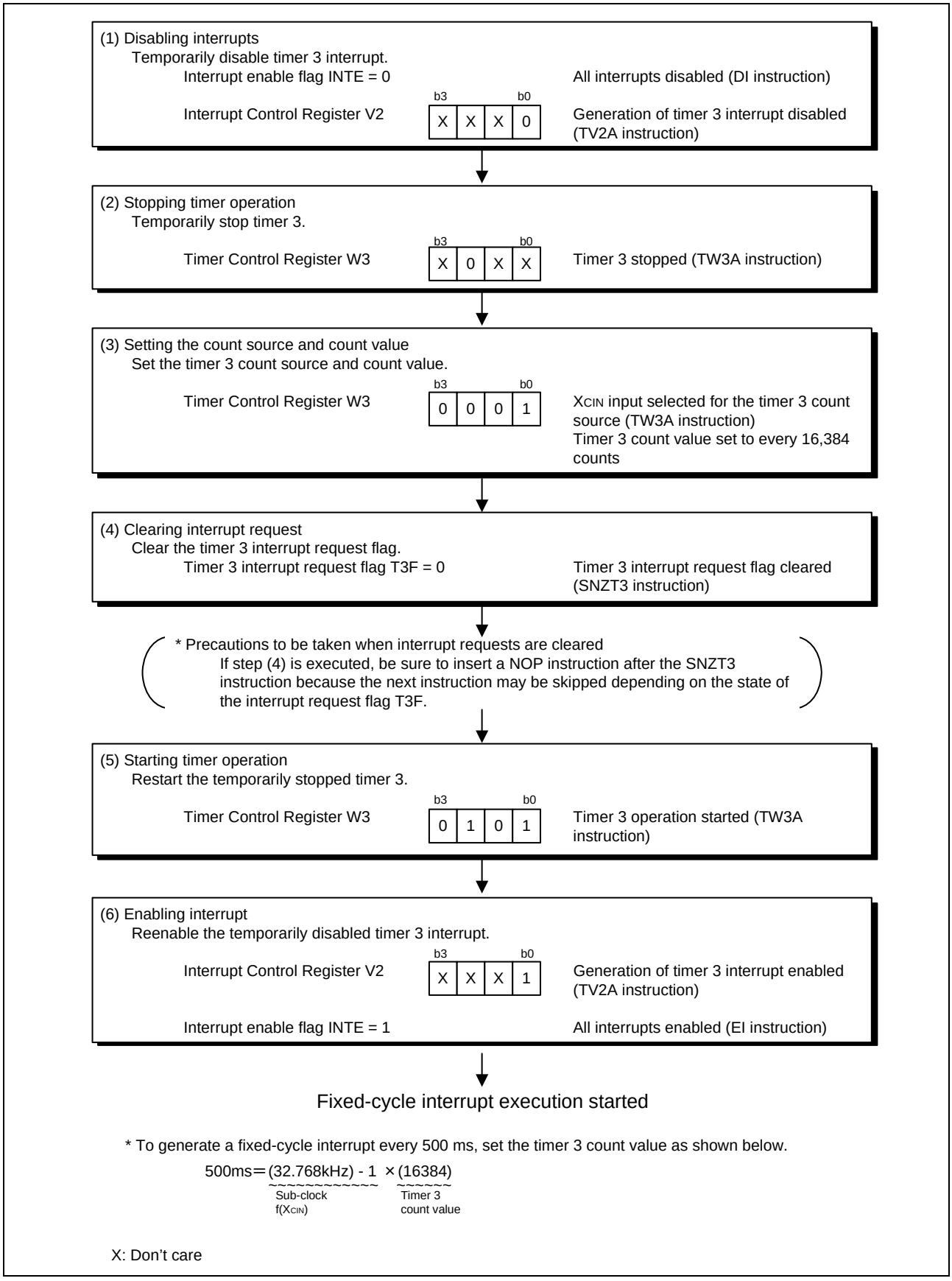

Figure 4.5 Example of Timer 3 Fixed-cycle Interrupt Setting

5. Sample Programs

Sample programs are available from the Renesas Technology Web site. To download one, click the screen menu "Application Note" on the left side of 4559 group Web page.

6. Reference Documents

Data sheet
4559 Group Data Sheet

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Renesas Technology Web site:
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		Page	Points
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