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4552 Group

Timer 1, Timer 2 (PWM Signal Output Control: Remote-Control Carrier Wave Output Control)

1. Abstract

The following article introduces and shows an application example of the PWM signal (remote-control carrier wave) output from CNTR pin by Timer 1 or Timer 2 of the 4552 Group.

2. Introduction

The explanation of this issue is applied to the following condition:

- Applicable MCU: 4552 Group
- Oscillation frequency: 3.64 MHz
- Operation mode: Frequency/4 mode



3. Contents

3.1 Application Example of PWM Signal Output Control

Outline

- Generate the PWM signal (remote-control carrier wave) by Timer 2.
- Control the output of the PWM signal to the CNTR pin by Timer 1.
- Switch the ON/OFF of the output of the CNTR pin every Timer 1 underflow.
- Timer 1 count source: PWM signal Change the interval of ON/OFF of the output of the CNTR pin by change of the Timer 1 set value.
- Even when the output of the PWM signal to the CNTR pin is not performed, the PWM signal is generated internall

Specifications

- PWM signal : 37.9 kHz, Duty 1/3
- CNTR output: Standard interval T = 0.55 ms, 8T output ON 4T output OFF T output ON

Figure 1 shows the auto-control of CNTR output by Timer 1, and Figure 2 shows the connection of Timer and the dividing ratio.

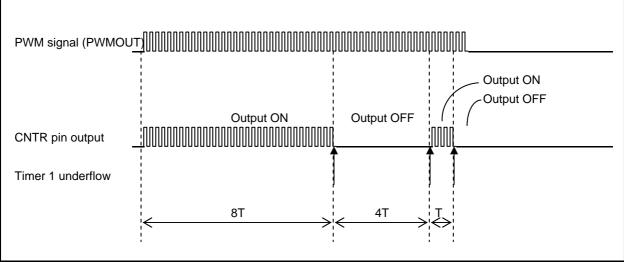


Figure 1 Auto-Control of CNTR Output by Timer 1



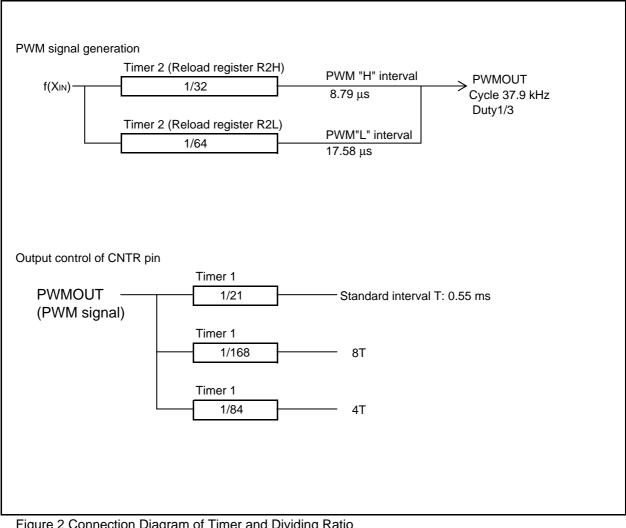
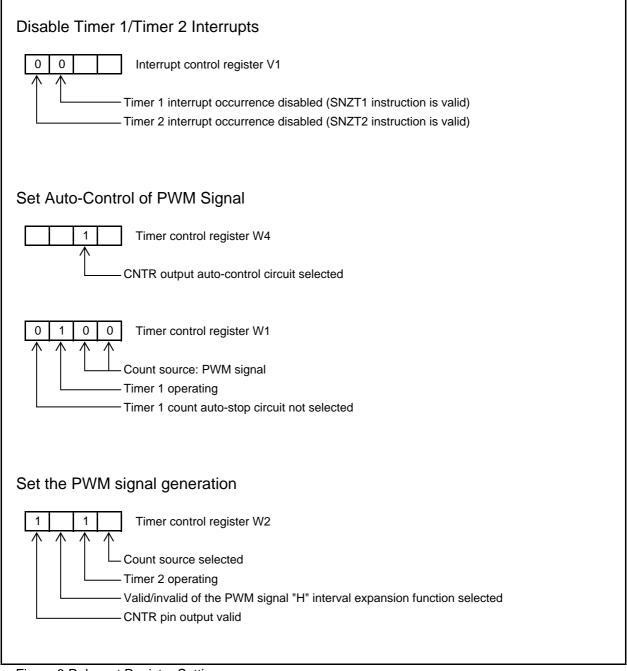


Figure 2 Connection Diagram of Timer and Dividing Ratio



3.2 Relevant Register Setting

Figure 3 shows the relevant register setting.







3.3 Control Procedure

Figure 4 and Figure 5 show the control procedure.

Interrupt control register V/1 / OOVV- [TV/1 / instruction]	X: Set an arbitrary valu
Interrupt control register V1 \leftarrow 00XX ₂ [TV1A instruction]	
Timer 1/Timer 2 interrupt occurrence disabled	
	-
RCP instruction	
C port: no output	
	_
Timer control register W2 \leftarrow XX0X ₂ [TW2A instruction]	
Timer 2: stop	
Timer control register W1 \leftarrow X0XX ₂ [TW1A instruction]	7
Timer 1: stop	
Timer 1 (A9., [T1AD instruction]	7
Timer 1 \leftarrow A8 ₁₆ [T1AB instruction]	
168 (= 8T output ON interval) set to Timer 1.	
Refer to 5.Note on Control of PWM Signal Output	_
	-
T1F \leftarrow 0 [SNZT1 instruction]	
Timer 1 interrupt request flag cleared	
Considering the skip of the next instruction according to the state of flag,	
insert NOP instruction considering after this instruction.	
Timer control register W4 \leftarrow XX1X ₂ [TW4A instruction]	
CNTR pin output auto-control circuit selected	
Timer control register W1 \leftarrow 01002 [TW1A instruction]	7
Timer 1 auto-stop circuit: not selected, Timer 1: operating,	
and count source: PWM signal selected	
Timer 2 reload register R2L \leftarrow 3F ₁₆ [T2AB instruction]	7
· · ·	
Timer 2 reload register R2H \leftarrow 1F ₁₆ [T2HAB instruction]	
PWM signal (carrier wave) set 37.9 kHz•Duty1/3	
	7
Timer control register $W2 \leftarrow 1010_2$ [TW2A instruction]	
Timer 2 count source: XIN input, Timer 2: operating	
PWM signal "H" interval expansion function invalid, CNTR pin output invalid	
PWM signal (carrier wave) generation start	
	7
Timer 1 reload registe R1 \leftarrow 53 ₁₆ [TR1AB instruction]	
Timer 1 reload registe R1 \leftarrow 53 ₁₆ [TR1AB instruction] 84 (= 4T output OFF interval) set to Timer 1.	
с і і	

Figure 4 Control Procedure (1)



Wait Timer 1 underflow	[SNZT1 instruction]	X: Set an arbitrary va
	• •	
) interval = Wait the start of 4T (no output) interval	
Wait in order to prevent what the t	imer 1 underflow and the setting of counter value	-
•	1 are performed simultaneously.	
-	trol of PWM Signal Output	
Refer to 5.Note off Con		
Timer 1 reload register R1	← 1416 [TR1AB instruction]	7
21-1of T (output) interva	· · ·	
· · · /	trol of PWM Signal Output	
Wait Timer 1 underflow	[SNZT1 instruction]	
	put) interval = Wait the start of T (output) interval	
Wait Timer 1 underflow	[SNZT1 instruction]	
The end of T (output) in	terval waited	
Timer control register W2 \leftarrow	XX0X ₂ [TW2A instruction]	
The generation of the P	WM signal (carrier wave) completed	
Timer control register W4 \leftarrow	XX0X ₂ [TW4A instruction]	
The CNTR output auto-	control circuit not selected	
after the output of the P	WM signal is completed	
Control by timer 1 comp	oleted.	
Timer control register W1 \leftarrow	X0XX2 [TW1A instruction]	
Timer 1: stop		

Figure 5 Control Procedure (2)



4. Sample Programming Code

Figure 6 and Figure 7 show the sample programming code.

EX_CNTR:	:: LA0000b; Disable Timer 1• Timer 2 interruptsTV1A; Set 0 to bit 2 of register V1 to use SNZT1 in		-	
	RCP		; C(/CNTR) no output ; * Even if CNTR is us	ed, H output function of port C is valid
	LA	0000b	; CNTR output: invalid • F ; Timer 2: stop	PWM signal "H" interval expansion function: invalid •
	TW2A			
	LA TW1A	0000b	; Switch the Timer 1 auto	-stop circuit from "not select state" to "selected state"
	LA TBA	0Ah	; Set the counter value	for the first output interval 4.4 ms (8T)
	LA	08h	; As T is carrier wave 2	21 counts,
	T1AB		; 21 X 8 = 168 = A8h	
	SNZT1 NOP		; Clear Timer 1 underfl	ow (interrupt request) flag
	LA TW4A	0010b	; In order that the CNT ; set 1 to bit 1 of regist	R output auto-control circuit is selected state, er W4.
	LA	0100b	; Timer 1 auto-stop cire ; Count source: PWM	cuit: not selected • Timer 1: operating • signal
	TW1A			er 1 for the output control first
	LA	03h	; Set for the waveform	of the PWM signal
	TBA		; L • 64 counts	
	LA	0Fh	; (3Fh = 64–1)	
	T2AB		; 64/3.64 MHz = 17.58	μs
	LA	01h	; H • 32 count	
	TBA		; (1Fh = 32–1)	
	LA	0Fh	; 32/3.64 MHz = 8.79 μs	
	T2HAB			
	LA	1010b	; Timer 2 • CNTR outp	ut: vaild•"H" interval expansion: invalid
	TW2A		; Timer 2: operating • 0	Count source: XIN
			; PWM signal cycle	17.58 μs + 8.79 μs = 26.37 μs ∴37.92 kHz
			; Xin/96	Duty1/3

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	LA	05h	; Set the counter value for the no output interval 2.2 ms (4T)
	TBA		; of the next PWM signal is set to reload register R1.
	LA	03h	; As T is carrier wave 21 counts,
	TR1AB		; 21 X 4 = 84 = 54h = 53h + 1
WAIT_NH:	SNZT1		; Wait the output interval 4.4 ms of the PWM signal
	BL	WAIT_NH	
		Ç	; Wait more than one cycle of the PWM signal
	NOP	(; One cycle of PWM signal (26.37 μ s) \leq Wait time (3.30 μ s X 8 = 26.40 μ s)
	NOP		
	NOP		
	LA	01h	; Set the counter value for the output interval 0.55 ms (T)
	ТВА		; of the next PWM signal to reload register R1.
	LA	04h)	; As T is carrier wave 21 counts,
	TR1AB		; 21 = 15h = 14h + 1
WAIT_L:	SNZT1		; Wait the end of the no output interval 2.2 ms of the PWM signal
	BL	WAIT_L	
WAIT_END:	SNZT1		; Wait the end of the output interval 0.55 ms of the PWM signal
	BL	WAIT_END	
	LA	0000b	; Stop Timer 2 (PWM signal generating side)
	TW2A		
	NOP)	
	NOP	($_{ m >}$; Wait more than one cycle of the PWM signal
	NOP	(; One cycle of PWM signal (26.37 μ s) \leq Wait time (3.30 μ s X 8 = 26.40 μ s)
	NOP		
	LA	0000b J	; In order that the CNTR output auto-control circuit is unselected state,
	TW4A		; set 0 to bit 1 of register W4
	LA	0000b	; Stop Timer 1 (CNTR output control side)
	TW1A		

Figure 7 Sample Programming Code (2)

4552 Group Timer 1, Timer 2 (PWM Signal Output Control: Remote-Control Carrier Wave Output Control)

5.Note on Control of PWM Signal Output

- The port C "H" output function is valid even when CNTR (output) pin is valid. Clear "0" to the output latch of port C with the RCP instruction before the PWM signal is output.
- When the CNTR output auto-control by timer 1 is performed, set the frequency division to Timer 1 at the first time.
 Set (frequency division 1) to the reload register R1 after second times.
 Also, the PWM signal is started at output, and it becomes the no-output state by the first Timer 1 underflow.
- Even when the CNTR pin output is set to be invalid by the CNTR pin output signal selection bit W23, the generation of the PWM signal is not stopped internally by timer 2 until the end of the one cycle of the PWM signa
- When writing data to the reload register R1 with the TR1AB instruction while Timer 1 is operating, avoid a timing when Timer 1 underflows.

In particular, wait one cycle or more of the timer 1 count source after underflow, and then,

set a value to the reload register R1.

Note is especially required when the cycle of the count source is longer than the machine cycle.



6. Reference

Data Sheet 4552 Group Data sheet

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