To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

4509 Group

Timer

1. Abstruct

The following article provides seting exaples and aplication examples of timer of 4509 Group.

2. Introduction

The explanation of this issue is applied to the following condition:

- Microcomputer: 4509 Group
- Ocsillation Frequency: 4 MHz
- System Clock: Through Mode (Frequency Not Divided)

Due to the bit location for the control register, a bit with no function may be operated in some cases. Values can be optionally set on those bits.

In this issue, application examples and setting examples of the followings are provided.

- CNTR0 Output: Buzzer Output
- CNTR0 Input: Event Count
- Timer: Timer Start by External Input
- CNTR1 Output: PWM Output Control
- Input Period Count by INT
- CNTR1 Output Auto-Contorl
- Watchdog Timer

3. Relevant Register

3.1 Interrupt Control Register V1

Table 3.1 shows the bit configuration for Interrupt control register V1.
Writing to register V1 can be performed by TV1A instruction after setting register A.
The contents of register V1 can be transfered to register A by TAV1 instruction.

Table 3.1 Bit Configuration for Interrupt Control Register V1

Interrupt control register V1		at reset: 0000_2	at RAM back-up: 0000_2	R/W TAV1/TV1A
$V1_3$	Timer 2 interrupt enable bit	0	Interrupt disabled (SNZT2 instruction is valid)	
		1	Interrupt enabled (SNZT2 instruction is invalid)	
$V1_2$	Timer 1 interrupt enable bit	0	Interrupt disabled (SNZT1 instruction is valid)	
		1	Interrupt enabled (SNZT1 instruction invalid)	
$V1_1$	Not used	0	This bit has no function but read /write is enabled	
		1		
$V1_0$	External 0 interrupt enable bit	0	Interrupt disabled (SNZ0 instruction valid)	
		1	Interrupt enabled (SNZ0 instruciton invalid)	

Note 1: "R" represents read enabled, and "W" represents write enabled.
Note 2: Unused bits while setting Timer

3.2 Interrupt Control Register I1

Table 3.2 shows the bit configuration for Interrupt control register I1.
Writing to register I1 can be performed by TI1A instruction after setting values to register A.
The contents of register I1 can be transfered to register A by TAI1 instruction.

Table 3.2 Bit Configuration for Interrupt Control Register I1

Interrupt control register I1		at reset: 0000_2	at RAM back-up: state retained	R/W TAI1/TI1A
$I1_3$	INT input control bit (Note 2)	0	INT pin input disabled	
		1	INT pin input enabled	
$I1_2$	Interrupt valid waveform for INT pin/ return level selection (Note 2)	0	Falling waveform ("L" level of INT pin is recognized with the SNZI0 instruction)/"L" level	
		1	Fising waveform ("H" level of INT pin is recognized with the SNZI0 instruction)/"H" level	
$I1_1$	INT pin edge detection circuit contril bit	0	One-sided edge detected	
		1	Both edges detected	
$I1_0$	INT pin timer 1 control enable bit	0	Disabled	
		1	Enabled	

Note 1: "R" represents read enabled and "W" represents write enabled.
Note 2: "1" may occasionally set to External interrupt request flag (EXF0) when the contents of $I1_2$ and $I1_3$ are changed.
Note 3: : Unused bits while setting Timer

3.3 Timer Control Register PA

Table 3.3 shows the bit configuration for Timer control register PA.

Writing to register PA can be performed by TPAA instruction after setting values to register A.

Table 3.3 Bit Configuration for Timer Contorl Register PA

Timer control regiser PA		at reset: 0_2		at RAMback-up: 0_2	W TPAA
PA_0	Prescaler control bit	0	Stop (state initialized)		
		1	Operate		

Note 1: "W" represents write enabled.

3.4 Timer Control Register W1

Table 3.4 shows the bit configuration for Timer control register W1.

Writing to register W1 can be perfromed by TW1A instruction after setting values to register A.

The contents of register W1 can be transfered to register A by TAW1 instruction.

Table 3.4 Bit Configuration for Timer Control Register W1

Timer control register W1		at reset: 0000_2		at RAM back-up: 0000_2	R/W TAW1/TW1A
$W1_3$	PWM1 function control bit	0	PWM1 function invalid		
		1	PWM1 function valid		
$W1_2$	Timer 1 control bit	0	Stop (state retained)		
		1	Operating		
$W1_1$	Timer 1 count source selection bit	$W1_1$	$W1_0$	Count source	
		0	0	PWM2 Signal	
		0	1	Prescaler output (ORCLK)	
$W1_0$		1	0	CNTR1 input	
		1	1	On-chip ocsillator clock (f(RING))	

Note 1: "R" represents read enabled, and "W" represents write enabled.

3.5 Timer Control Register W2

Table 3.5 shows the bit configuration for Timer control register W2.

Writing to register W2 can be accomplished by TW2A instruction after setting values to register A.

The contents of register W2 can be transfered to register A by TAW2 instruciton.

Table 3.5 Bit Configuration for Timer Control Register W2

Timer control register W2		at reset: 0000_2		at RAM back-up: 0000_2	R/W TAW2/TW2A
$W2_3$	PWM2 function control bit	0	PWM2 function invalid		
		1	PWM2 function valid		
$W2_2$	Timer 2 control bit	0	Stop (state retained)		
		1	Operate		
$W2_1$	Timer 2 count source selection bit	$W2_1$	$W2_0$	Count source	
		0	0	Timer 1 underflow signal (T1UDF)	
		0	1	Prescaler output (ORCLK)	
$W2_0$		1	0	CNTR0 input	
		1	1	System clock (STCK)	

Note 1: “R” represents read enabled, and “W” represents write enabled.

3.6 Timer Control Register W5

Table 3.6 shows the bit configuration for Timer control register W5.

Writing to register W5 can be achieved by TW5A instruction after setting values to register A.

The contents of register W5 can be transfered to register A by TAW5 instruction.

Table 3.6 Bit Configuration for Timer Control Register W5

Timer control register W5		at reset: 0000_2	at RAM back-up: state retained	R/W TAW5/TW5A
$W5_3$	$P1_2$/CNTR0 pin function selection bit	0	$P1_2$ (I/O) / CNTR0 (input)	
		1	$P1_2$ (input) / CNTR0 (I/O)	
$W5_2$	Timer 1 count auto-stop circuit selection bit (Note 2)	0	Count auto-stop circuit not selected	
		1	Count auto-stop circuit selected	
$W5_1$	Timer 1 count start synchronous circuit selection bit (Note 3)	0	Count start synchronous circuit not selected	
		1	Count start synchronous circuit selected	
$W5_0$	CNTR0 input count edge selection bit	0	Falling edge	
		1	Rising edge	

Note 1: “R” represents read enabled, and “W” represents write enabled.

Note 2: Vaild only when the INT pin/timer 1 control is enabled ($I1_0$ = “1”) and the timer 1 count start synchronous circuit is selected ($W5_1$ = “1”).

Note 3: Valid only when the INT pin/timer 1 control is enabled ($I1_0$ = “1”)

3.7 Timer Control Register W6

Table 3.7 provides the bit configuration for Timer control register W6.

Writing to register W6 can be achieved by TW6A instruction after setting register A.

The content of register W6 can be transfered to register A by TAW6 instruction.

Table 3.7 Bit Configuration for Timer Control Register W6

Timer Control Register W6		Reset: 0000_2		RAM Backup: Hold	R/W TAW6/TW6A
$W6_3$	$P1_1$/CNTR1 pin function selection bit	0	$P1_1$ (I/O) / CNTR (input)		
		1	$P1_1$ (input) / CNTR1(I/O)		
$W6_2$	CNTR1pin output auto-control circuit selection bit	0	Output auto-control circuit not selected		
		1	Output auto-control circuit selected		
$W6_1$	Timer 2 INT pin input cycle count circuit selection bit	0	INT pin input period count circuit not selected		
		1	INT pin input period count circuit selected		
$W6_0$	CNTR1 pin input count edge select bit	0	Falling edge		
		1	Rising edge		

Note 1: "R" represents read enabled, and "W" represents write enabled.

4. Application Example of Timer

4.1 CNTR0 Output Operation: Buzzer Output

Overview: Rectangular wave from timer 1 can be applied to buzzer output performance.

Specification: Rectangular wave of 4 kHz will be output from CNTR0 when the frequency of system clock is 4 MHz. Further, timer 1 interrupt occurs simultaneously.

Figure 4.1 depicts the peripheral circuit while Figure 4.4 explains the setting procedure of CNTR0 output.

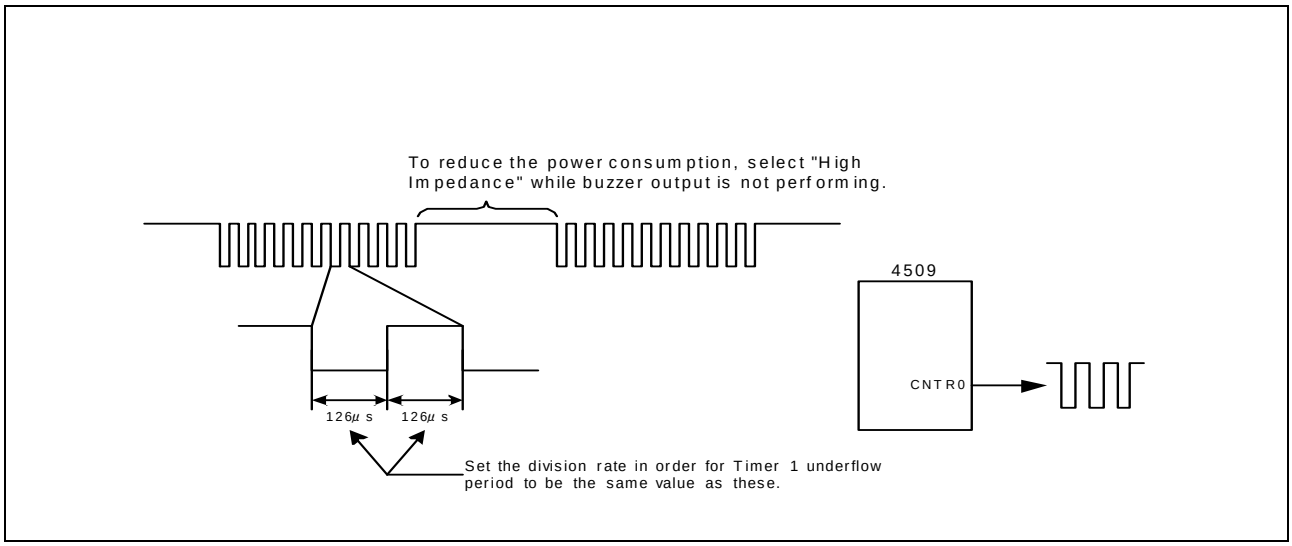


Figure 4.1 Peripheral Circuit

4.2 CNTR0 Input Operation: Event Count

Overview: Counts the input signal (rising wave) from CNTR0 as an event.

Specification: As the count source for timer 2, counts the external low frequency palse input into CNTR0; performs timer 2 interrupt when one hundred times of input events occur.

Figure 4.5 shows the setting procedure for CNTR0 input.

4.3 Timer Operation: Timer Start by External Input

Overview: With external input, a certain period of time is measured.

Specification: Activates timer 1 with INT input as a trigger thereby an interrupt occurs 1 ms after the timer 1 activation.

Figure 4.6 explains the setting procedure for timer 1 activation by external input.

4.4 CNTR1 Output Control: PWMOutput Control

Overview: PWM output is performed from port CNTR1 by timer 2.

Specification: System clock frequency of 4.0 MHz is divided by timer 2; thereby outputs PWM waveform with an interval of 1.75 μs (0.75 μs during the "H" period) from port CNTR1.

Figure 4.2 shows Timer 2 operation, Figure 4.7 explains the setting procedure for PWM output control.

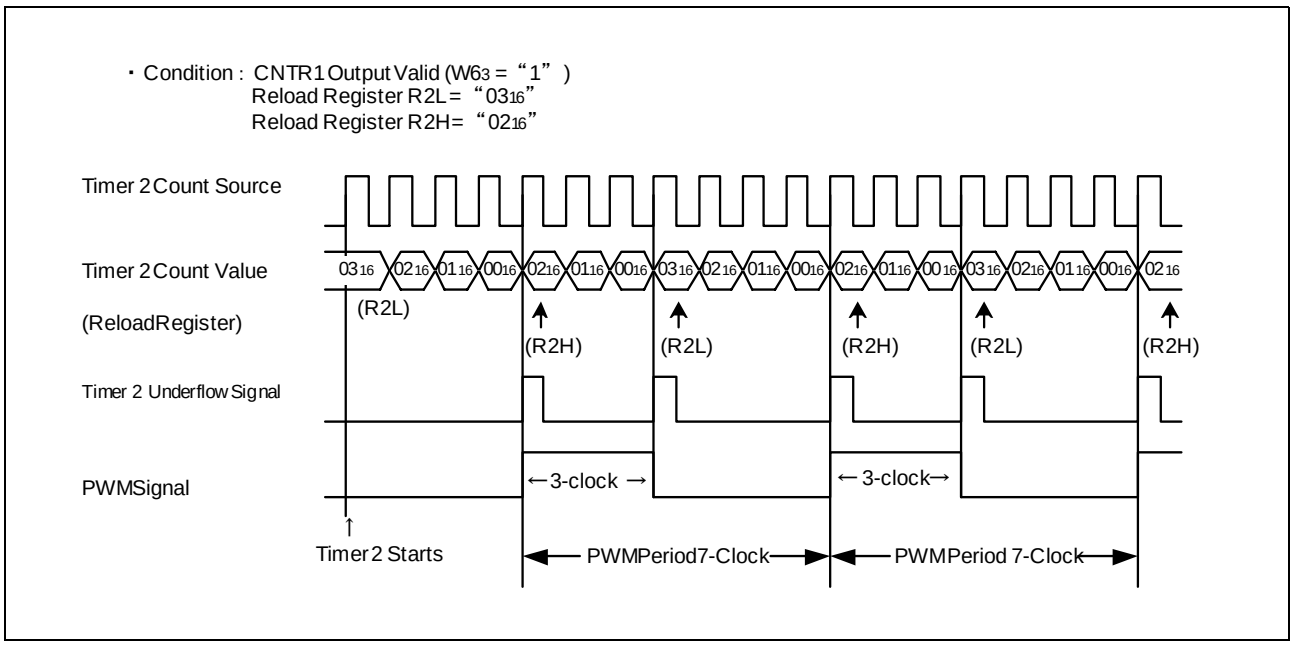


Figure 4.2 Timer 2 Operation

4.5 INT Input Period Count

Overview: The period of INT input can be counted by timer 2.

Specification: The period from the rising edge to the next rising edge is defined as one cycle.
The counting performance is carried out by timer 2.
The count source for timer 2 is the system clock.

Figure 4.8 and Figure 4.9 explains the setting procedures for the INT input period count performance.

4.6 CNTR1 Output Auto Control

Overview: PWM2 signals are genereted by timer 2; CNTR1 output is automatically controlled by timer 1.

Specification: The setting periods to reload registers R2L and R2H are defined as "L" and "H" respectively. PWM signals of "L" and "H" are generated. The PWM signal generation is executed by reloading data from R2L and R2H alternately everytime timer 2 performs underflow. During this period, if "1" is set to bit 2 of register W6; the performance of PWM2 singal output to port CNTR1 turns to be enable and disable alternately everytime timer 1 underflow occurs.

Figure 4.10 illustrates the setting procedure for CNTR1 output auto-contorl.

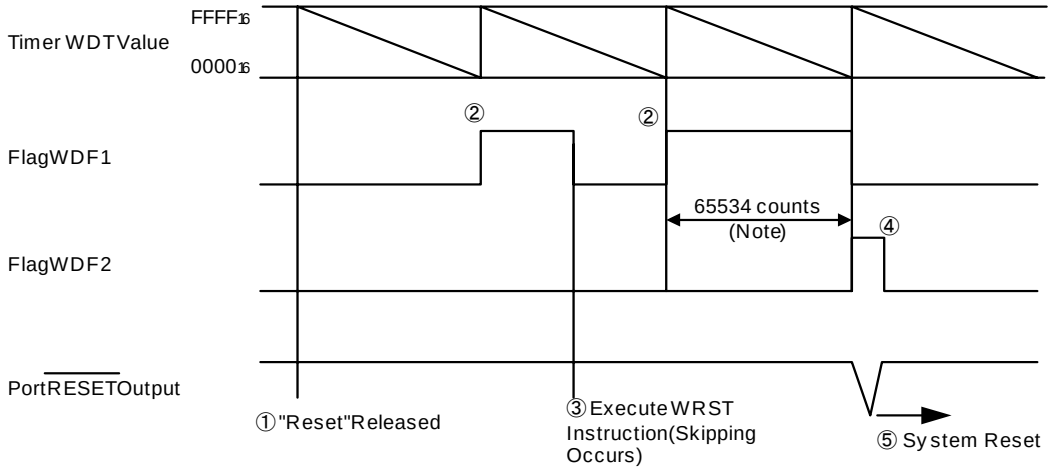
4.7 Watchdog Timer

Watchdog timer enables to reset the settings, if the program goes out of control or some fault condition occurs. WRST instruction must be executed with an interval of less than 65534 of 16-bit timer, (i.e., less than 65534 of machine cycle), when the watchdog timer is enabled.

Overview: WRST needs to be executed within 65534 counts of the 16-bit timer while the microcomputer is operating normally. Resetting will be executed if something goes out of control and WRST instruction cannot be performed.

Specification: Using 4.0 MHz of system clock frequency, detects an inappropiate operation within 49 ms by executing WRST instruction.

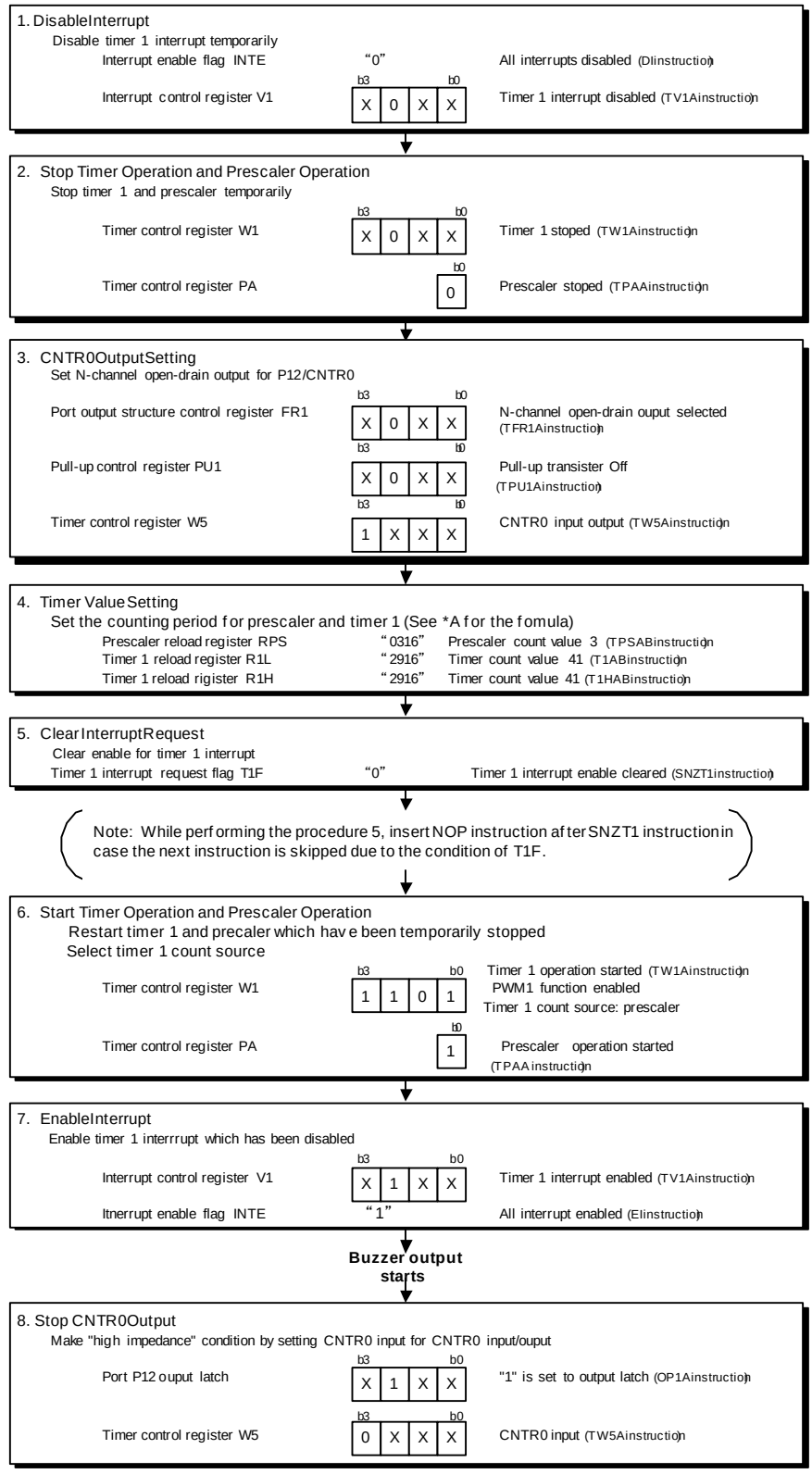
Figure 4.3 shows Watchdog timer function, while Figure 4.11 provides a usage example of Watchdog timer.



①Timer WDT starts down counting once "Reset" is released (=the program starts).
②"1" is set to flag WDF1 when timer WDT underflow occurs.
③Flag WDF1 turns back to "0" and the next instruction is skipped when WRST instruction is performed.
④"1" is set to flag WDF2 and the watchdog reset signal is output, if timer WDT underflow occurs while flag WDF1 is "1".
⑤By the watchdog reset signal, the output transistor of port $\overline{\text{RESET}}$ becomes "ON" thereby system reset is performed.

Note: The count source for timer WDT is the instruction clock; thus the count is same as the machine-cycle.

Figure 4.3 Watchdog Timer Function



*A: Set the count values for timer 1 and prescaler of the rectangular wave output which is reversed every 126 μs, using the following formula.

$$126\ \mu s \fallingdotseq \frac{(4.0\ MHz)}{\text{System Clock}} - 1 \quad \times \underbrace{3}_{\text{Instruction Clock}} \quad \times \underbrace{(3+1)}_{\text{Prescaler Count Value}} \quad \times \underbrace{(41+1)}_{\text{Timer 1 Count Value}}$$

"X": Set either "0" or "1".

Figure 4.4 CNTR0 Output Setting Procedure

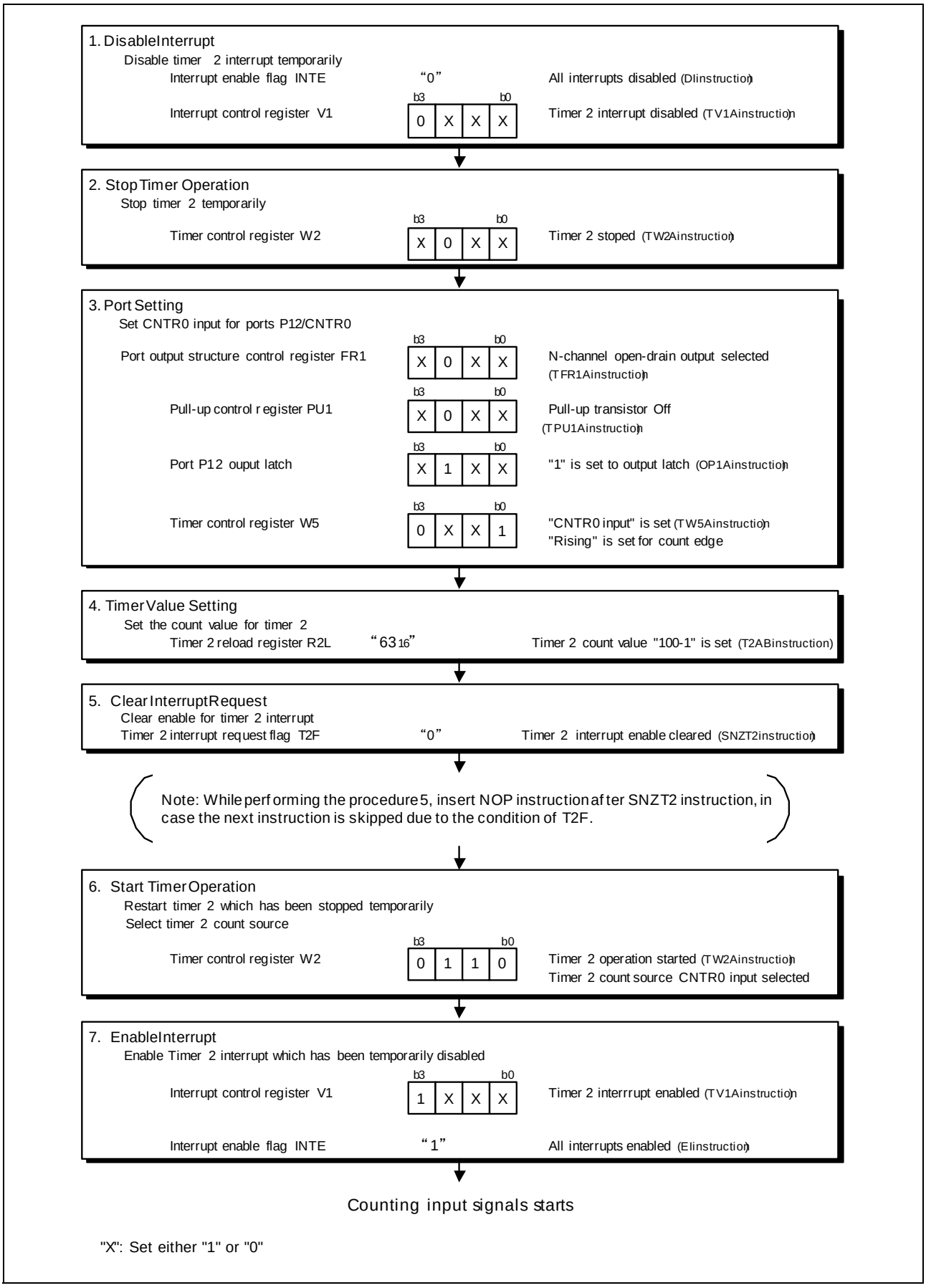


Figure 4.5 CNTR0 Input Setting Procedure

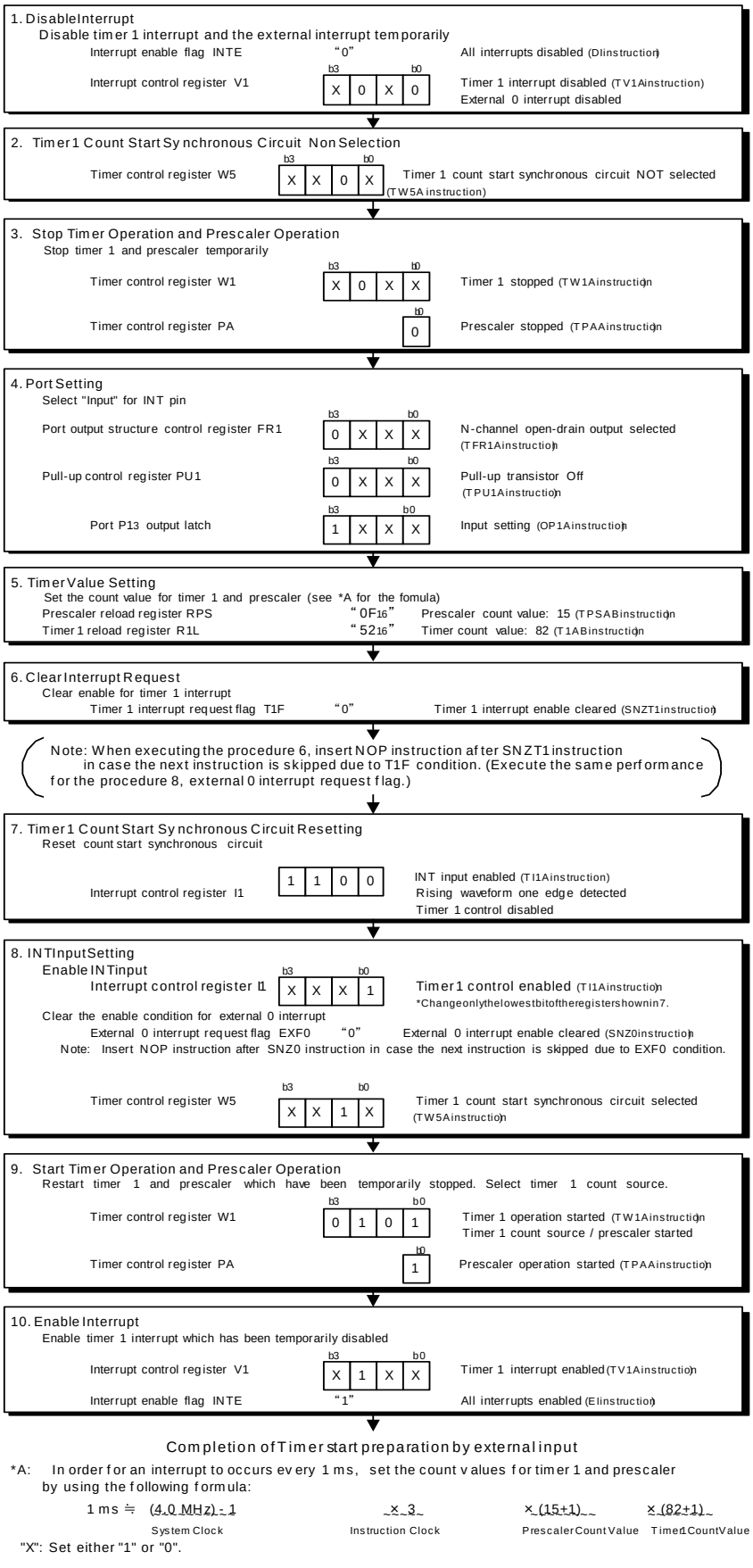


Figure 4.6 Setting Procedure for Timer 1 Start By External Input

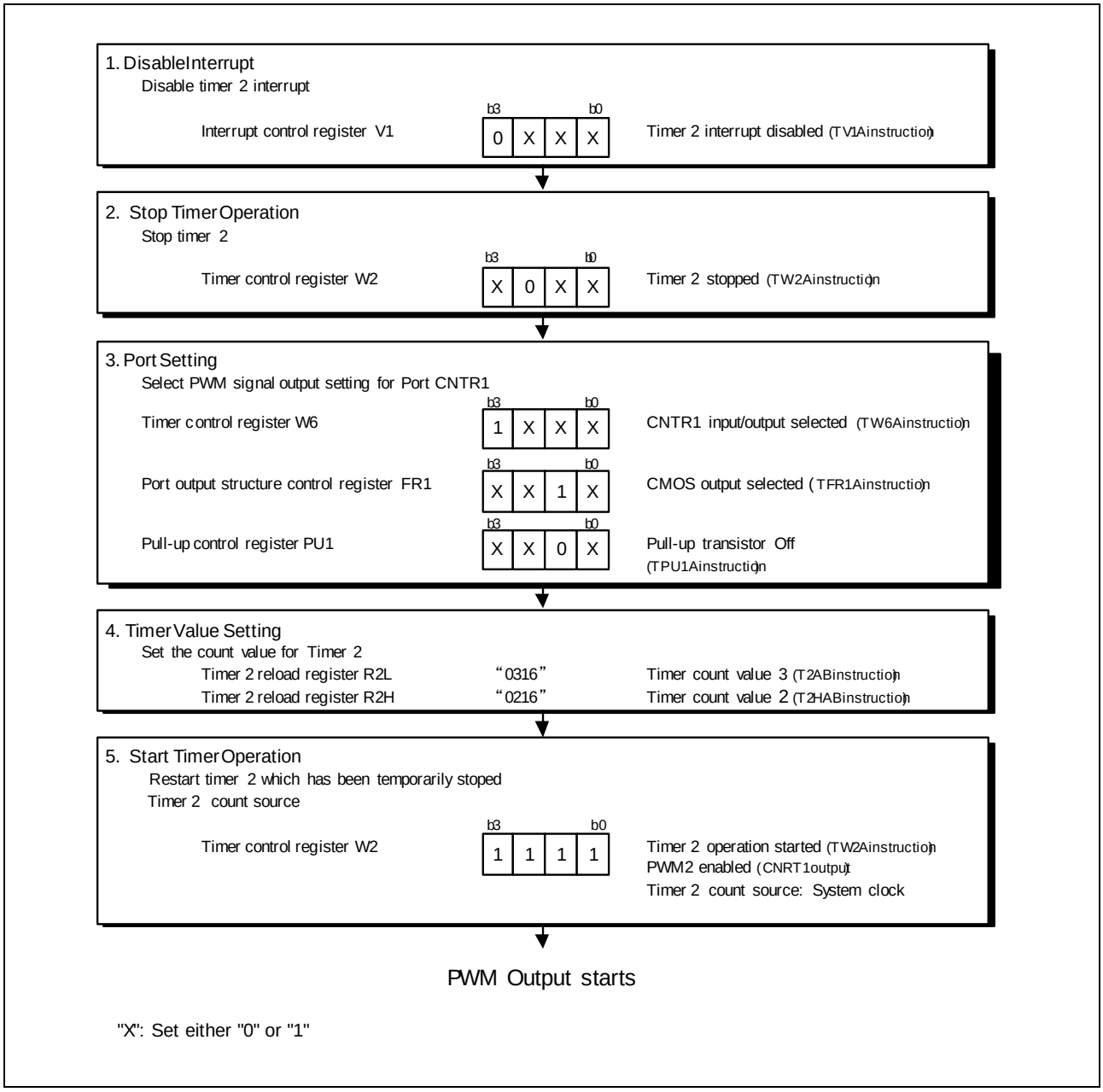


Figure 4.7 Setting Procedure for PWM Output Control

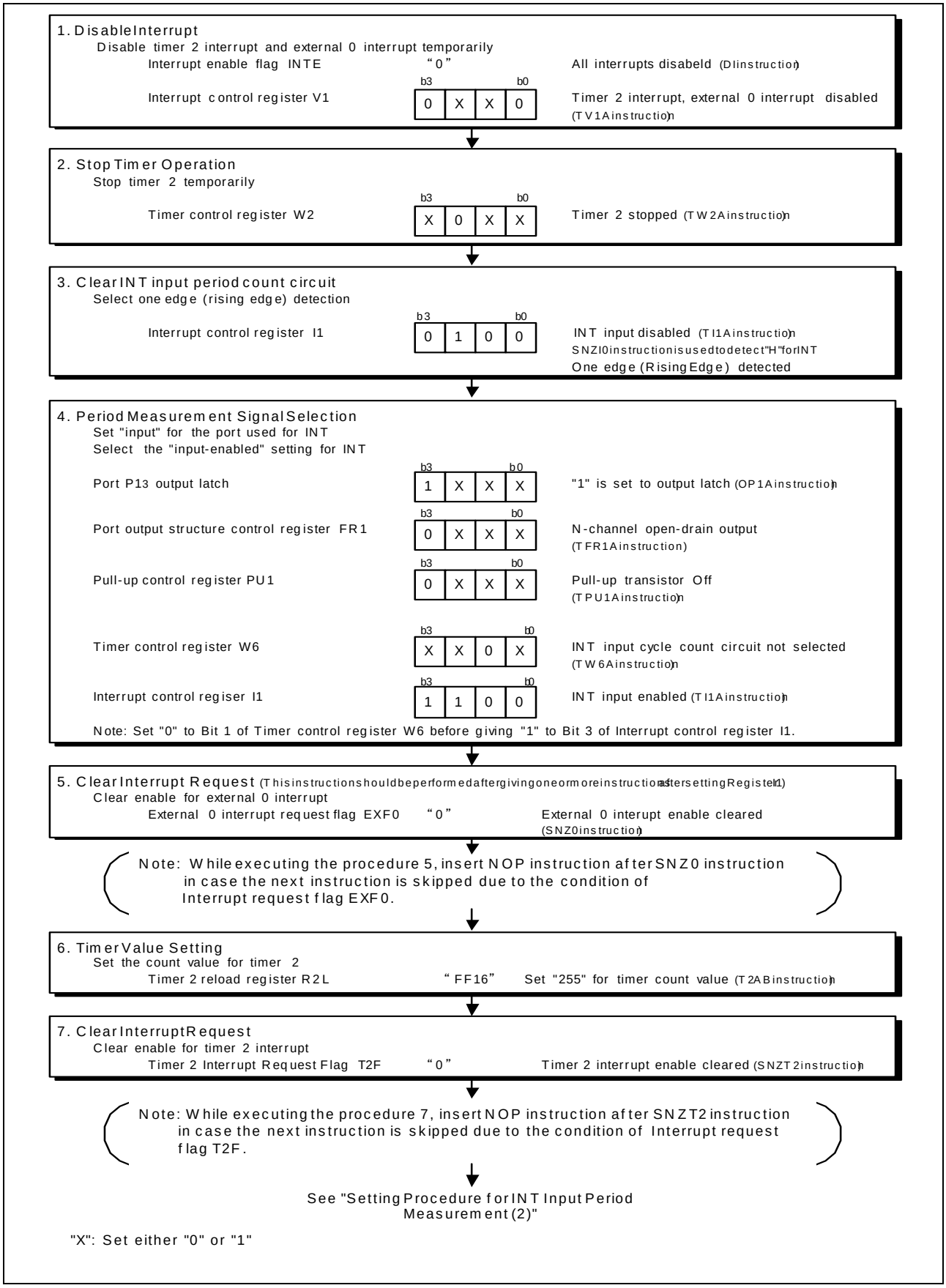


Figure 4.8 Setting Procedure for INT Input Period Measurement (1)

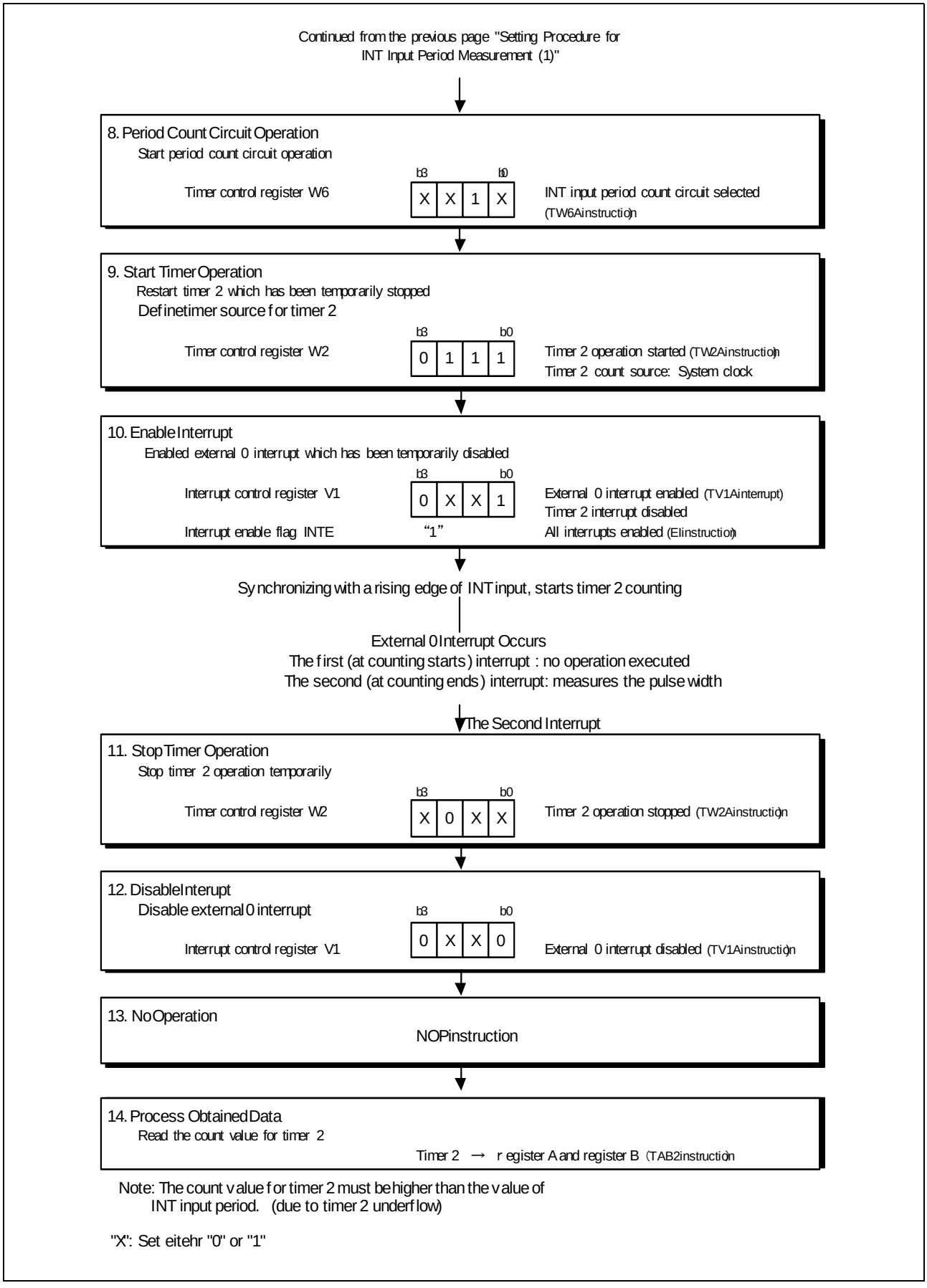


Figure 4.9 Setting Procedure for INT Input Period Measurement (2)

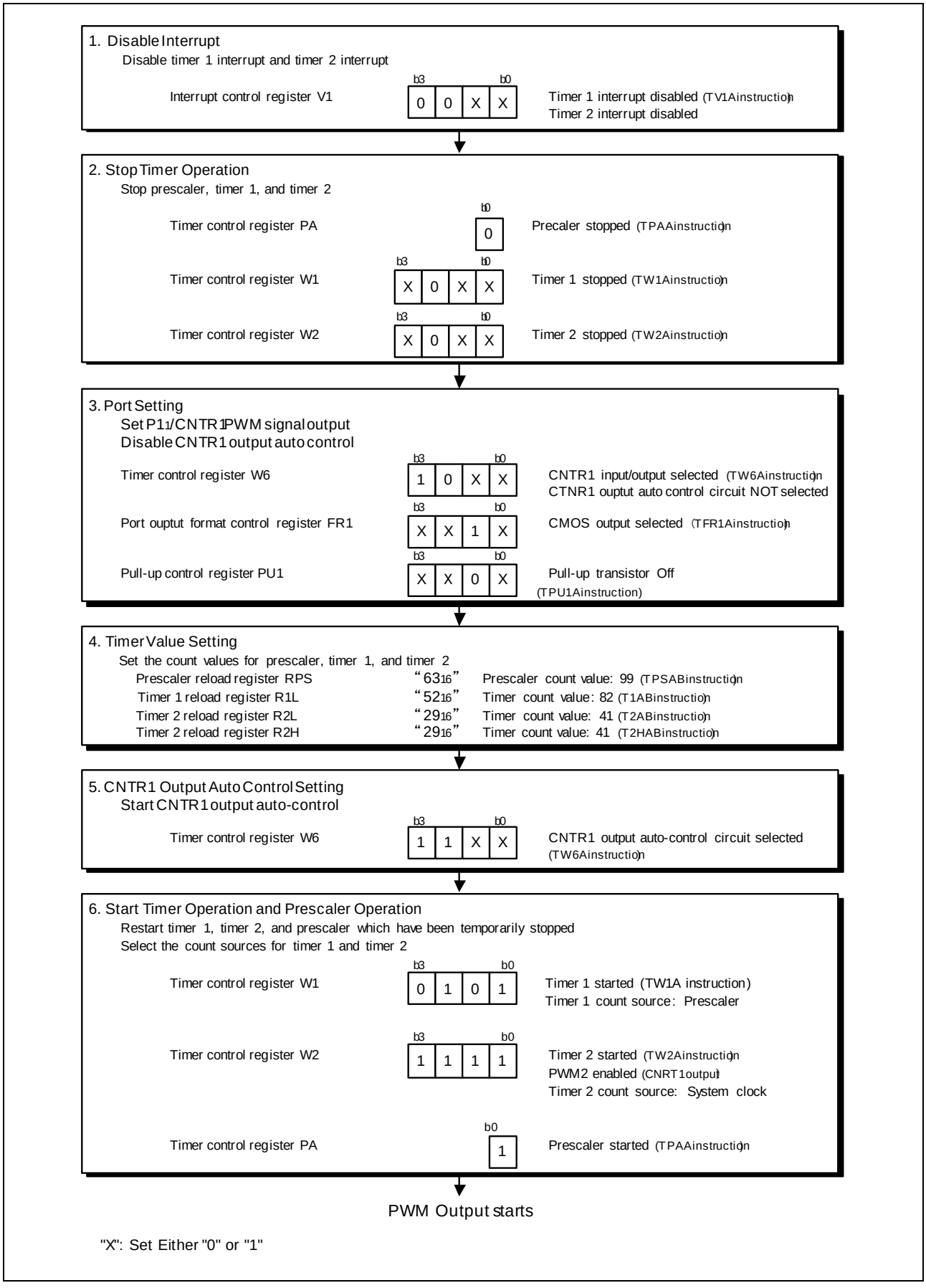


Figure 4.10 Setting Procedure for CNTR1 Output Auto-Control

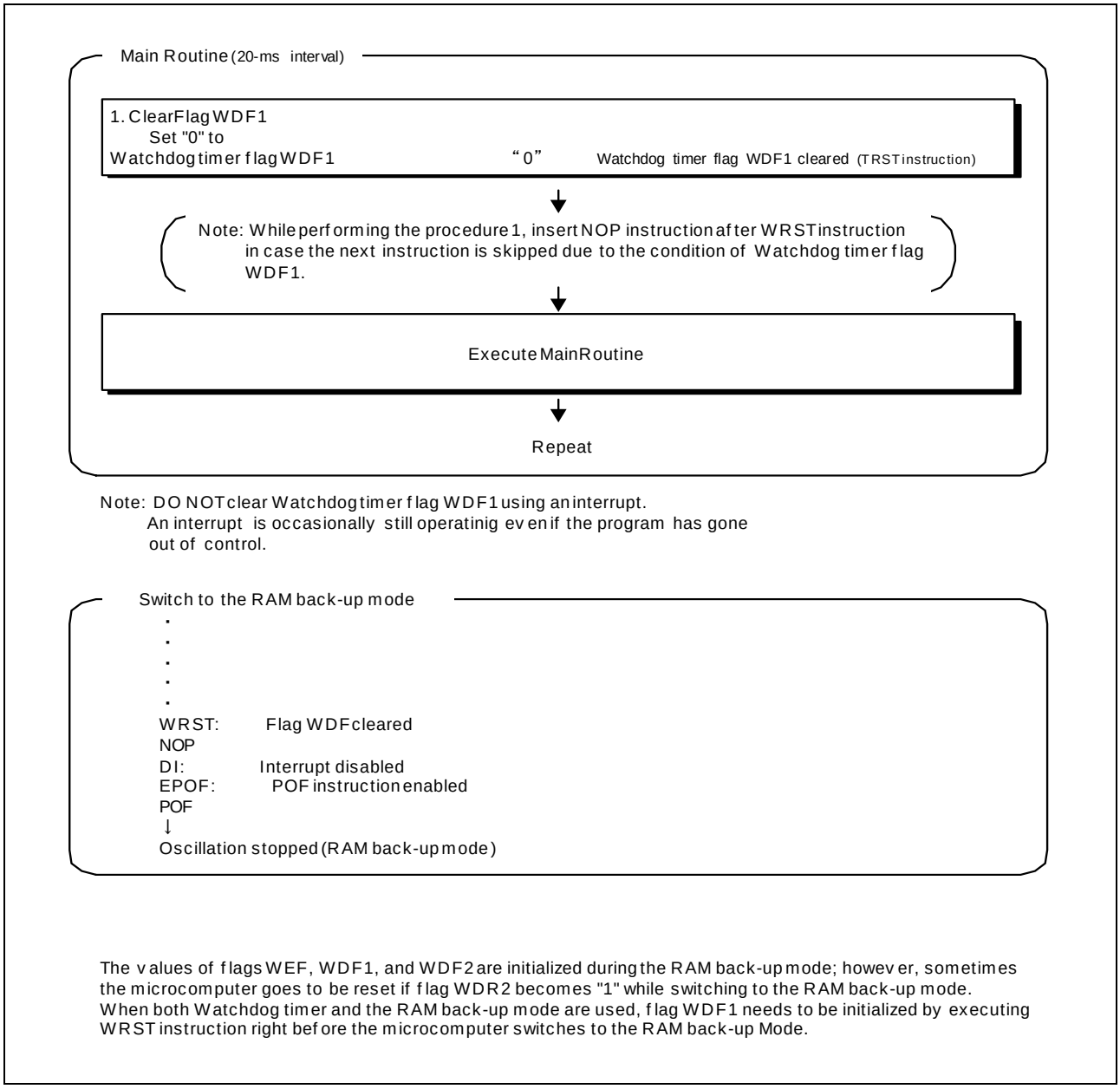


Figure 4.11 Usage Example for Watchdog Timer

5. Reference Software Programs

Reference software programs are available on Renesas Corporation Website.
To obtain the programs, click “Application Note” on the left side of the 4509 Group page.

6. Reference Documents

Datasheet
4509 Group Datasheet

Before using this material, pelase visit our website to verify that this is the most updated docmuent available.

7. Our Official Website and Inquiry Contact

Renesas Technology Corporation Website
http://www.renesas.com

Inquiry Contact
http://www.renesas.com/inquiry
csc@renesas.com

Revision History	4509 GroupTimer Application Note

Rev.	Date	Description	
		Page	Summary
1.00	July 01, 2006	—	First Edition Issued

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.