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# 4509 Group

## Serial Interface

#### 1. Abstruct

The following article introduces application examples and setting examples of the serial interface of 4509 Group.

#### 2. Introduction

The explanation of t his issue is applied to the following condition:

• Microcomputer:	4509 Group
Ocsillation Frequecy:	4 MHz
System Clock:	Through Mode (Frequency not divided)

Due to the bit location for the control register, a bit with no funciton may be operated in some cases. Values can be optionally set on those bits.



#### 3. Relevant Register

#### 3.1 Serial Itnerface Register SI

Register SI is the 8-bit data transfering serial-pararel conversion Register.

Writing to register SI can be accomplished by TSIAB instruction after setting values to the lower four bits of register A and the upper 4 bits of register B.

The contents of the lower four bits of register SI can be transferred to register A by TABSI instruction. Similarly, the contents of the upper four bits of register SI can be transferred to register B by TABSI instruction.

### 3.2 Serial Interface Transmit/Receive Completion Flag SIOF

Once the serial data transmission/reception is completed, flag SIOF turns to "1".

The condition of flag SIOF can be confirmed by SNZSI instruction when Serial interface interrupt enable bit is set to the disable mode.

### 3.3 Interrupt Control Register V2

Table 3.1 shows the bit configuration for Interrupt control register V2. Writing to register V2 can be performed by TV2A instruction after setting values to register A. The contents of register V2 can be transfered to register A by TAV2 instruction.

#### Table 3.1 Bit Configuration for Interrupt Control Register V2

	Interrupt control register V2		at reset: 00002	at RAM back-up: 00002	R/W TAV2/TV2A	
1/20	V23 Serial interface interrupt enable bit		Interrupt disabled (SNZSI instruction is valid)			
V 23			Interrupt enabled (SNZSI instruction is invalid)			
1/20	V22 A/D interrupt enable bit	0	Interrupt disabled (	SNZAD instruction is valid)		
V Z Z		1	Interrupt enablede	(SNZAD instruction is invalid)		
V21	V21 Not used		This bit has no function but read/write is enabled			
VZI	V21 Not used	1		alon but read/write is enabled		
V20	V20 Not used	0	This bit has no function but read/write is enabled			
V 20						

Note 1: "R" represents read enabled, and "W" represents write enabled.

Note 2: Unsed bits while setting the serial interface.



## 3.4 Serial Itnerface Control Register J1

Table 3.2 shows the bit configuration for Serial interface control register J1. Writing to register J1 can be achieved by TJ1A instruction after setting values to register A. The content of register J1 can be transferred to register A by TAJ1 instruction.

Table 3.2 Bit Configuration for	r Serial Interface	Contorl Register J1.
---------------------------------	--------------------	----------------------

	Serial interface contorl register J1	at reset: 00		0002	at RAM back-up: Hold	R/W TAJ1/TJ1A	
			J12	Synchronous Clock			
J13	J13 Serial interface synchronous clock selection bits J12	0	0	Instruct	Instruction clock (INSTCK) divided by 8		
		0	1	Instuction	Instuction clock (INSTCK) divided by 4		
11.0		1	0	Instuction	Instuction clock (INSTCK) divided by 2		
<b>J</b> 12		1	1	External clock (Sck input)			
	J11 Serial interface port function selection bits J10	<b>J1</b> 1	<b>J1</b> 0	Port Function			
<b>J1</b> 1		0	0	P00, P01, P02 selected / SIN, SOUT, SCK not selected		ected	
		0	1	P00, SOUT, SCK selected / SIN, P01, P02 not selected			
110		1	0	SIN, P01, SCK selected / P00, SOUT, P02 not selected		ected	
<b>J</b> 10		1	1	SIN, SO	лт, Scк selected / P00, P01, P02 not sele	ected	

Note1: "R" represents read enabled, and "W" represents write enabled.



#### 4. Operation Procedure

Figure 4.1 depicts an example of the serial interface connection, whereas Figure 4.2 illustrates the transfering timing of the serial interface. For actual cabling, pull up each signal line via a resistor.



Figure 4.1 Serial Interface Connnection Example



Figure 4.2 Serial Interface Transfer Timing

#### 5. Application Example for Serial Interface

#### 5.1 Serial Itnerface

Overview:Communicates with the peripheral ICSpecification:See Figure 4.1 Serial Interface Commection Example.

Figure 5.2 explains the setting procedure when using NO Serial Interface Interrupt for Master while Figure 5.2 shows the setting procedure using Serial Interface Interrupt for Slave.



Interrupt control register V2	$\begin{bmatrix} b3 \\ 0 \\ X \\ X \\ X \end{bmatrix}$	Serial interface interrupt disabled
		(T V2A instruction)
2. PortSetting	•	
Select the input setting for the port us	ed for control signal	
Register Y	0 0 1 1	Port D bit location specified (TYAinstruction
Port D3 output latch	"1" _b3b0	"1" is set to output latch (SDinstruction)
Port output structure control register FR3		N-channel open-drain output selected (TFR3Ainstructio))
Pull-up contorl register PU2	b3 b0 0 X X X	Pull-up transistor Off (TPU2Ainstruction)
2 Coloct the Input Sotting for the Dort for S		
<ol> <li>Select the Input Setting for the Port for S Port P02, 1,0 output latch</li> </ol>	<u>b3</u> <u>b0</u>	"1" is set to output latch (OP0Ainstruction)
	X 1 1 1 b3 b0	
Port output structure control register FR0	X 0 0 0	N-channel open-drain output selected (TFR0Ainstructio)
Pull-up contorl register PU0	X 0 0 0	Pull-up transistor Off (TPU0Ainstruction)
	+	
4. SerialInterfaceSetting	<u>b3</u> b0	Serial interface ports SCK, SOUT, SIN selected
Serial interface control register J1	0 1 1 1	(TJ1Ainstructio) 1/4 division signal of the instruction clock for synchronous clock
	*	
5. Clear Interrupt R equest Clear serial interface interrupt enable condition Serial interface interrupt request flag		nterface interrupt enable cleared
Note: W hile performing 5, insert N instruction is skipped due to the c	♦ NOP instruction after condition of Interrupt	SNZSI instruction in case the next request flagSIOF.
6. Transmission Data Setting Set transmission data to serial interface re	egister	
serial interface register SI	" XX 16" (T S IA	Binstruction
7. DetectEnable Condition to Start SerialIn Confirm if the slave side is ready to transm		rol signal="L")
Register Y		Bit location of port D specified (TYAinstruction)
Port D3 Output latch Port D3 intput level confirmation	"1"	"1" is set to output latch (SDinstruction) (SZDinstruction)
	*	
8. Start Serial Interface Operation Start serial transfering if the slave side is r	eady to transmit/receive	(SSTinstructio)
9. ConfirmSerialInterfaceInterruptReques Serial Interface transmit/receive completion		ZSlinstruction
·	<b>★</b>	
10. Process ReceivedData Process the data received by serial transfer		er A/register B (TABSlinstructio)n
R	egister or / iveuist	

Figure 5.2 Setting Procedure with NO Serial Interface Interrupt on Master



1. DisableInterrupt			
Disable serial interface interrupt temporarily Interrupt enable flag INTE	"О" b3 b0	All interrupts disabled (Dlinstruction)	
Interrupt control register V2	0 X X X	Serial interface interrupt disabled (TV2Ainstruction	
	★		
2. PortSetting Set "H" output to the ports used for cont	rolsignalperforma	nce	
Register Y	0 0 1 1	Port D bit location specified (TYAinstruction	
Port D3 output latch	"1" _b3b0	"1" is set to output latch (SDinstruction)	
Port output structure control register FR3	0 X X X b3 b0	N-channel open-drain output (TFR3Ainstructio)	
Pull-up control register PU2	0 X X X	Pull-up tansistor Off (TPU2Ainstruction	
3. Set "Intput" to the Port Used for Serial Inter			
Port P02, 1, 0 output latch	b3         b0           X         1         1         1	"1" is set to output latch (OP0Ainstructio)	
Port output structure control register FR0	b3 b0 X 0 0 0	N-channel open-drain output (TFR0Ainstructio)	
Pull-up control register PU0	b3 b0 X 0 0 0	Pull-up transistor Off (TPU0AInstruction)	
· · · · · · · · · · · · · · · · · · ·			
4. SerialInterfaceSetting	b3 h0		
Serial interface control register J1		External clock selected (TJ1Ainstruction Serial interface port SCK, SOUT, SIN selected	
·	*		
5. ClearInterrupt R equest Clear the enable condition for Serial inte Serial interface interrupt request flag SIOF	"0" Serial i	nterface interrrupt enable cleared nstruction	
·	+		
W hile performing5, insert NOP ins instruction is skipped due to the co			
6. EnableInterrupt	•		
Enable serial interface interrupt which has bee			
Interrupt control register V2	b3 b0	Serial interface interrupt enabled	
	1 X X X	(TV2Ainstructio)n	
Interrupt control register V2 Interrupt enable flag INTE			
	1 X X X "1" ∳ gister	(TV2Ainstructio)n	
Interrupt enable flag INTE 7. Transmission DataSetting Set transmission data to Serial interface reg Serial interface register SI	1 X X X "1" ↓ gister "XX 16" (TSIA	(TV2Ainstruction All interrupts enabled (Elinstruction)	
Interrupt enable flag INTE           7. Transmission DataSetting Set transmission data to Serial interface reg	1 X X X "1" ↓ gister "XX 16" (TSIA ↓ ation	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction	
Interrupt enable flag INTE 7. Transmission DataSetting Set transmission data to Serial interface reg Serial interface register SI 8. Condition Setting for Serial Interface Activ Set the serial itnerface enable mode (start ser	1 X X X "1" ↓ gister "XX 16" (TSIA ↓ ation	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction gnal "L" output)	
Interrupt enable flag INTE 7. Transmission DataSetting Set transmission data to Serial interface register SI 8. Condition Setting for Serial Interface Activ Set the serial interface enable mode (start ser Serial transfer start	1 X X X "1" ↓ gister "XX 16" (TSIA ↓ ation ial transfer / control si	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction gnal "L" output) (SSTinstruction)	
Interrupt enable flag INTE 7. Transmission DataSetting Set transmission data to Serial interface reg Serial interface register SI 8. Condition Setting for Serial Interface Activ Set the serial itnerface enable mode (start ser Serial transfer start Register Y Port D3 output latch	$\begin{array}{c c} 1 & X & X \\ \hline 1 & X & X \\ \hline \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction gnal "L" output) (SSTinstruction) Port D bit location speficied (TYAinstruciton) "L" output (RDinstruction)	
Interrupt enable flag INTE 7. Transmission DataSetting Set transmission data to Serial interface reg Serial interface register SI 8. Condition Setting for Serial Interface Activ Set the serial itnerface enable mode (start ser Serial transfer start Register Y Port D3 output latch	$\begin{array}{c c} 1 & X & X \\ \hline 1 & X & X \\ \hline \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction gnal "L" output) (SSTinstruction) Port D bit location speficied (TYAinstruciton) "L" output (RDinstruction)	
Interrupt enable flag INTE 7. Transmission DataSetting Set transmission data to Serial interface reg Serial interface register SI 8. Condition Setting for Serial Interface Activ Set the serial itnerface enable mode (start ser Serial transfer start Register Y Port D3 output latch	$\begin{array}{c c} 1 & X & X \\ \hline 1 & X & X \\ \hline 1 & X & X \\ \hline 1 & & \\ \hline 1 & X & X \\ \hline 1 & & \\ 1 & & \\ \hline 1 & & \\ \hline 1 & & \\ \hline 1 & & \\ 1 & & \\ \hline 1 & & \\$	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction gnal "L" output) (SSTinstruction) Port D bit location speficied (TYAinstruciton) "L" output (RDinstruction) eption on Master	
Interrupt enable flag INTE 7. Transmission DataSetting Set transmission data to Serial interface register SI 8. Condition Setting for Serial Interface Activ Set the serial interface enable mode (start ser Serial transfer start Register Y Port D3 output latch 9. Process Received Data at Serial Interface	1 X X X $(TSIA)$	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction gnal "L" output) (SSTinstruction) Port D bit location speficied (TYAinstruciton) "L" output (RDinstruction) eption on Master	
Interrupt enable flag INTE         7. Transmission DataSetting Set transmission data to Serial interface reg Serial interface register SI         8. Condition Setting for Serial Interface Activ Set the serial interface enable mode (start ser Serial transfer start Register Y Port D3 output latch         9. Process Received Data at Serial Interface Set serial interface performance disable mode Register Y Port D3 output latch	$\begin{array}{c c} 1 & X & X \\ \hline 1 & X & X \\ \hline 1 & X & X \\ \hline 1 & & \\ \hline 1 & X & X \\ \hline 1 & & \\ 1 & & \\ \hline 1 & & \\ \hline 1 & & \\ \hline 1 & & \\ 1 & & \\ \hline 1 & & \\$	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction gnal "L" output) (SSTinstruction) Port D bit location speficied (TYAinstruciton) "L" output (RDinstruction) eption on Master utput) and process the received data. Port D bit location specified (TYAinstruction) "H" output (SDinstruction)	
Interrupt enable flag INTE         7. Transmission DataSetting Set transmission data to Serial interface reg Serial interface register SI         8. Condition Setting for Serial Interface Activ Set the serial interface enable mode (start ser Serial transfer start Register Y Port D3 output latch         9. Process Received Data at Serial Interface Set serial interface performance disable mode Register Y Port D3 output latch	$\begin{array}{c c} 1 & X & X \\ \hline 1 & Y \\$	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction gnal "L" output) (SSTinstruction) Port D bit location speficied (TYAinstruciton) "L" output (RDinstruction) eption on Master utput) and process the received data. Port D bit location specified (TYAinstruction) "H" output (SDinstruction)	
Interrupt enable flag INTE         7. Transmission DataSetting Set transmission data to Serial interface reg Serial interface register SI         8. Condition Setting for Serial Interface Activ Set the serial interface enable mode (start ser Serial transfer start Register Y Port D3 output latch         9. Process Received Data at Serial Interface Set serial interface performance disable mode Register Y Port D3 output latch	$1 \times X \times$ $(T \times X)$ $(T \times$	(TV2Ainstruction All interrupts enabled (Elinstruction) Binstruction gnal "L" output) (SSTinstruction) Port D bit location speficied (TYAinstruciton) "L" output (RDinstruction) eption on Master utput) and process the received data. Port D bit location specified (TYAinstruction) "H" output (SDinstruction)	

Figure 5.2 Setting Procedure with Serial Interface Interrupt on Slave



#### 6. Reference Software Programs

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Datasheet 4509 Group Datasheet

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## **Revision History**

## 4509 GroupSerial Interface Application Note

Rev.	ev. Date		Description	
itev.	Dale	Page	Summary	
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