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4509 Group

Interrupt

1. Abstract

The following article provides application examples and setting examples of interrupt of 4509 Group.

2. Introduction

The explanation of this issue is applied to the following condition:

- Microcomputer : 4509 Group
- Oscillation Frequency : 4 MHz (External 0 interrupt, Timer 1 interrupt), 2 MHz (Timer 2 interrupt)
- System Clock : Through Mode (Frequency not divided)

Due to the bit location for the control register, a bit with no function may be operated in some cases. Values can be optionally set on those bits.

In this issue, application examples and setting examples of the followings are provided.

- External 0 interrupt
- Timer 1 interrupt
- Timer 2 interrupt

3. Relevant Registers

3.1 Interrupt Control Register V1

Table 3.1 shows the bit configuration for Interrupt control register V1.
Writing to register V1 can be performed by TV1A instruction after setting values to register A.
Furtuer, contents of register V1 can be transfered by TAV1 instruction.

Table 3.1 Bit Configuration for Interrupt Control Register V1

Interrupt control register V1		reset : 0000_2	at RAM back-up: 0000_2	R/W TAV1/TV1A
$V1_3$	Timer 2 interrupt enable bit	0	Disabled (SNZT2 instruction is valid)	
		1	Enabled (SNZT2 instruction is invalid)	
$V1_2$	Timer 1 interrupt enable bit	0	Disabled (SNZT1 instruction is valid)	
		1	Enabled (SNZT1 instruction is invalid)	
$V1_1$	Not used	0	This bit has no function but read/write is enabled	
		1		
$V1_0$	External 0 interrupt enable bit	0	Disabled (SNZ0 instruction is valid)	
		1	Enabled (SNZ0 instruction is invalid)	

Note 1. “R” represents read enabled, and “W” represents write enabled.
Note 2. : Unsued bit s for interrupt setting.

3.2 Interrupt Control Register V2

Table 3.2 shows the bit configuration for Interrupt control register V2.
Writing to register V2 can be performed by TV2A instruction after setting values to register A.
Further, contents of register V2 can be transfered to register A by TAV2 instruction.

Table 3.2 Bit Configuration for Interrupt Control Register V2

Interrupt control register V2		at reset: 0000_2	at RAM back-up: 0000_2	R/W TAV2/TV2A
$V2_3$	Serial interface interrupt enable bit	0	Disabled (SNZSI instruction is valid)	
		1	Enabled (SNZSI instruction is invalid)	
$V2_2$	A/D interrupt enable bit	0	Disabled (SNZAD instruction is valid)	
		1	Enabled (SNZAD instruction is invalid)	
$V2_1$	Not used	0	This bit has no function but read/write is enabled	
		1		
$V2_0$	Not used	0	Thit bit has no function but read/write is enabled	
		1		

Note 1. “R” represents read enabled, and “W” represents write enabled.
Note 2. : Unused bit for interrupt setting

3.3 Interrupt Control Register I1

Table 3.3 shows the bit configuration for Interrupt control register I1.

Writing to register I1 can be performed by TI1A instruction after setting values to register A.

Further, contents of register I1 can be transfered to register A by TAI1 instruction.

Table 3.3 Bit Configuration for Interrupt Control Register I1

Interrupt control register I1		at reset: 0000_2		at RAMback-up: Hold	R/W TAI1/TI1A
$I1_3$	INT input control bit (Note 2)	0	INT pin input disabled		
		1	INT pin input enabled		
$I1_2$	Interrupt valid waveform for INT pin/ return level selection bit (Note 2)	0	Falling waveform ("L" level of INT pin is recognized with the SNZI0 instruction)"L" level		
		1	Rising waveform ("H" level of INT pin is recognized with the SNZI0 instruction/"H" level		
$I1_1$	INT pin edge detection circuit control bit	0	One-sided edge detected		
		1	Both edges detected		
$I1_0$	INT pin timer 1 control enable bit	0	Disabled		
		1	Enabled		

Note 1. "R" represents read enabled, and "W" represents write enabled.

Note 2. "1" is occasionally set to External interrupt request flag (EXF0) when the contents of bit $I1_2$ or bit $I1_3$ is changed.

3.4 Timer Control Register PA

Table 3.4 shows the bit configuration for Timer control register PA.

Writing to register PA is achieved by TPAA instruction after setting values to register A.

Table 3.4 Bit Configuration for Timer Control Register PA

Timer control register PA		at reset: 0_2		at RAM back-up0_2	W TPAA
PA_0	Prescaler control bit	0	Stop (State initialized)		
		1	Operating		

Note 1. "W" represents write enabled.

3.5 Timer Control Register W1

Table 3.5 describes the bit configuration for Timer control register W1.

Writing to register W1 can be performed by TW1A after setting values to regiser A.

Further, contents of register W1 can be transfered to register A by TAW1 instruction.

Table 3.5 Bit Configuration for Timer Control Register W1

Timer control register W1		at reset: 0000_2		at RAM back-up: 0000_2	R/W TAW1/TW1A
$W1_3$	PWM1 function control bit	0	PWM1function invalid		
		1	PWM1function valid		
$W1_2$	TImer 1 control bit	0	Stop (Hold)		
		1	Operate		
$W1_1$	Timer 1 count source slection bit	$W1_1$	$W1_0$	Count source	
		0	0	PWM2 signal	
		0	1	Prescaler output (ORCLK)	
$W1_0$		1	0	CNTR1 Input	
		1	1	On-chip ocsillator clock (f(RING))	

Note 1: “R” represents read enabled, and “W” represents write enabled.

3.6 Timer Control Register W2

Table 3.6 shows the bit configuration for Timer control register W2.

Writing to register W2 can be performed by TW2A instruction after setting values to register A.

Table 3.6 Bit Configuration for Timer Control Register W2.

Timer Control Register W2		at reset: 0000_2		at RAM back-up: 0000_2	R/W TAW2/TW2A
$W2_3$	PWM2 function control bit	0	PWM2 function disabled		
		1	PWM2 function enabled		
$W2_2$	Timer 2 control bit	0	Stop (state retained)		
		1	Operate		
$W2_1$	Timer 2 count source selection bit	$W2_1$	$W2_0$	Count source	
		0	0	Timer 1 underflow signal (T1UDF)	
		0	1	Prescaler output (ORCLK)	
$W2_0$		1	0	CNTR0 input	
		1	1	System clock (STCK)	

Note1: “R” represents read enabled, and “W” represents write enabled.

4. Application Examples of Interrupt

4.1 External 0 Interrupt

INT, an external interrupt pin, select s valid waveform and detects a falling edge (H→L), a rising edge (L→H) or both edges (H→L and L→H).

Overview: Performs external 0 interrupt with a falling edge (H→L), a rising edge (L→H), or bothe edges (H→L and L→H) as a trigger.

Specification: Enables external 0 interrupt to occur by detecting both edges of the external signal.

Figure 4.1 shows the opearation example of external 0 interrupt whereas Figure 4.2 provides the setting example of external 0 interrupt.

4.2 Timer 1 Interrupt

Using Timer 1, a fixed-cycle interrupt based on the setting value can be performed.

Overview: Performs a fixed-cycle interrupt by underflow singnal of timer 1

Specification: Allows timer 1 interrupt to perform at an interval of 1 ms using the prescaler and timer 1 to divide the system clock frequency (= 4.0 MHz).

Figure 4.3 shows the setting examples of timer 1 fixed-cycle interrupt.

4.3 Timer 2 Interrupt

Using Timer 2, a fixed-cycle interrrupt based on the setting value can be performed.

Overvies: Performs a fixed cycle interrupt by underflow signal of timer 2.

Specification: Allows timer 2 interupt to perform at an interval of 1.25 ms, using timer 2 to divide the system clock frequency (=2.0 MHz).

Figure 4.4 shows the setting example of timer 2 fixed-cycle interrupt

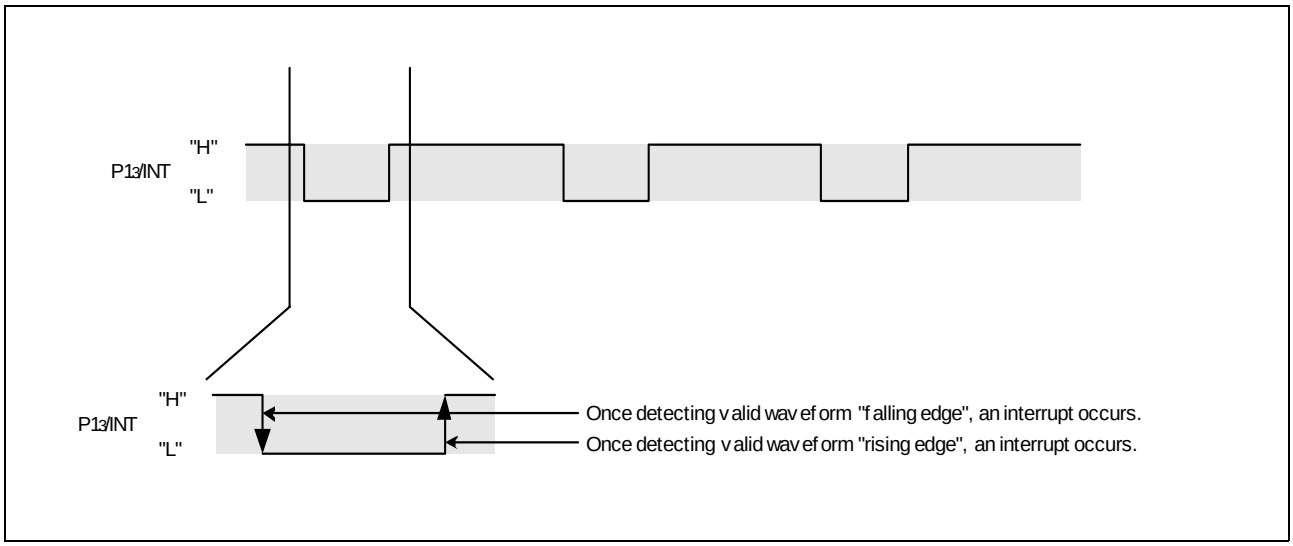
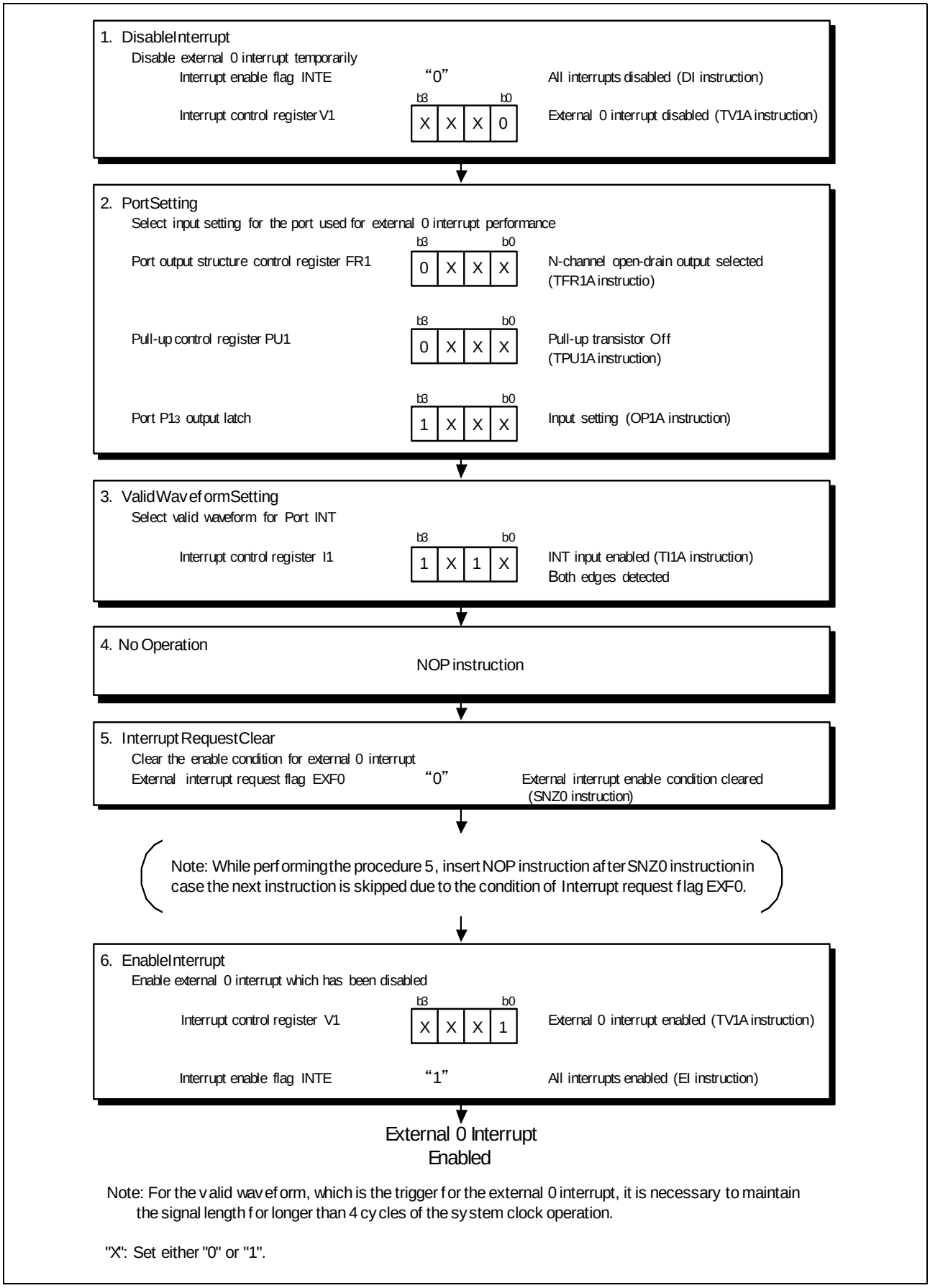


Figure 4.1 Operation Example of External 0 Interrupt



Note: For the valid waveform, which is the trigger for the external 0 interrupt, it is necessary to maintain the signal length for longer than 4 cycles of the system clock operation.

"X": Set either "0" or "1".

Figure 4.2 Setting Example of External 0 Interrupt

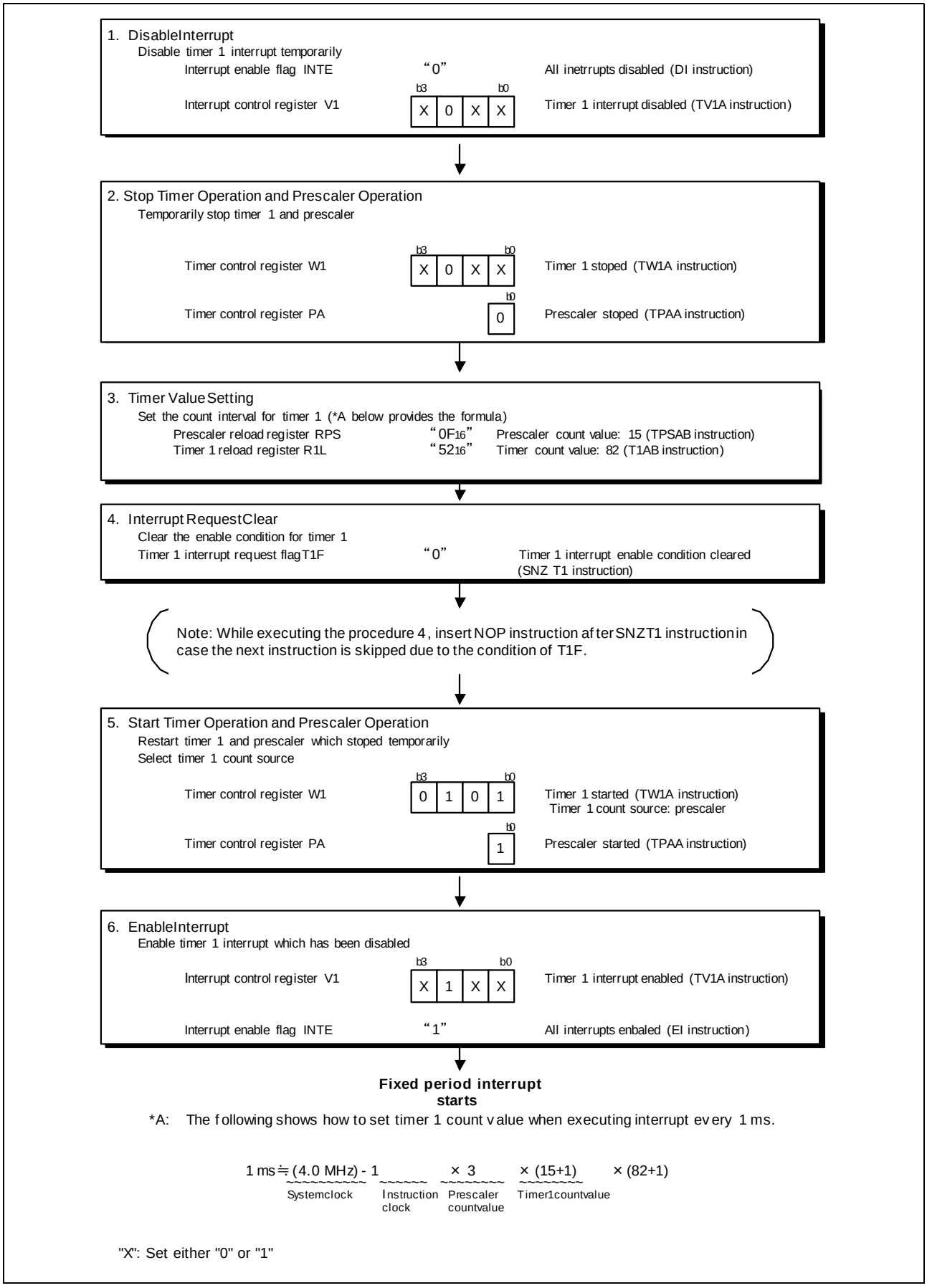
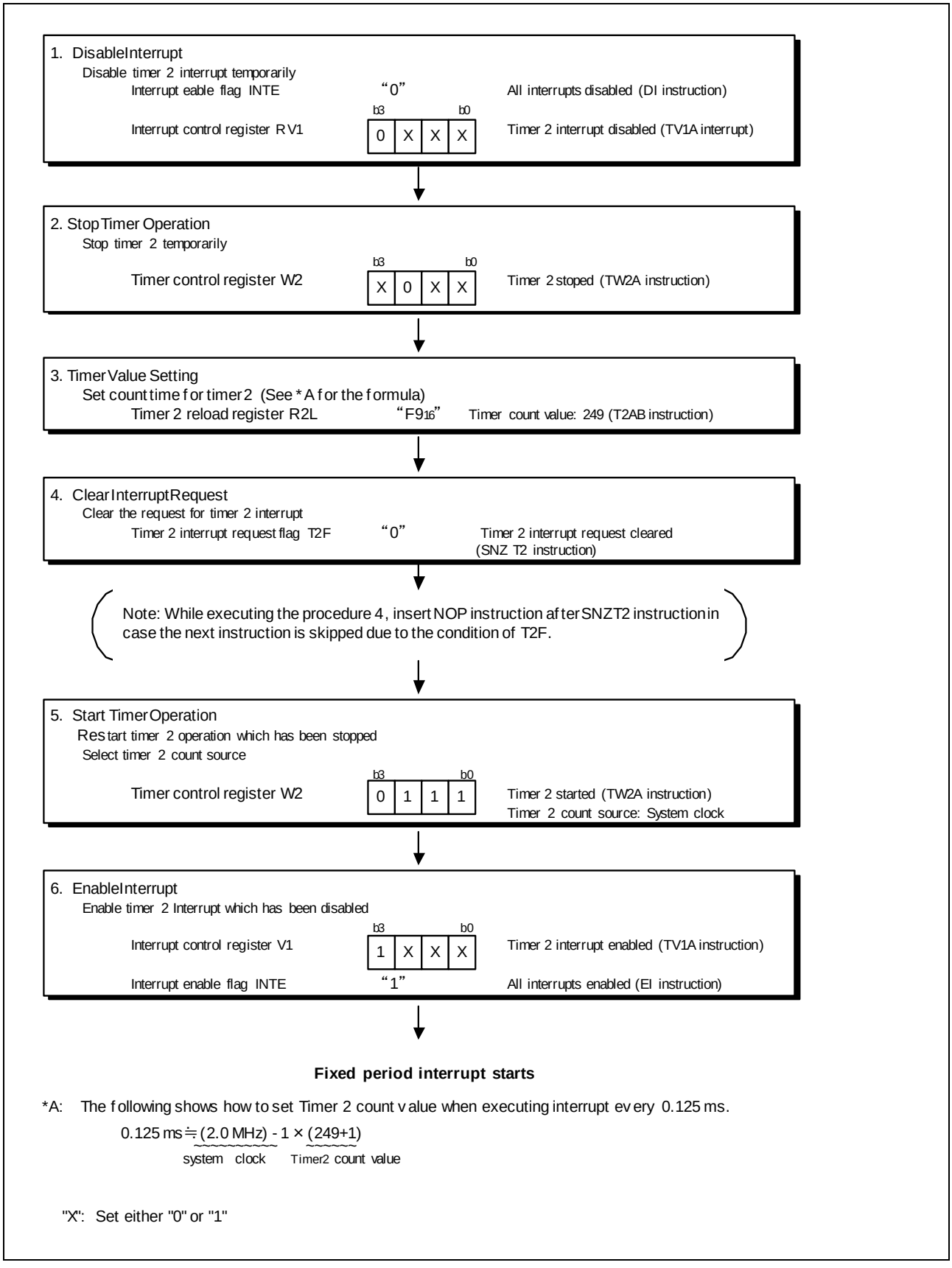


Figure 4.3 Setting Example of Fixed Cycle Timer 1 Interrupt



*A: The following shows how to set Timer 2 count value when executing interrupt every 0.125 ms.

$$0.125\ \text{ms} \fallingdotseq \underbrace{(2.0\ \text{MHz})}_{\text{system clock}} - 1 \times \underbrace{(249+1)}_{\text{Timer2 count value}}$$

"X": Set either "0" or "1"

Figure 4.4 Setting Example of Fixed Cycle Timer 2 Interrupt

5. Reference Software Programs

Reference software programs are available on Renesas Technology Corporation Website.
To obtain the programs, click “Application Note” on the left side of the 4509 Group page.

6. Reference Documents

Datasheet
4509 Group Datasheet

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Revision History	4509 Group Interrupt Application Note

Rev.	Date	Description	
		Page	Summary
1.00	July 01, 2006	—	First Edition Issued

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