

To our customers,

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# 4509 Group

## A/D Converter

### 1. Abstract

The following article introduces application examples and setting examples of A/D converter of 4509 Group.

### 2. Introduction

The explanation of this issue is applied to the following condition:

- Microcomputer: 4509 Group
- Oscillation Frequency: 4 MHz
- System Clock: Through Mode (Frequency not divided)
- Power Supply: 2.0 V - 5.5 V (Ta=0 - 50°C)  
2.7 V - 5.5 V (Ta=-20 - 85°C)

Due to the bit location for the control register, a bit with no function may be operated in some cases. Values can be optionally set on those bits.

### 3. A/D Converter Control Registers

#### 3.1 Interrupt Control Register V2

Table 3.1 depicts the bit configuration for Interrupt control register V2.

Writing to register V2 can be performed by TV2A instruction after setting values to register A.

Further, contents of register V2 can be transferred register A by TAV2 instruction.

Table 3.1 Bit configuration for Interrupt Control Register V2

Interrupt control register V2		at reset: 0000 <sub>2</sub>		at RAM back-up: 0000 <sub>2</sub>		R/W TAV2/TV2A	
V2 <sub>3</sub>	Serial Interface interrupt enable bit	0	Disabled (SNZSI instruction is valid)				
		1	Enabled (SNZSI instruction is invalid)				
V2 <sub>2</sub>	A/D interrupt enable bit	0	Disabled (SNZAD instruction is valid)				
		1	Enabled (SNZAD instruction is invalid)				
V2 <sub>1</sub>	Not used	0	This bit has no function but read/write is enabled				
		1					
V2 <sub>0</sub>	Not used	0	This bit has no function but read/write is enabled				
		1					

Note 1. “R” represents read enabled, and “W” represents write enabled.

Note 2. : Unused bits when setting A/D converter

#### 3.2 A/D Control Register Q1

Table 3.2 displays the bit configuration for A/D control register Q1.

Writing to register Q1 can be performed by TQ1A operation after setting values to register A.

Further, contents of register Q1 can be transferred to register A by TAQ1 instruction.

Table 3.2 Bit Configuration for A/D Control Register Q1

A/D control register Q1		at reset : 0000 <sub>2</sub>			at RAM back-up: state retained		R/W TAQ1/TQ1A	
Q1 <sub>3</sub>	A/D operation mode selection bit	0	A/D conversion mode					
		1	Comparator mode					
Q1 <sub>2</sub>	Analogue input pin selection bit	Q1 <sub>2</sub>	Q1 <sub>1</sub>	Q1 <sub>0</sub>	Selected pins			
		0	0	0	AIN0			
0		0	1	AIN1				
Q1 <sub>1</sub>		0	1	0	AIN2			
		0	1	1	AIN3			
Q1 <sub>0</sub>		1	0	0	AIN4			
		1	0	1	AIN5			
		1	1	0	Not available			
	1	1	1	Not available				

Note 1. “R” represents read available, and “W” represents write enabled.

## 4. Application Example of A/D Converter

### 4.1 A/D Conversion Mode

Overview : Converts analog input signals, from the sensor, into digital value.

Specification : Converts analog voltage value, from the sensor, into digital value using 10-bit serial conversion method. Uses AIN0 pin as analog input pin.

Figure 4.1 illustrates the setting example of A/D conversion (without interrupt), whereas Figure 4.2 shows the setting example of A/D conversion mode (with interrupt).

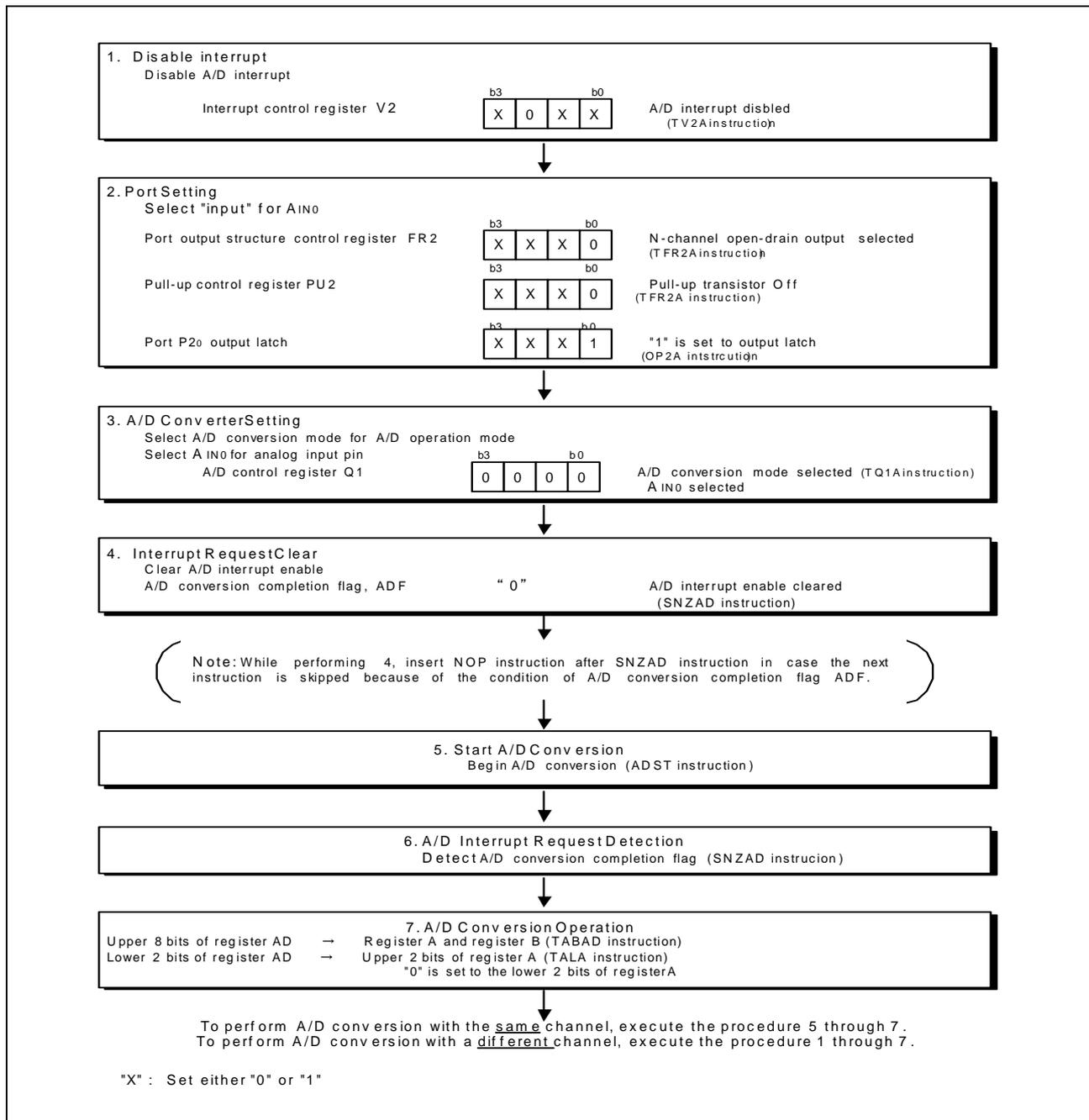


Figure 4.1 Setting Example of A/D Conversion Mode (Without Interrupt)

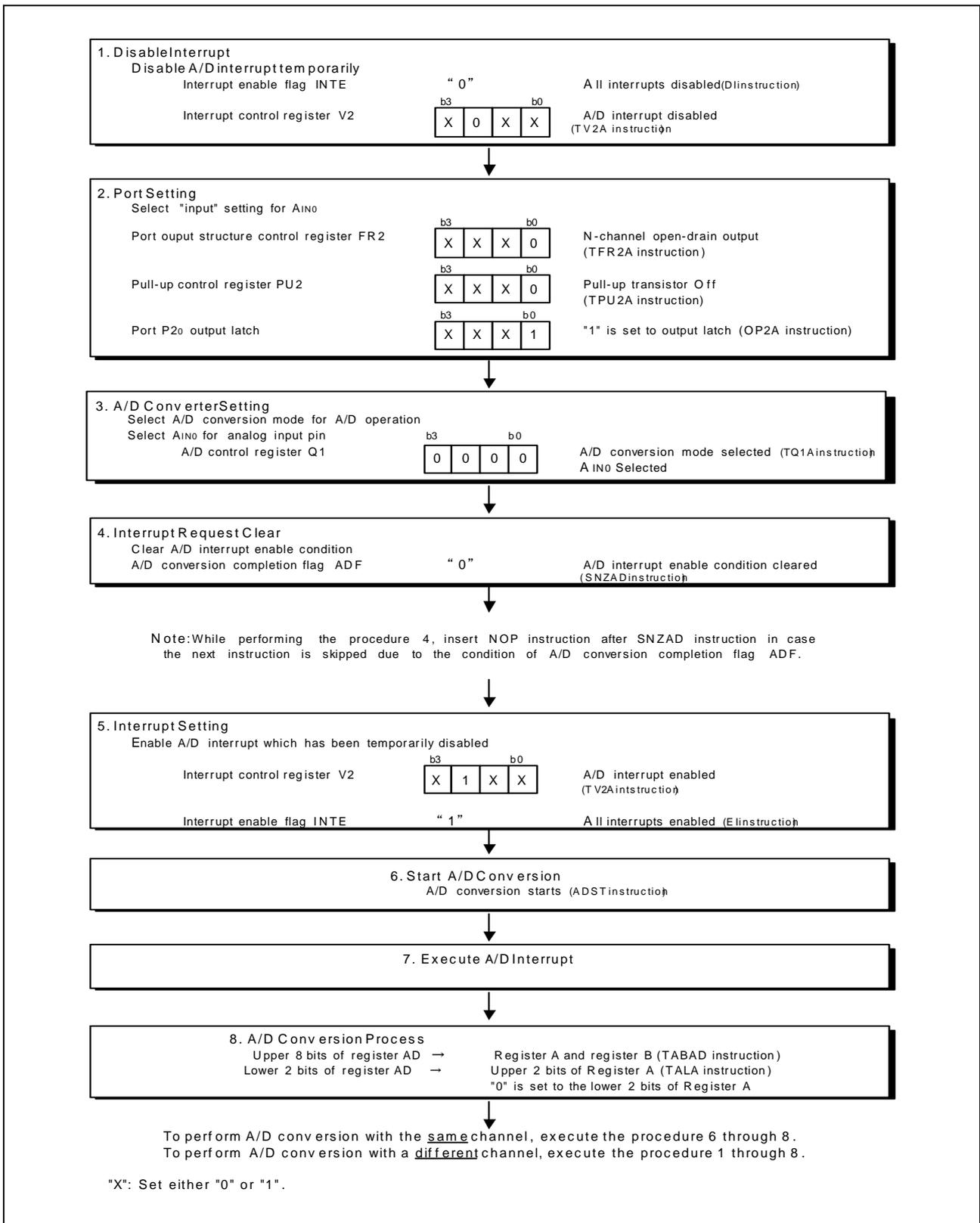


Figure 4.2 Setting Example of A/D Conversion Mode (With Interrupt)

## 5. Reference Software Programs

Reference software programs are available on Renesas Technology Corporation Website.  
To obtain the programs, click “Application Note” on the left side of the 4509 Group page.

## 6. Reference Documents

Datasheet  
4509 Group Datasheet

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Revision History	4509 Group A/D Converter Application Note
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Rev.	Date	Description	
		Page	Summary
1.00	July 01, 2006	—	First Edition Issued

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