Using the RC32434/5 Verilog Model

Application Note AN-439

Notes

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Introduction

The RC32434/5 is a member of the IDT™ Interprise™ family of PCI integrated communications processors. It incorporates a high performance CPU core and a number of on-chip peripherals. Using a highly sophisticated direct memory access (DMA) engine, the RC32434/5 integrated processor is designed to transfer information from I/O modules to main memory with minimal CPU intervention.

The RC32434/5 Verilog Model is a bus functional model designed to be used in a simulation environment with other verilog device models to simulate a system, thus enabling the designer to verify connectivity and functionality of the devices being used in the system prior to physically building the system. This document describes the contents of the RC32434/5 Verilog Model package and how to compile and run the model.

Contents of the Verilog Model Package

The RC32434/5 Verilog Model package, rc434_bfm.tar, is comprised of the following files:

- jade_vmc_model.vcs.v — Protected form of the MIPS 4Kc (“Jade”) RTL using the SWIFT language.
- all_rtl-jade.vp — Encrypted RC32438 RTL (except the Jade core).
- boot_mem.v — 8-bit wide boot ROM model attached to chip select 0 - csn[0].
- mt46v16m16.v — Micron Technology DDR memory model attached to DDR chip select 0 - ddrcsn[0].
- Makefile — Used to compile the executable VCS simulator.
- memory.jade_config — Used to customize MIPS-4Kc VMC model, however, this file should not require modification. See MIPS 4Kc Integrator's guide documentation for more details.
- system.v — Top-level Verilog file that instantiates everything and creates the clocks and resets.
- program.srec — Sample program S-Record file.
- program.dis — Sample program disassembly file.
- memmod0_0.mem — 8-bit wide hex memory image loaded by the boot memory model.
- memmake — Perl script that calls srec2mem and memsplit scripts with parameters.
- srec2mem — Executable for Solaris that converts S-Records into an intermediate memory image.
- memsplit — Executable for Solaris that converts the output of srec2mem into an 8-bit wide memory image required by the boot_mem.v model.

The sample boot code provided is automatically loaded into the boot memory model at startup. However, customized boot code can be substituted by replacing one or both of the hex image files. The helper scripts (memmake, srec2mem, and memsplit) are provided to convert the S-Records into the required hex format.

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Additional Requirements

To compile and run the RC32434/5 Verilog Model the user must have the following licenses and tools:

- FlexLM License File — Required for the Jade VMC model (www.mips.com).
- VCS 6.1 (Synopsys) — Used to compile the model. Note that only version 6.1 has been tested.
- SignalScan or other waveform viewer tool.

Test Bench

Figure 1 shows the sample test bench used in this model. Designers can vary this test bench as required.

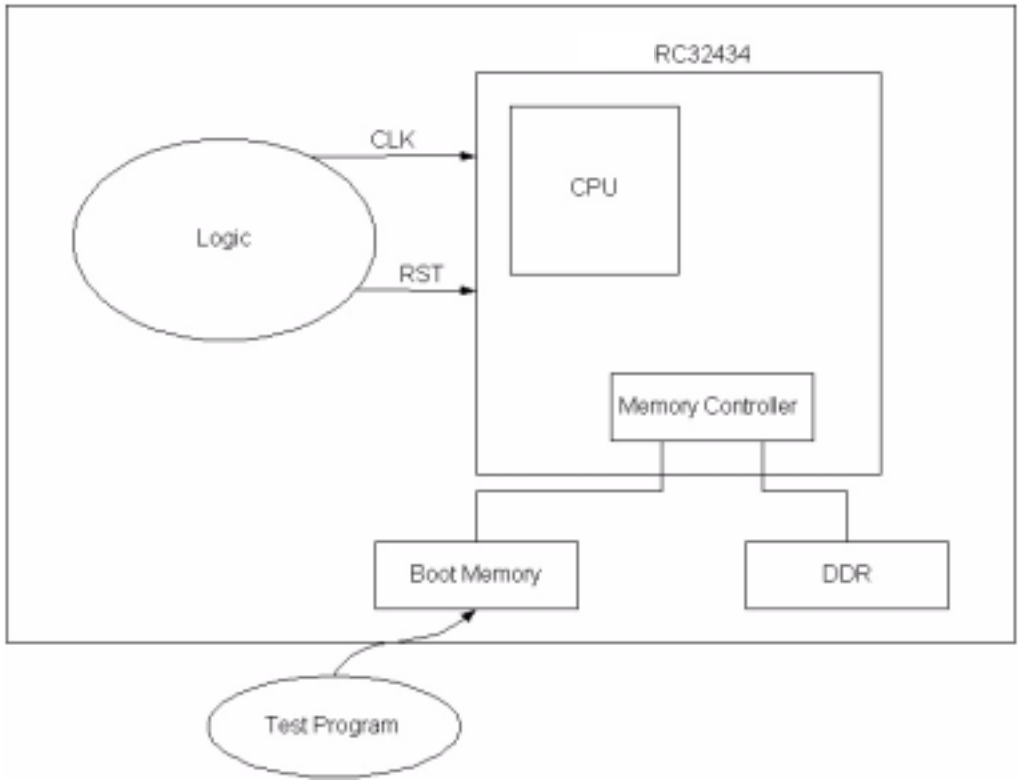

Figure 1 RC32434/5 Sample Test Bench

Using the Verilog Model

This section describes the various steps involved in compiling and running the RC32434/5 model.

Getting Started

Extract the compressed files from the rc32434_bfm.tar file. The files will be extracted to a folder called “rc32434_bfm”. Also, verify the Flex license from MIPS, any other necessary license(s), and the tools are correctly installed.

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Compiling the Verilog Simulator

a) Customize the Makefile as follows:

- Choose the appropriate VCS command/path.
- Link the desired PLI for signal dumping (e.g. Signal Scan, Debussy, etc.).
- Add RTL files for other models if desired.

b) Customize the system.v file as follows:

- If desired, instantiate additional device models.
- If desired, modify clocks, resets, pull up/down resistors, etc.
- If desired, modify the boot vector (configuration data latched by the processor during cold reset).
- If desired, modify Signal Scan recording options.

c) Type 'gmake' to build the rc32434_bfm executable.

Compiling a Test

If you are using the included sample test, skip this part and go to the next section, Running a Simulation.

If you are not using the included sample test, perform the following steps:

- Generate an S-Record file of the test you would like to perform with your compiler/tool.
- Convert the .srec format into a hex format required by the boot memory model. The following three helper scripts are provided for this:

  memmake — Perl script that calls the srec2mem and memsplit scripts with parameters.

  srec2mem — Executable for Solaris that converts the S-Records into an intermediate memory image.

  memsplit — Executable for Solaris that converts that output of srec2mem into the 8-bit wide memory image file required by the boot memory model.

Running a Simulation

Type 'rc32434_bfm' at the command line prompt. The simulation will automatically terminate when it has reached the end. However, the designer can terminate the simulation while it is running by writing to the special offset address of 0x300000 in Device0 space.

Conclusion

The RC32434/5 Verilog Model is easy to implement as a stand-alone or system test bench using the files contained in the RC32434/5 Verilog Model Package. Following the steps outlined in this document will ensure ease of model integration into a system level simulation test environment.

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