SDRAM Architecture, Signals and Routing Considerations for the RC32365

Application Note AN-437

Notes

By Rakesh Bhatia

Introduction

The RC32365 device is a member of the IDT™ Interprise™ family of integrated communications processors. It provides a single chip solution for virtual private network (VPN) platforms with bandwidth requirements ranging from full T1/E1 through fractional T3. Featuring a MIPS CPU core, the device also includes a memory controller supporting SDRAM memory, a PCI interface featuring an on-chip arbiter to simplify the design of embedded systems, and a security module that accelerates IPSEC performance.

This application note provides information on board architecture, signal routing requirements, and system loading requirements that should be followed when designing an SDRAM-based memory subsystem capable of operating at the maximum system bus frequency/s of the processor.

Architectural Design

The SDRAM controller provides a glueless interface to industry standard SDRAMs and SDRAM SODIMMs. The SDRAM controller provides two chip selects (SDCSN [1:0]) with each chip select supporting two or four internal SDRAM banks. Two internal banks are supported when 16 Mb SDRAMs are used and four internal banks when 64 Mb, 128 Mb, 256 Mb, 512 Mb SDRAMs are used. Each SDRAM chip select (that is, external SDRAM bank) supports a 32-bit data path.

For maximum SDRAM speed, it is recommended that all SDRAM control and data signals be directly connected to the RC32365. All other memory devices should be placed behind the data and address buffers. The SDCLKOUT pin should be used to drive only the clocks on the SDRAM chips. It should not be used to drive any other device on the board.

The SDCLKINP clock is used to clock in the data from the SDRAM. The SDCLKINP signal should be tapped off from the SDCLKOUT at the SDRAM. The length of the resulting SDCLKINP trace should match the SDRAM data trace length as much as possible. In no case should the length of the SDCLKINP trace exceed the length of the SDRAM data traces. The SDRAM data flow architecture for normally loaded systems is shown in Figure 1 below.

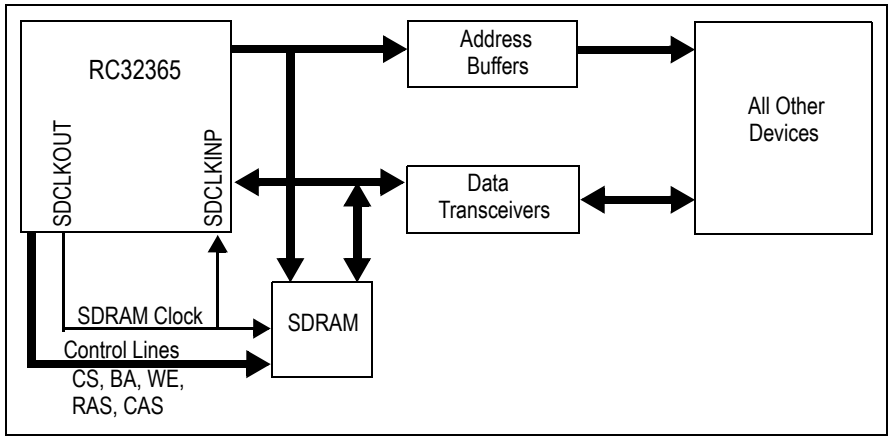

Figure 1 SDRAM Data Flow Architecture for Normally Loaded Systems

Notes

The SDRAM data flow architecture for heavily loaded systems is shown in Figure 2 below. The timing of the data path through data transceivers must be considered when designing such systems.

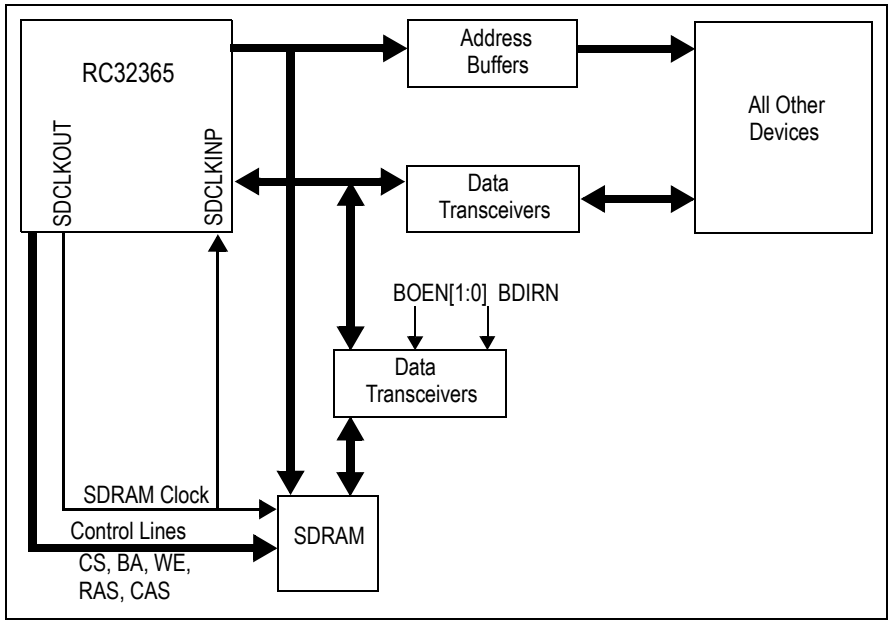

Figure 2 SDRAM Data Flow Architecture for Heavily Loaded Systems

Signal Routing

To provide the most margin for SDRAM hold times:

- *Keep all signals going to the SDRAM, address, data, and control signals as short as possible*
- *Match trace lengths as close as possible*
- *Minimize as much as possible the trace length for SDCLKOUT (this is very important)*
- *Make the SDCLKOUT trace the shortest SDRAM trace on the board*
- *Match the length of the SDCLKINP to the SDRAM data lines.*

Although this optimum configuration may not be achievable, the more the layout deviates from this configuration, the less margin there is for SDRAM hold times.

System Loading

To support maximum speeds, reasonable SDRAM loading constraints must be followed. For high-speed operation, it is recommended that no more than 6 loads (total) be used. For example, a system with four discrete SDRAM chips, a PROM and possibly one other peripheral can be connected directly to the processor. It is acceptable to use a SODIMM or DIMM, provided it does not contain more than four chips. In addition, any unused clock lines should be left unconnected; otherwise, the loading on SDCLKOUT could exceed the drive capability of the RC32365 SDCLKOUT pin.

It is possible to use more than four SDRAM chips or very large DIMMs at lower speeds. However, if the loading exceeds the above recommendation, users should buffer all of the control, address, and data lines accordingly. Because of the extra delay associated with this, higher system speeds are not achievable. Also, timing analysis should be done when designing such systems. To calculate maximum possible system speeds for specific designs, users should review the RC32365 Data Sheet on IDT's RC32365 web page and the data sheets for the buffers and other devices being used.

Notes

Connecting SDRAM Clocks

SDRAM accesses are expected to operate at the full bandwidth of the system clock (CLK). In order to accomplish this, the RC32365 provides an output clock (SDCLKOUT) and accepts an input clock (SDCLKINP). Both clocks run at the same frequency as CLK. The output clock, SDCLKOUT, should be connected to the SDRAM chips and returned to the RC32365 through SDCLKINP. Figure 3 below shows the connection of SDRAM clocks.

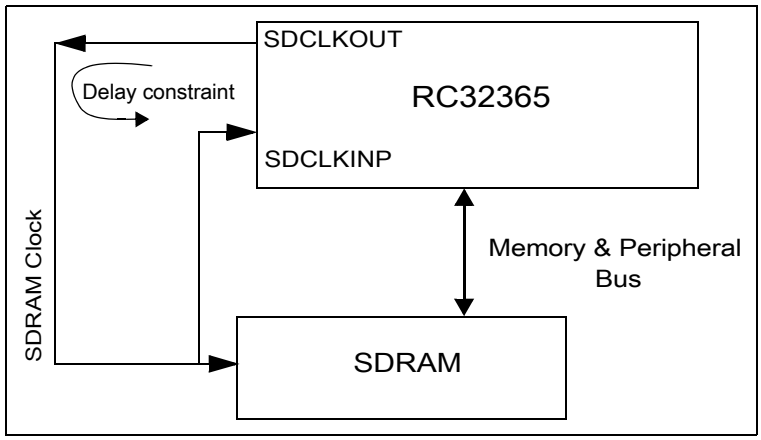

Figure 3 Connection of SDRAM Clocks

When accessing SDRAMs, the RC32365 outputs all SDRAM control signals (such as RASN, MADDR, BWEN, SDWEN, etc.) relative to SDCLKOUT. SDCLKINP is used to register SDRAM read data. This implies that all signals going to the SDRAM chips from the RC32365 must meet setup and hold times relative to SDCLKOUT, while signals going to the RC32365 from the SDRAM chips (i.e., the SDRAM read data) must meet setup and hold times relative to SDCLKINP. Finally, as shown in Figure 3, the circuit board routing and load delay of the SDRAM clock must be within the limits specified in the data sheet.

SODIMM Support

The SDRAM controller can be configured to control SODIMMs. In this mode, the RC32365 drives eight data masks (four on BWEN [3:0] and four on MADDR [20:17]). Because the RC32365 data bus is 32-bits wide and an SODIMM supports a 64-bit data path, either BWEN [3:0] or MADDR [20:17] will control the accessing of the correct word to the SODIMM, depending on the state of an internally decoded upper address bit. To connect an SODIMM to the RC32365, connect the 32-bit data bus (MDATA [31:0]) to the 64-bit data bus of the SODIMM. MDATA [0] connects to SODIMM DATA [0] and SODIMM DATA [32]; MDATA [1] connects to SODIMM DATA [1] and SODIMM DATA [33], and so on. Connect MADDR [20:17] to the upper data masks of the SODIMM (DQM [7:4]) and BWEN [3:0] to the lower data masks (DQM [3:0]).

All remaining SDRAM control signals are connected as usual. SODIMM mode is enabled by setting the SODIMM Mode Enable (SOD) bit in the SDRAMC register. The SDRAMC register DTYPE field is configured with the type of SDRAMs on the SODIMM. For SODIMMs that require two chip selects (SDCSN [0|1]), both SDRAM memory regions must be configured so that the two regions are equal, contiguous, and together total the amount of memory on the SODIMM. For an example, see Figure 4.

Notes

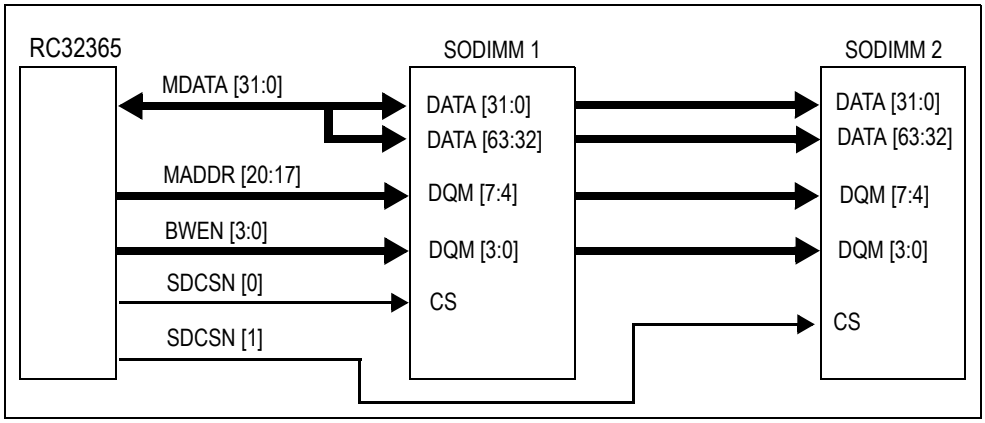

Figure 4 SODIMM Connection Example

SDRAM System Example

The purpose of this example is to show how to program the SDRAM controller with the RC32365 and 128MB of SDRAM (SODIMM). Refer to Figure 4. Because the system uses two 64MB SODIMMs, one of the SODIMMs must be connected to SDCSN [0] and the other to SDCSN [1]. Finally, because each of the two SODIMMs provides 64MB and is connected to one of the RC32365's SDRAM chip-selects, the SDRAM Base and Mask registers could be programmed to the following:

- *SDRAMC.DTYPE = 2Mb x 8 x 4 (the SODIMM is composed of eight 2Mb x 8 x 4 SDRAM chips).*
- *SDRAMC.SOD = 1 (enable SODIMM mode).*

SDRAM0BASE = 0x0000_0000
SDRAM0MASK = 0xFC00_0000 — 64MB

SDRAM1BASE = 0x0400_0000
SDRAM1MASK = 0xFC00_0000 — 64MB

Note: The above Base and Mask register programming will allocate 128MB of continuous SDRAM space starting at physical address 0x0000_0000. If each SODIMM is composed of eight 2Mbx8x4 SDRAM chips, the SDRAMC register must be programmed as follows:

Other SDRAM fields, such as CL, RCD, RP, and RC should be programmed to values consistent with those in the SODIMM's specification. Note that if DIMMs are used, they should contain a maximum of 8 chips. For example, if two DIMMs are used, each DIMM should contain no more than four chips.

Design Resources

Detailed information on the 79EB365 evaluation board, which is designed to support the maximum system bus frequencies, is available at:

http://www.idt.com/products/pages/Integrated_Processors-79RC32365.html

Notes

The SDRAM board architecture is depicted in Figure 5.

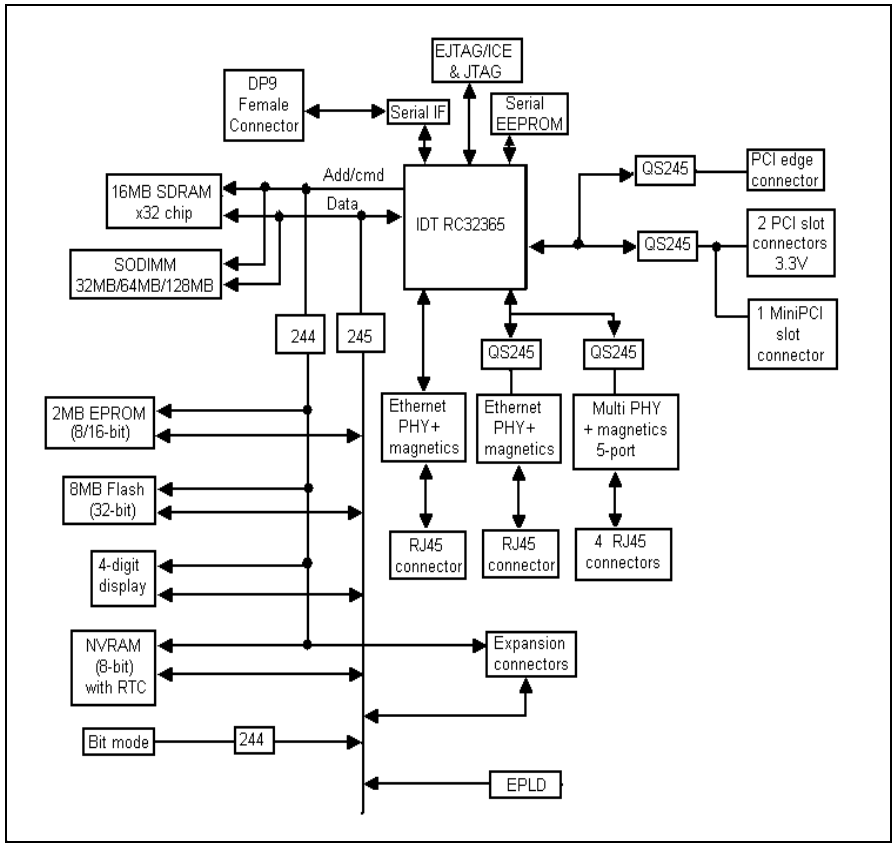

Figure 5 Block Diagram of the 79EB365 Evaluation Board

Acknowledgements

The following persons contributed to this document by providing technical content.

Harold Gomard, IDT Inc.

Paul Snell, IDT Inc.

References

79RC32365 Data Sheet — IDT Inc.

79RC32365 User Reference Manual — IDT Inc.

79EB365 Evaluation Board Manual — IDT Inc.

SDRAM Architecture, Signals and Routing, AN 260 — Paul Snell, IDT Inc.