LINECARD SOLUTIONS WITH THE IDT8216X1 AND IDT821054A

Application Note AN-408

IDT ADVANTAGE

- 5 V (CODEC & SLIC) and Battery Power Supply
- DSP-Based: Single LineCard Design Meets Different Standards Worldwide
- Internal Polarity Reversal
- On-Chip Thermal Management
- Less External Components
- High Reliability and Robust (ESD > 2000 V, Latch-up > 100 mA)
- Cost-Effective

OTHER FEATURES OF THE SLIC:

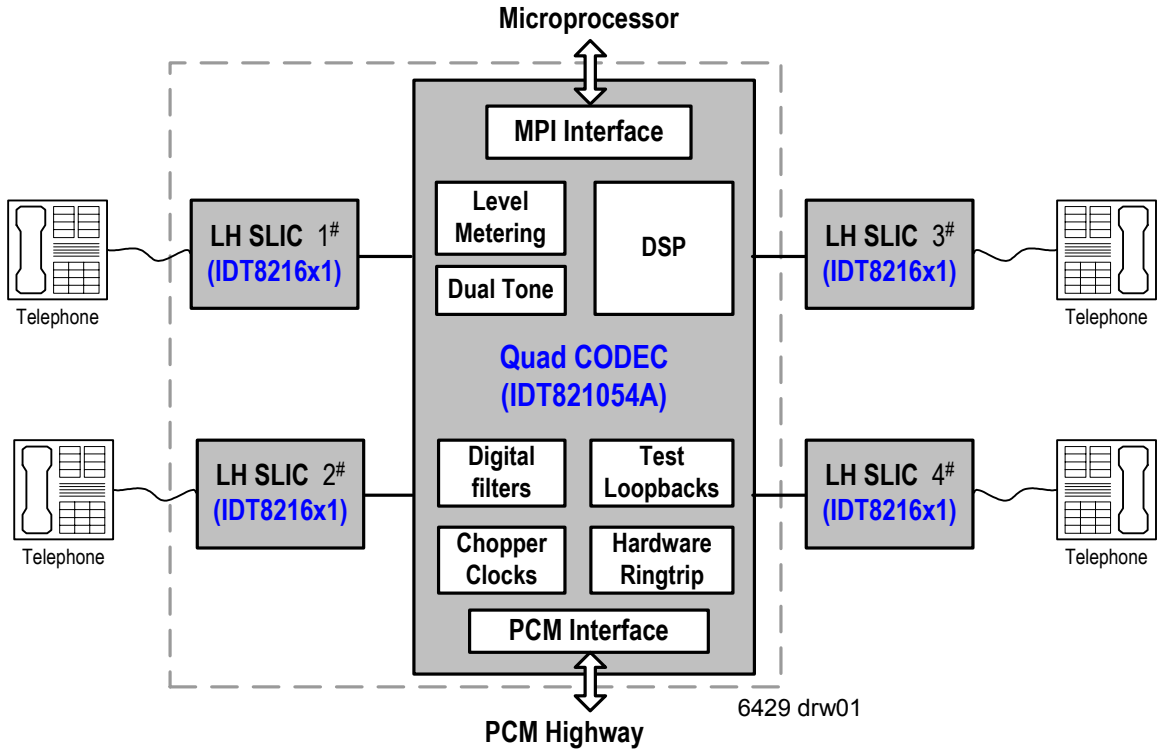
- Slic operating states: Active, Reverse Active, Ringing, Standby and Disconnect
- Low Standby power consumption (35 mW)
- -19 V to -58 V Battery Supply
- On-Hook Transmission
- Two-Wire impedance set by single external impedance
- Programmable constant-current feed
- Programmable loop-detect threshold and ring-trip detect threshold
- Three on-chip relay drivers and relay snubbers

Programmable digital filters adapting to different requirements:

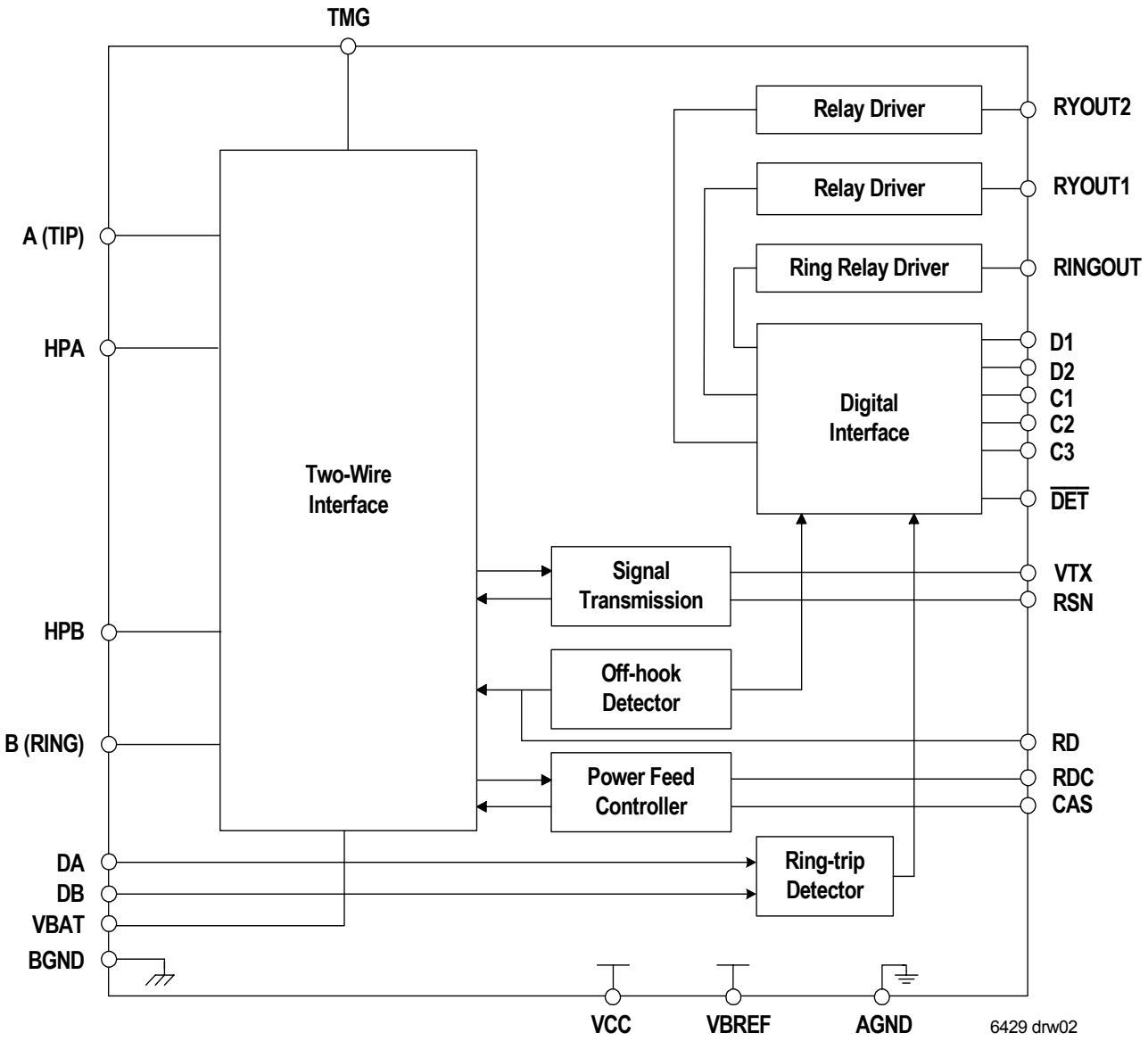
- — AC impedance matching
- — Transhybrid balance
- — Frequency response correction
- — Gain adjustment

- Programmable A/u-law compressed or linear code conversion
- Supports two programmable PCM buses and MPI interface
- 7 SLIC signaling pins per channel
- Two programmable dual tone generators per channel
- Two programmable chopper clocks
- Advanced test capability (level metering and programmable loopbacks)

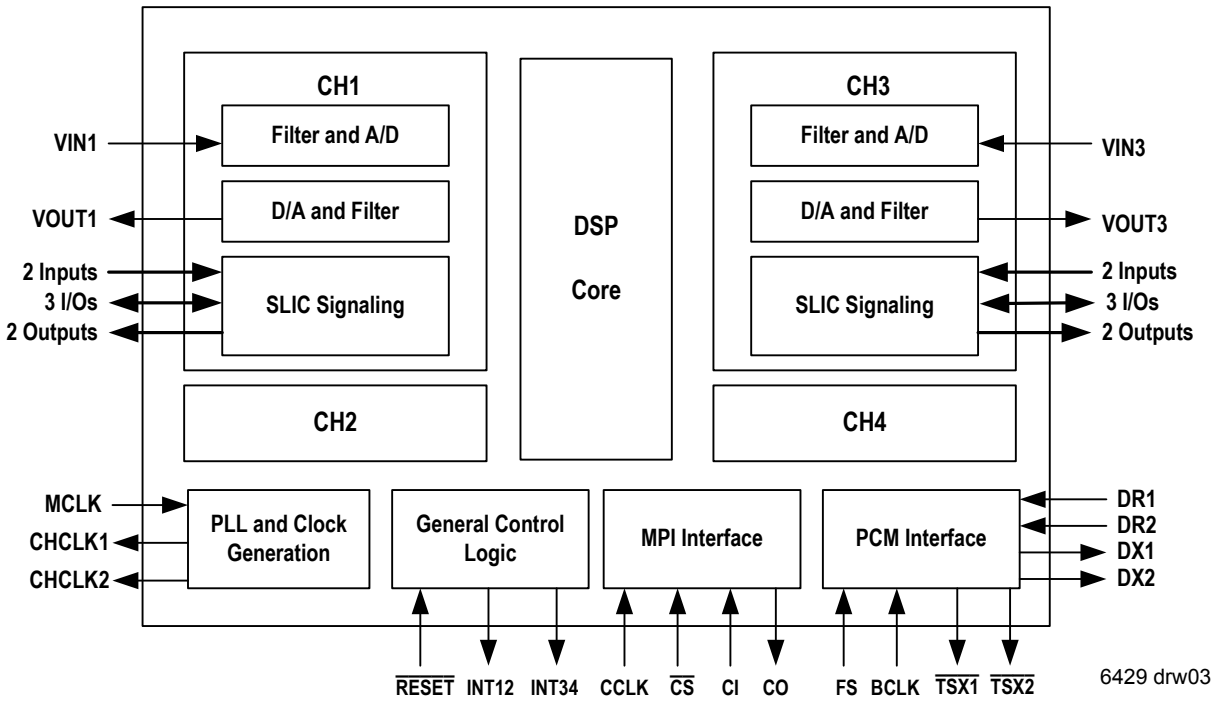
TOTAL SOLUTION BLOCK DIAGRAM



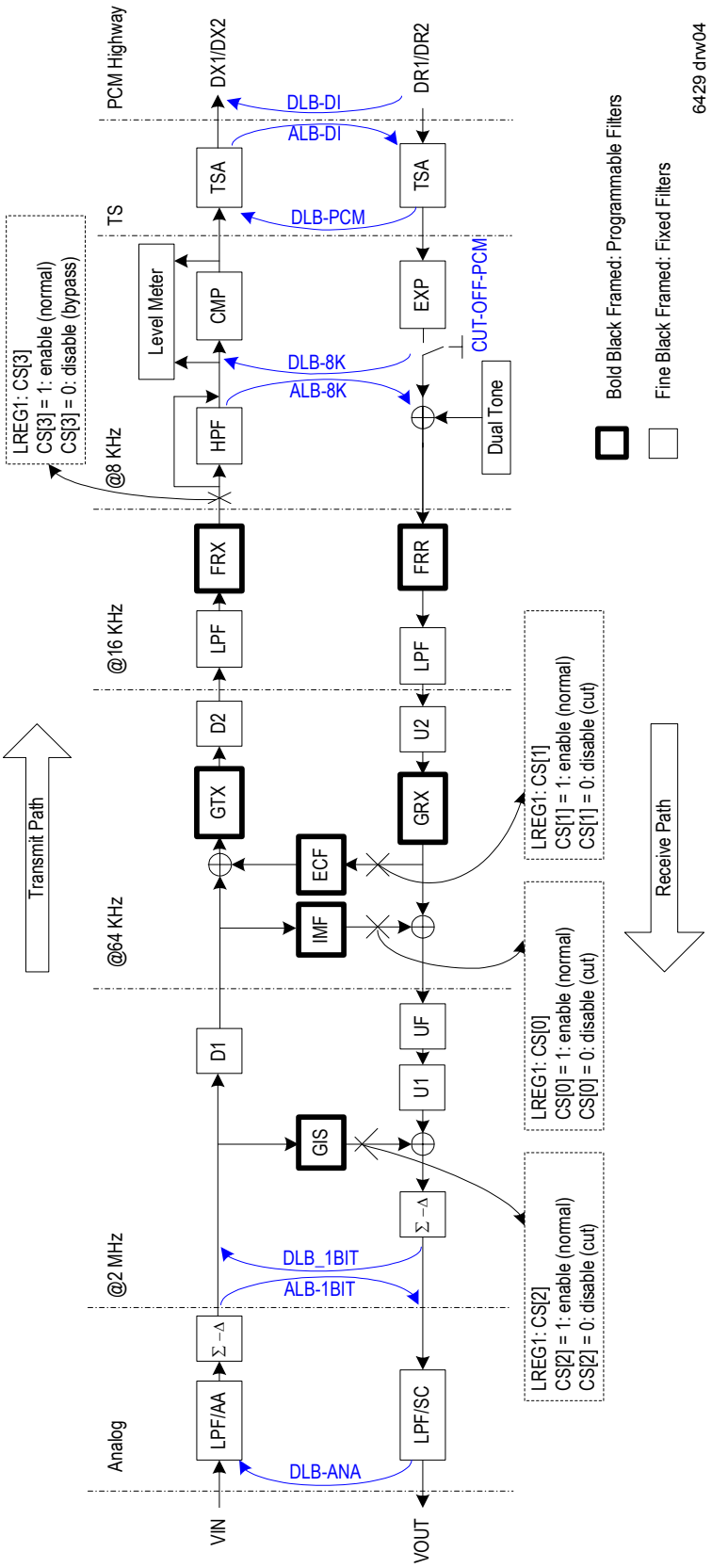
SLIC FUNCTIONAL BLOCK DIAGRAM

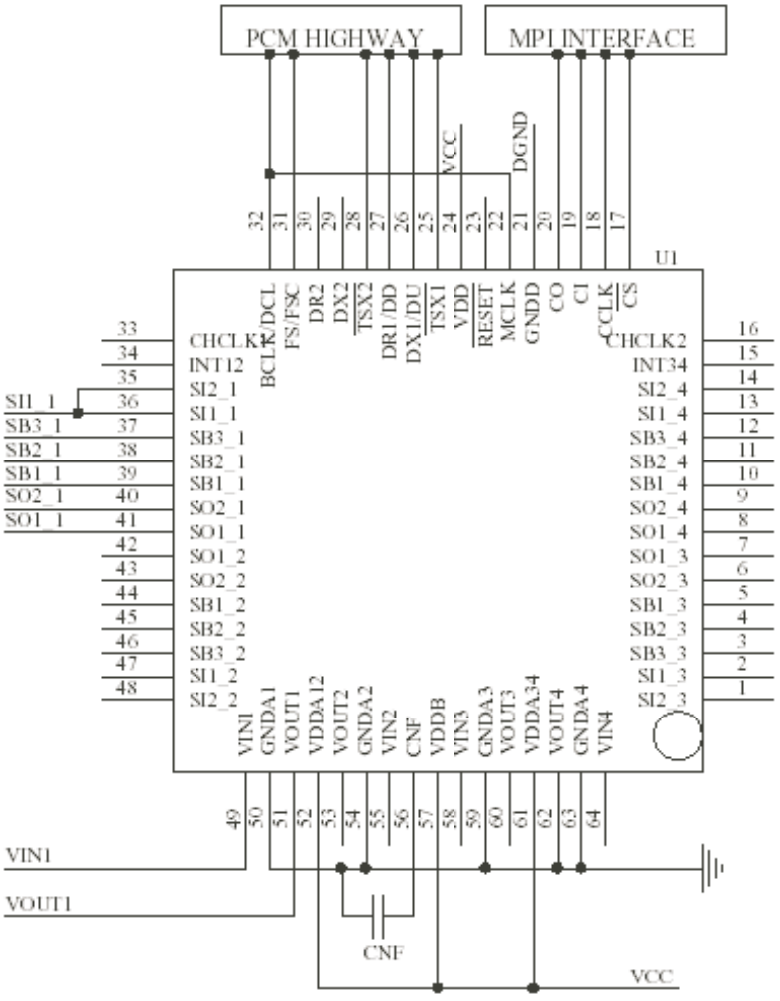


CODEC FUNCTIONAL BLOCK PROGRAM



CODEC SIGNAL FLOW DIAGRAM





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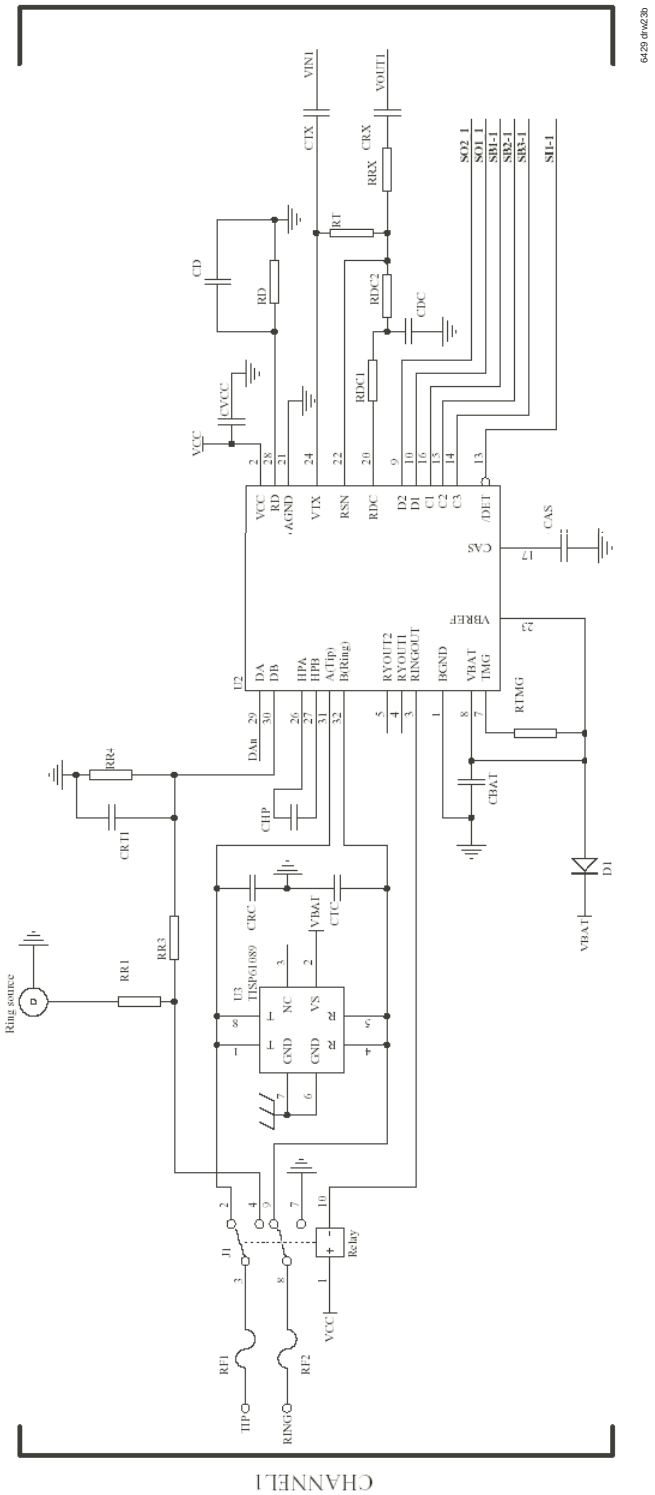
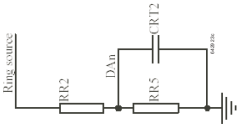




COMPONENTS LIST:

Designator	Description	Part Type	Precision	Maximum Power/Voltage	Other
CAS	Capacitor	0.1uF	10%	100V	
CNF	Capacitor	0.1uF	10%	16V	
CRC	Capacitor	2.2nF	10%	100V	
CTC	Capacitor	2.2nF	10%	100V	
CTX	Capacitor	0.1uF	10%	16V	
CRX	Capacitor	0.1uF	10%	16V	
CD	Capacitor	0.01uF	10%	16V	
CVCC	Capacitor	0.1uF	20%	16V	
CBAT	Capacitor	0.01uF	20%	100V	
CHP	Capacitor	0.27uF	10%	100V	
CDC	Capacitor	0.27uF	10%	16V	
CRT1	Capacitor	33nF	10%	100V	
CRT2	Capacitor	33nF	10%	100V	
RR2	Resister	4M	10%	1/4W	
RR3	Resister	3.4M	10%	1/4W	
RTMG	Resister	2K	10%	1W	
RR5	Resister	3.4M	10%	1/4W	
RDC2	Resister	27K	1%	1/4W	
RDC1	Resister	27K	1%	1/4W	
RD	Resister	36K	1%	1/4W	
RRX	Resister	120K	1%	1/4W	
RT	Resister	120K	1%	1/4W	
RR1	Resister	800	10%	1W	
RR4	Reisister	4M	10%	1/4W	
RF1	Fuse	50	1%	1W	
RF2	Fuse	50	1%	1W	
D1	DIODE			100V, 100mA	
U1	IDT821054A				
U2	IDT8216x1				
J1	Relay				

COEFFICIENTS IN DSP RAM 600Ω

The system target gain from tip / ring to digital port: 0 dB
The system target gain from digital port to tip / ring: 0 dB

Coefficients in the DSP Ram From low address to high address:

IMF Ram:	C6	FD	6B	04	00	00	00	00	00	00	00	00	00	00	00	00
ECF Ram:	42	F4	A4	15	00	00	00	00	00	00	04	54	CE	E0	00	00
GIS + Dual Tone Ram:	00	00	08	FC	00	00	00	00	00	00	00	00	00	00	00	00
FRX + GTX Ram:	70	00	37	F3	16	20	16	20	37	F3	70	00	99	31	F0	07
FRR + GRX Ram:	38	01	13	00	0B	3E	0B	3E	13	00	38	01	CE	84	55	1D

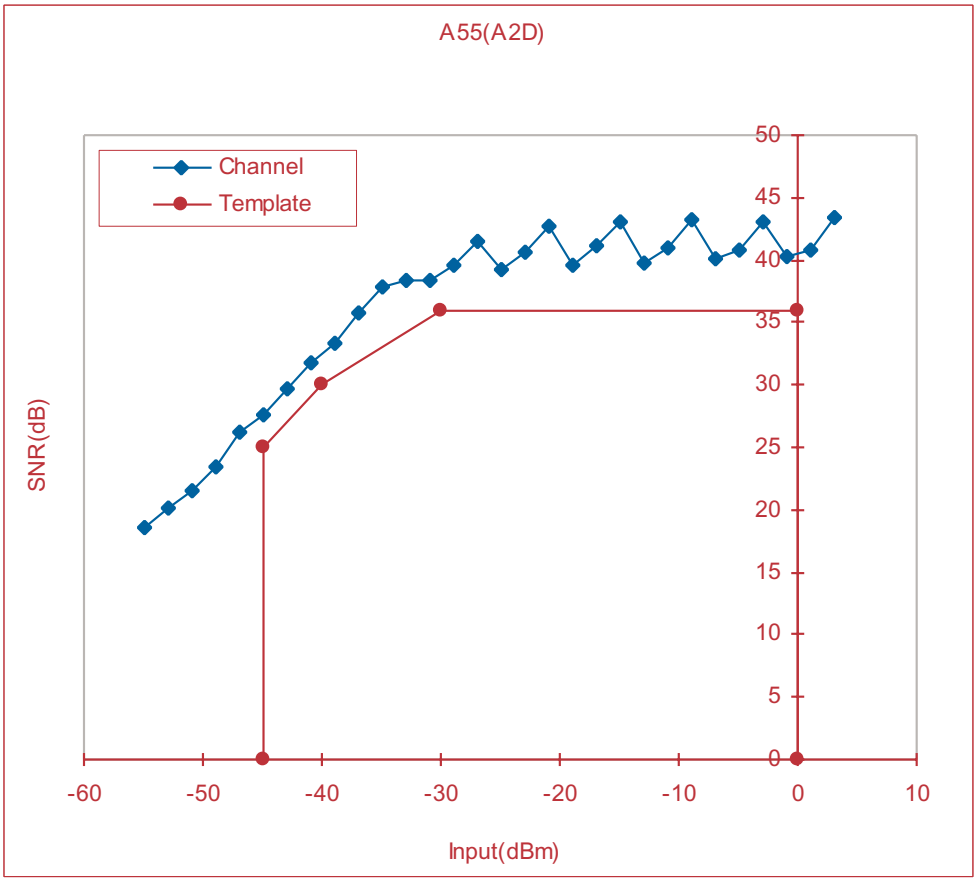
1. Select filter coefficients in the Coe-RAM by setting LREG1 to FFH;
2. Set the analog gain of A/D to 6 dB by setting the GAD bit in LREG9 to "1";
3. Set the analog gain of D/A to 0 dB by setting the GDA bit in LREG9 to "0".

Total Distortion - A55 (A2D)

(For 600Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: 0dB)

Data

Level(dBm0)	Channel
-55	18.65
-53	20.06
-51	21.54
-49	23.39
-47	26.21
-45	27.58
-43	29.75
-41	31.69
-39	33.4
-37	35.78
-35	37.79
-33	38.39
-31	38.38
-29	39.5
-27	41.55
-25	39.22
-23	40.69
-21	42.68
-19	39.56
-17	41.21
-15	43.1
-13	39.81
-11	41.05
-9	43.25
-7	40.09
-5	40.88
-3	43.12
-1	40.31
1	40.78
3	43.42



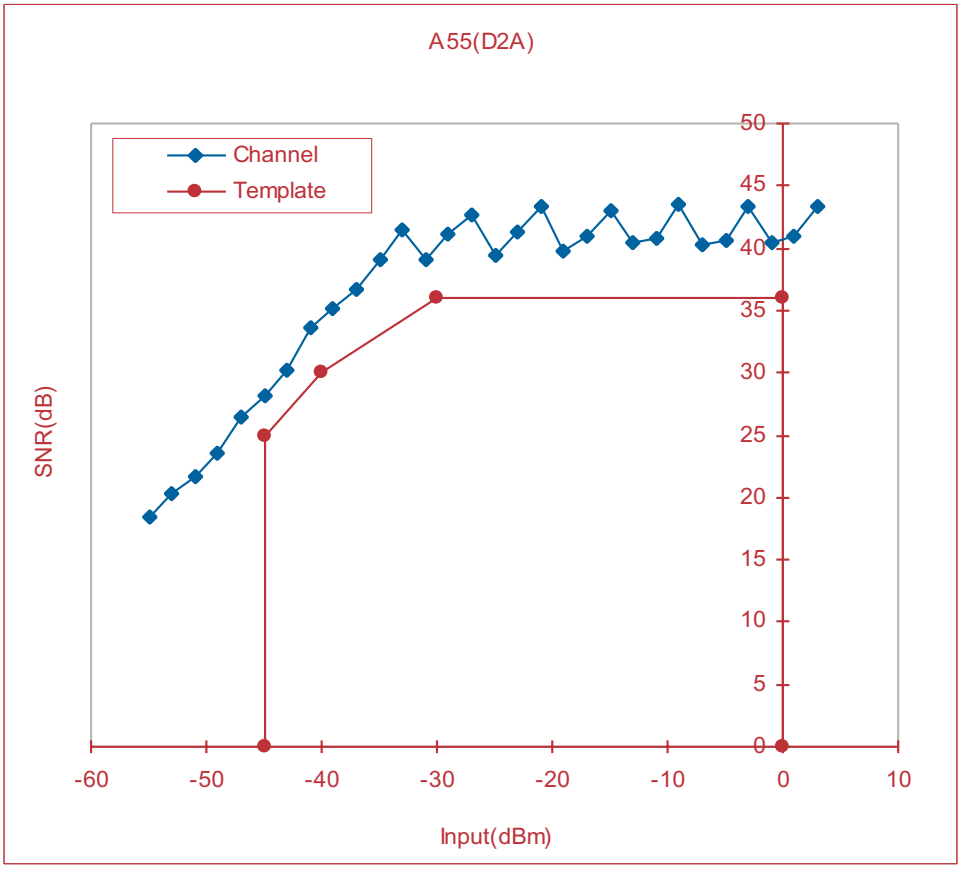
6429drw05

Total Distortion - A55 (D2A)

(For 600Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: 0dB)

Data

Level(dBm0)	Channel
-55	18.48
-53	20.32
-51	21.59
-49	23.62
-47	26.41
-45	28.21
-43	30.16
-41	33.6
-39	35.22
-37	36.72
-35	39.02
-33	41.41
-31	39.02
-29	41.19
-27	42.63
-25	39.47
-23	41.31
-21	43.28
-19	39.8
-17	41
-15	43.06
-13	40.41
-11	40.73
-9	43.56
-7	40.21
-5	40.63
-3	43.42
-1	40.51
1	41.04
3	43.3



6429drw06

COEFFICIENTS IN DSP RAM 600Ω

The system target gain from tip / ring to digital port: 0 dB
The system target gain from digital port to tip / ring: -3.5 dB

Coefficients in the DSP Ram From low address to high address:

IMF Ram:	C6	FD	6B	04	00	00	00	00	00	00	00	00	00	00	00	00
ECF Ram:	42	F4	A4	15	00	00	00	00	00	00	04	54	CE	E0	00	00
GIS + Dual Tone Ram:	00	00	08	FC	00	00	00	00	00	00	00	00	00	00	00	00
FRX + GTX Ram:	70	00	37	F3	16	20	15	20	37	F3	70	00	99	31	F0	07
FRX + GRX Ram:	38	01	13	00	0B	3E	0B	3E	13	00	38	01	CE	84	9A	13

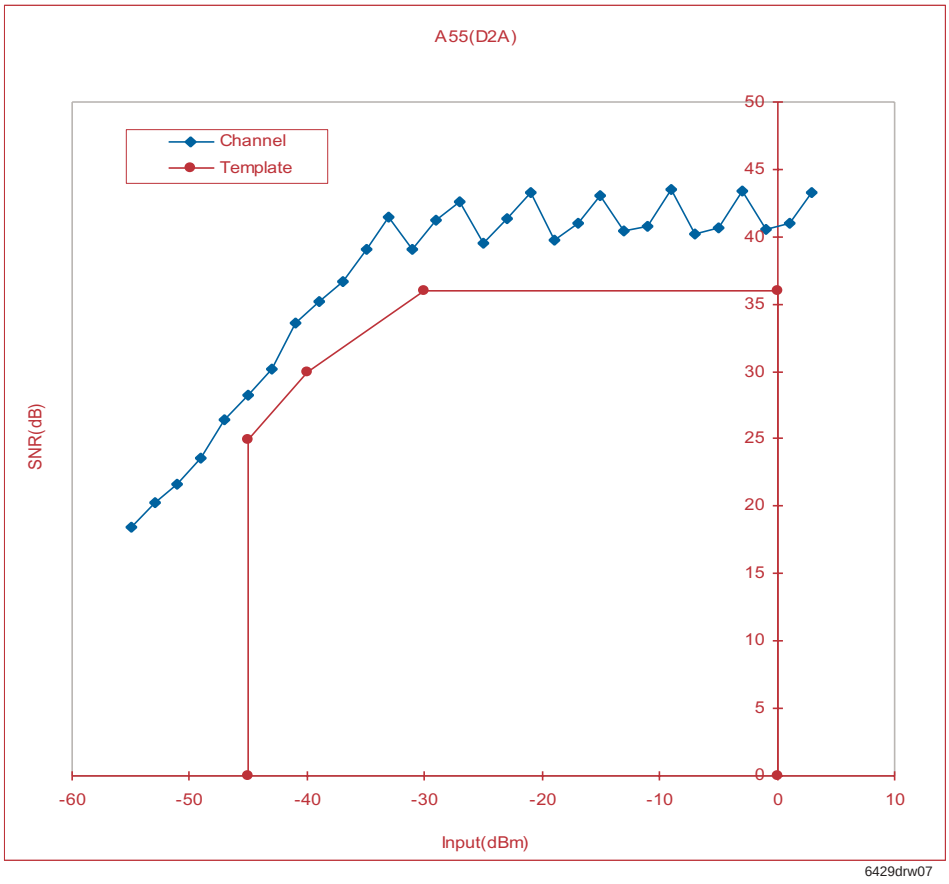
1. Select filter coefficients in the Coe-RAM by setting LREG1 to FFH;
2. Set the analog gain of A/D to 6 dB by setting the GAD bit in LREG9 to "1";
3. Set the analog gain of D/A to 0 dB by setting the GDA bit in LREG9 to "0".

Total Distortion - A55 (A2D)

(For 600W impedance, system target gain of A2D: 0dB; system target gain of D2A: -3.5dB)

Data

Level (dBm0)	Channel
-55	18.48
-53	20.32
-51	21.59
-49	23.62
-47	26.41
-45	28.21
-43	30.16
-41	33.6
-39	35.22
-37	36.72
-35	39.02
-33	41.41
-31	39.02
-29	41.19
-27	42.63
-25	39.47
-23	41.31
-21	43.28
-19	39.8
-17	41
-15	43.06
-13	40.41
-11	40.73
-9	43.56
-7	40.21
-5	40.63
-3	43.42
-1	40.51
1	41.04
3	43.3

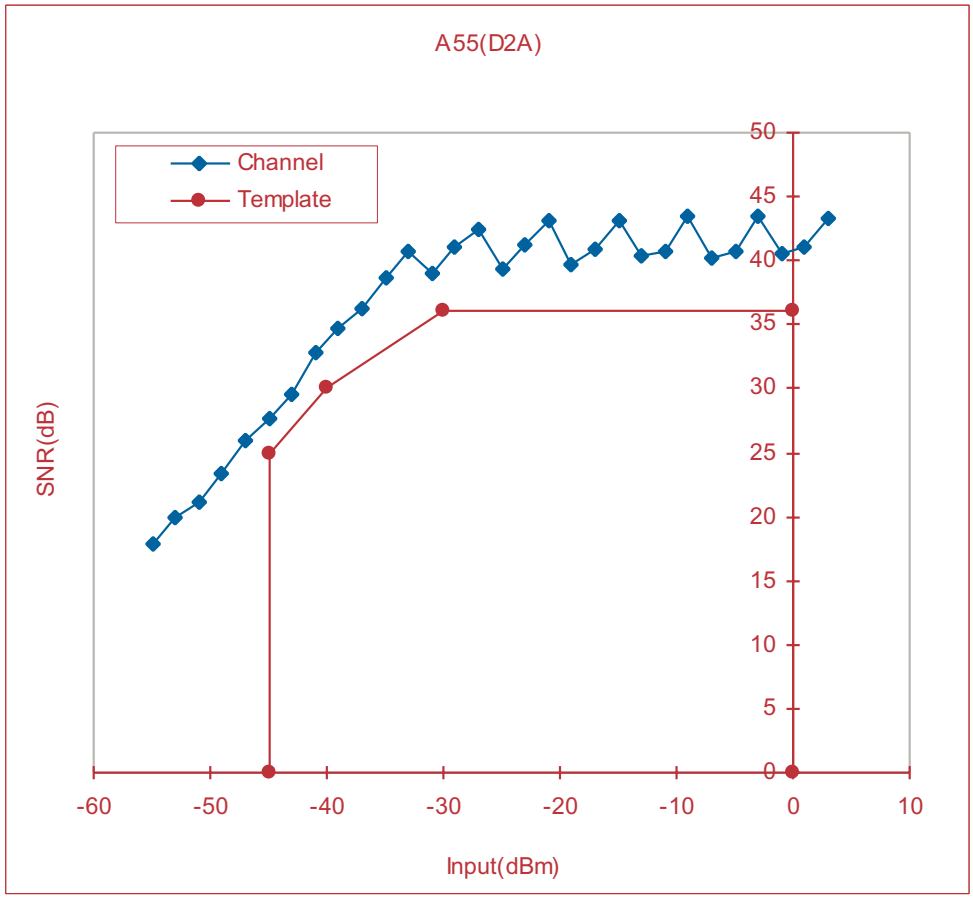


Total Distortion - A55 (D2A)

(For 600Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: -.3.5dB)

Data

Level (dBm0)	Channel
-55	17.88
-53	19.96
-51	21.1
-49	23.29
-47	25.86
-45	27.71
-43	29.54
-41	32.86
-39	34.63
-37	36.23
-35	38.6
-33	40.72
-31	38.95
-29	41.04
-27	42.49
-25	39.39
-23	41.24
-21	43.19
-19	39.77
-17	40.97
-15	43.05
-13	40.4
-11	40.73
-9	43.55
-7	40.21
-5	40.65
-3	43.41
-1	40.52
1	41.04
3	43.31



6429drw08

COEFFICIENTS IN DSP RAM 600Ω

The system target gain from tip / ring to digital port: 0 dB
The system target gain from digital port to tip / ring: -7 dB

Coefficients in the DSP Ram From low address to high address:

IMF Ram:	F5	01	C1	03	00	00	00	00	00	00	00	00	00	00	00	00
ECF Ram:	01	FA	0A	0B	00	00	00	00	00	00	65	53	4C	E1	00	00
GIS + Dual Tone Ram:	00	00	18	F4	00	00	00	00	00	00	00	00	00	00	00	00
FRX + GTX Ram:	6E	00	19	F3	31	20	31	20	19	F3	6E	00	99	31	E2	07
FRR + GRX Ram:	1C	01	04	00	28	3E	28	3E	04	00	1C	01	CE	84	24	1A

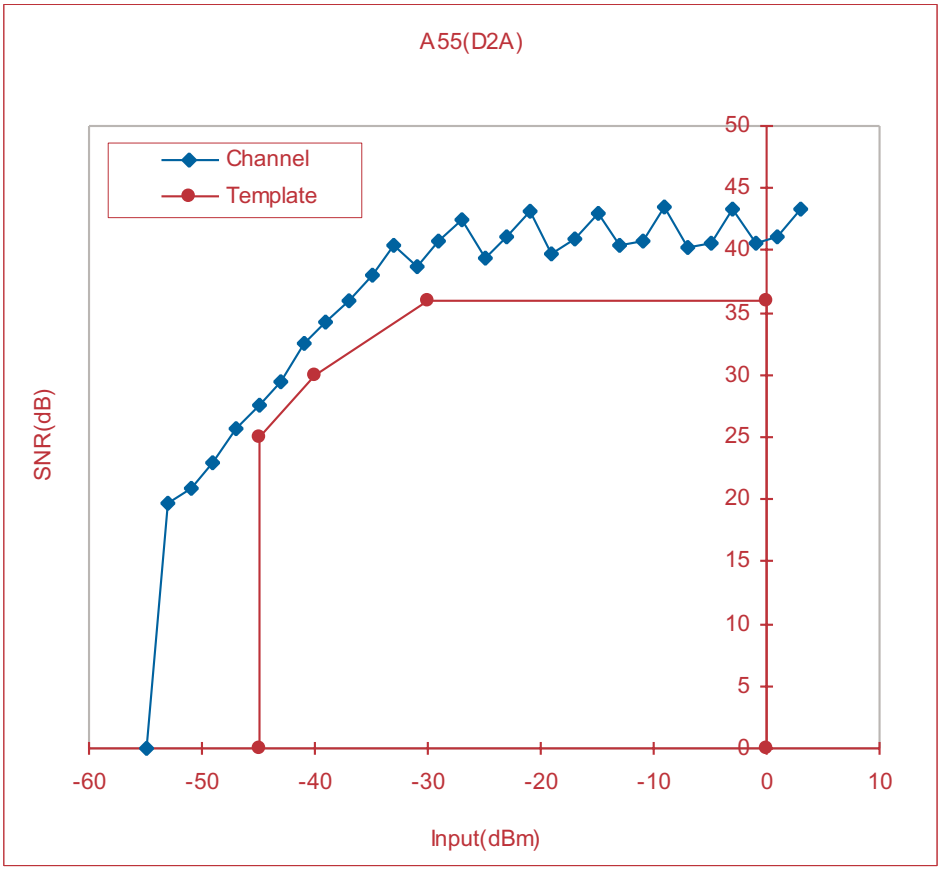
1. Select filter coefficients in the Coe-RAM by setting LREG1 to FFH;
2. Set the analog gain of A/D to 6 dB by setting the GAD bit in LREG9 to "1";
3. Set the analog gain of D/A to -6 dB by setting the GDA bit in LREG9 to "1".

Total Distortion - A55 (A2D)

(For 600Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: -7dB)

Data

Level (dBm0)	Channel
-55	19.64
-53	21.06
-51	21.85
-49	23.82
-47	27.16
-45	28.23
-43	30.36
-41	32.83
-39	34.55
-37	36.46
-35	38.87
-33	39.48
-31	38.92
-29	41.15
-27	42.11
-25	39.42
-23	41.23
-21	43.09
-19	39.92
-17	40.89
-15	43.19
-13	40.3
-11	40.8
-9	43.45
-7	40.39
-5	40.62
-3	43.42
-1	40.53
1	41.01
3	43.11

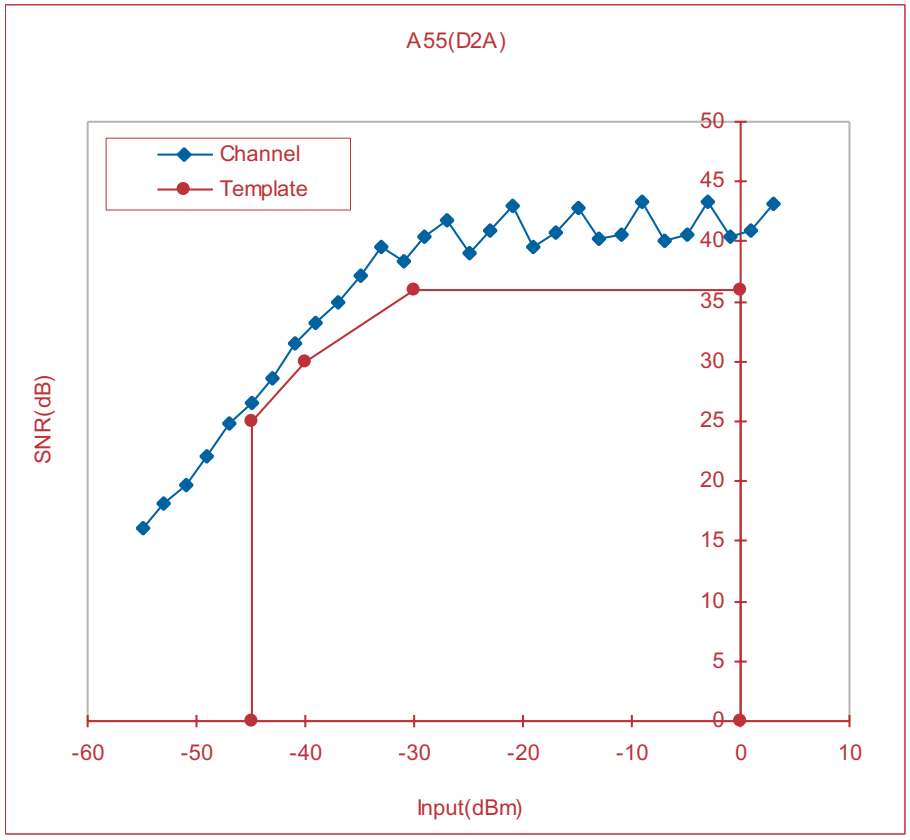


6429drw09

Total Distortion - A55 (D2A)

(For 600Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: -.7dB)

Data Level (dBm0)	Channel
-55	17.73
-53	19.67
-51	20.96
-49	23.01
-47	25.69
-45	27.52
-43	29.45
-41	32.56
-39	34.28
-37	36.02
-35	38.08
-33	40.33
-31	38.66
-29	40.79
-27	42.45
-25	39.30
-23	41.16
-21	43.17
-19	39.78
-17	40.94
-15	43.02
-13	40.37
-11	40.70
-9	43.52
-7	40.20
-5	40.63
-3	43.38
-1	40.50
1	41.02
3	43.28



6429drw10

COEFFICIENTS IN DSP RAM 900Ω

The system target gain from tip / ring to digital port: 0 dB
The system target gain from digital port to tip / ring: 0 dB

Coefficients in the DSP Ram From low address to high address:

IMF Ram:	0F	26	0F	EE	00	00	00	00	00	00	00	00	00	00	00	00
ECF Ram:	CE	F5	CC	11	00	00	00	00	00	00	80	53	F7	E0	00	00
GIS + Dual Tone Ram:	00	00	B8	A4	00	00	00	00	00	00	00	00	00	00	00	00
FRX + GTX Ram:	3E	FF	42	F2	04	1F	04	1F	42	F2	3E	FF	66	3E	95	0C
FRR + GRX Ram:	CD	01	33	F3	0F	22	0F	22	33	F3	CD	01	CD	24	E6	16

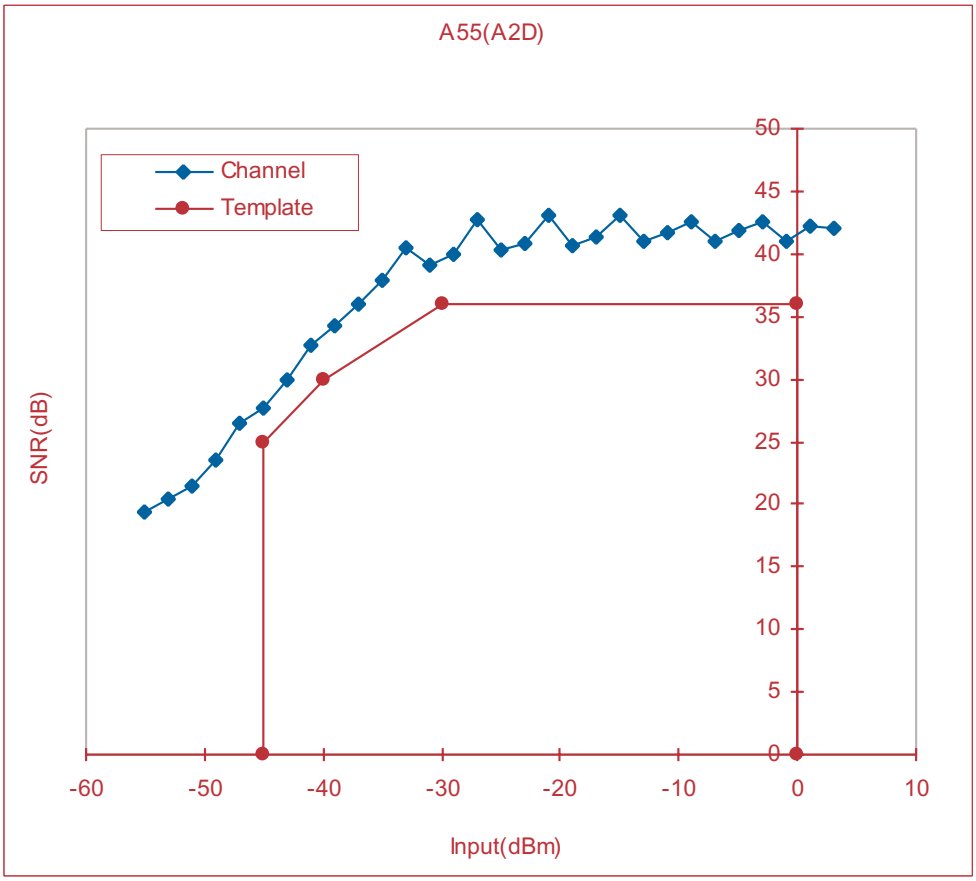
1. Select filter coefficients in the Coe-RAM by setting LREG1 to FFH;
2. Set the analog gain of A/D to 0 dB by setting the GAD bit in LREG9 to "0";
3. Set the analog gain of D/A to 0 dB by setting the GDA bit in LREG9 to "0".

Total Distortion - A55 (A2D)

(For 900Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: 0dB)

Data

Level (dBm0)	Channel
-55	19.44
-53	20.4
-51	21.52
-49	23.55
-47	26.48
-45	27.71
-43	29.85
-41	32.78
-39	34.21
-37	35.95
-35	37.97
-33	40.44
-31	39.11
-29	40.05
-27	42.77
-25	40.25
-23	40.82
-21	43.03
-19	40.7
-17	41.41
-15	43.02
-13	40.98
-11	41.74
-9	42.64
-7	41.01
-5	41.95
-3	42.54
-1	40.94
1	42.19
3	42.06



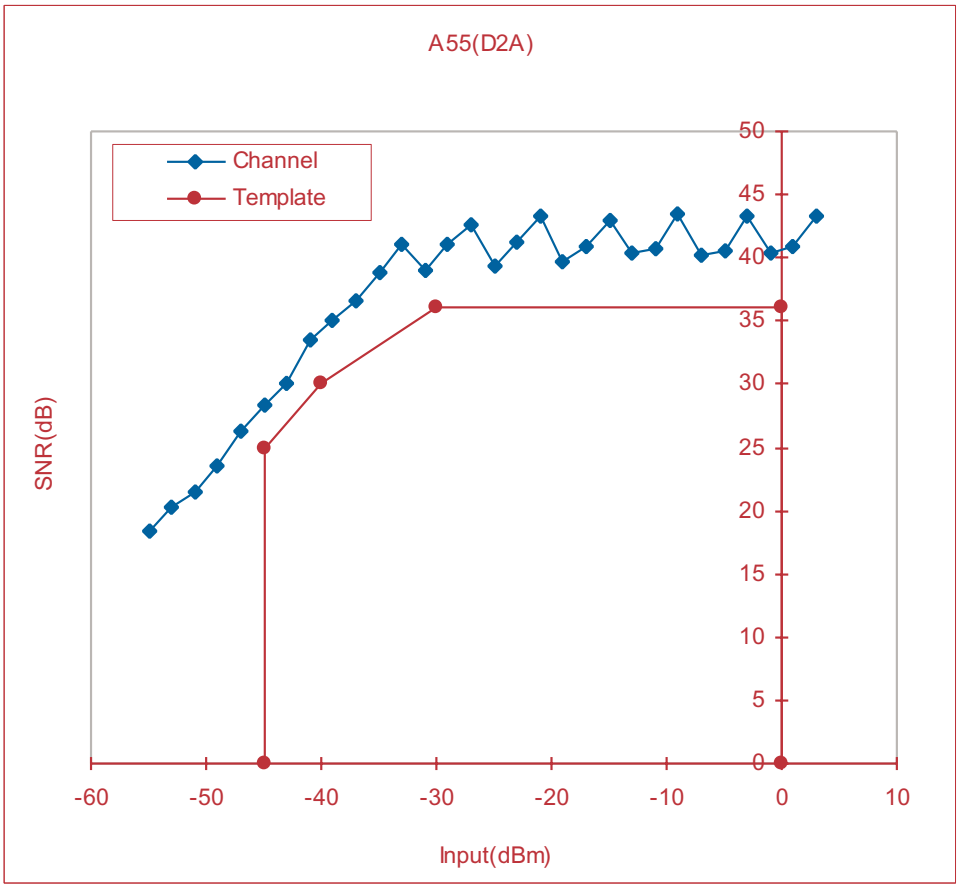
6429drw11

Total Distortion - A55 (D2A)

(For 900Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: 0dB)

Data

Level (dBm0)	Channel
-55	18.36
-53	20.19
-51	21.44
-49	23.49
-47	26.23
-45	28.29
-43	30.03
-41	33.47
-39	34.97
-37	35.58
-35	38.79
-33	41.14
-31	39.05
-29	41.14
-27	42.64
-25	39.4
-23	41.2
-21	43.22
-19	39.73
-17	40.92
-15	43
-13	40.32
-11	40.67
-9	43.49
-7	40.14
-5	41.58
-3	43.35
-1	40.46
1	40.97
3	42.23



6429drw12

COEFFICIENTS IN DSP RAM 900Ω

The system target gain from tip / ring to digital port: 0 dB
The system target gain from digital port to tip / ring: -3.5 dB

Coefficients in the DSP Ram From low address to high address:

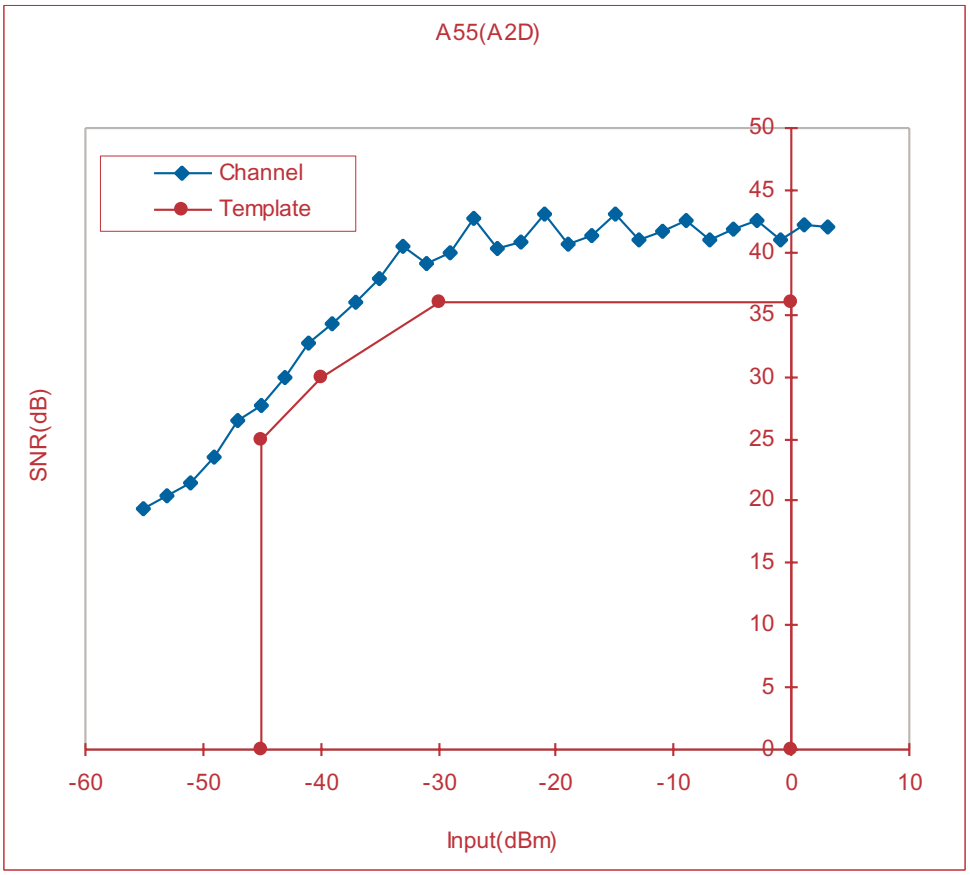
IMF Ram:	0F	26	0F	EE	00	00	00	00	00	00	00	00	00	00	00	00
ECF Ram:	CE	F5	CC	11	00	00	00	00	00	00	80	53	F7	E0	00	00
GIS + Dual Tone Ram:	00	00	B8	A4	00	00	00	00	00	00	00	00	00	00	00	00
FRX + GTX Ram:	3E	FF	42	F2	04	1F	04	1F	42	F2	3E	FF	66	3E	95	0C
FRR + GRX Ram:	CD	01	33	F3	0F	22	0F	22	33	F3	CD	01	CD	24	4E	0F

1. Select filter coefficients in the Coe-RAM by setting LREG1 to FFH;
2. Set the analog gain of A/D to 0 dB by setting the GAD bit in LREG9 to "0";
3. Set the analog gain of D/A to 0 dB by setting the GDA bit in LREG9 to "0".

Total Distortion - A55 (A2D)

(For 900Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: -3.5dB)

Data Level (dBm0)	Channel
-55	19.44
-53	20.4
-51	21.52
-49	23.55
-47	26.48
-45	27.71
-43	29.85
-41	32.78
-39	34.21
-37	35.95
-35	37.97
-33	40.44
-31	39.11
-29	40.05
-27	42.77
-25	40.25
-23	40.82
-21	43.03
-19	40.7
-17	41.41
-15	43.02
-13	40.98
-11	41.74
-9	42.64
-7	41.01
-5	41.95
-3	42.54
-1	40.94
1	42.19
3	42.06



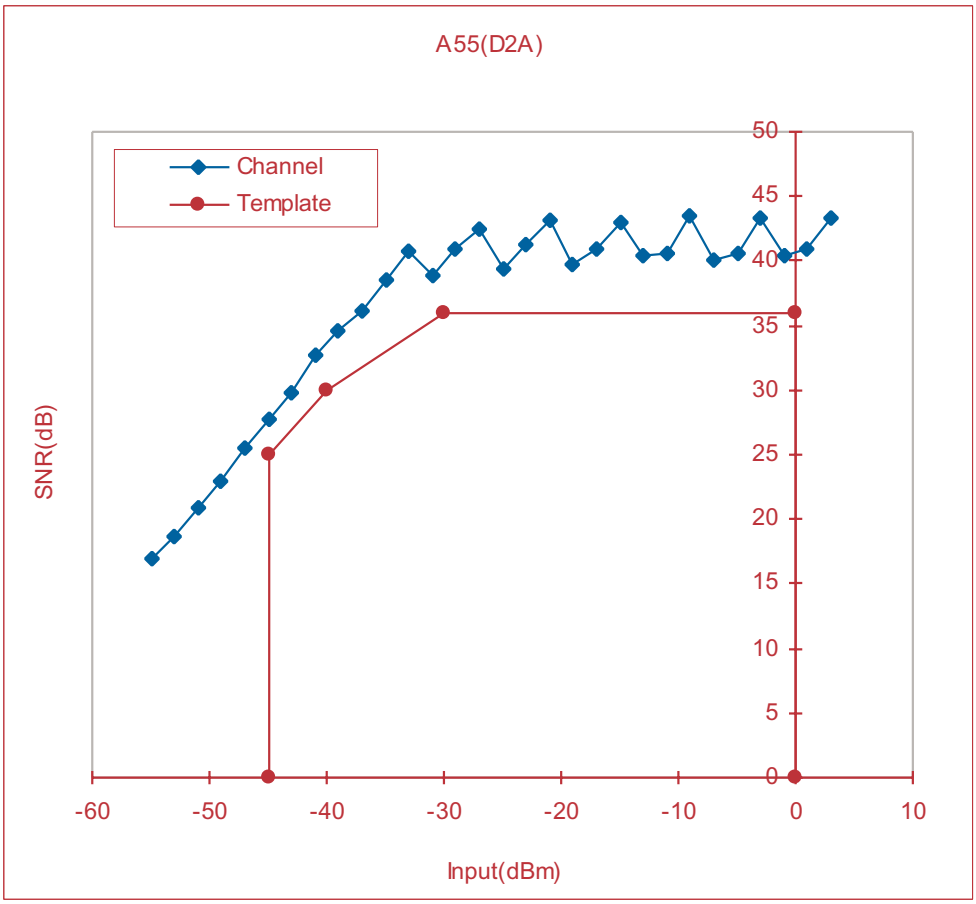
6429drw13

Total Distortion - A55 (D2A)

(For 900Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: -3.5dB)

Data

Level (dBm0)	Channel
-55	16.92
-53	18.65
-51	20.86
-49	22.92
-47	25.52
-45	27.73
-43	29.71
-41	32.65
-39	34.54
-37	36.05
-35	38.49
-33	40.68
-31	38.86
-29	40.91
-27	42.47
-25	39.34
-23	41.22
-21	43.19
-19	39.7
-17	40.93
-15	42.98
-13	40.34
-11	40.66
-9	43.5
-7	40.13
-5	40.59
-3	43.34
-1	40.47
1	40.99
3	43.24



6429drw14

COEFFICIENTS IN DSP RAM 900Ω

The system target gain from tip / ring to digital port: 0 dB
The system target gain from digital port to tip / ring: -7 dB

Coefficients in the DSP Ram From low address to high address:

IMF Ram:	0F	26	0F	EE	00	00	00	00	00	00	00	00	00	00	00	00
ECF Ram:	CE	F5	CC	11	00	00	00	00	00	00	80	53	F7	E0	00	00
GIS + Dual Tone Ram:	00	00	B8	A4	00	00	00	00	00	00	00	00	00	00	00	00
FRX + GTX Ram:	3E	FF	42	F2	04	1F	04	1F	42	F2	3E	FF	66	3E	57	06
FRR + GRX Ram:	CD	01	33	F3	0F	22	0F	22	33	F3	CD	01	CD	24	2D	14

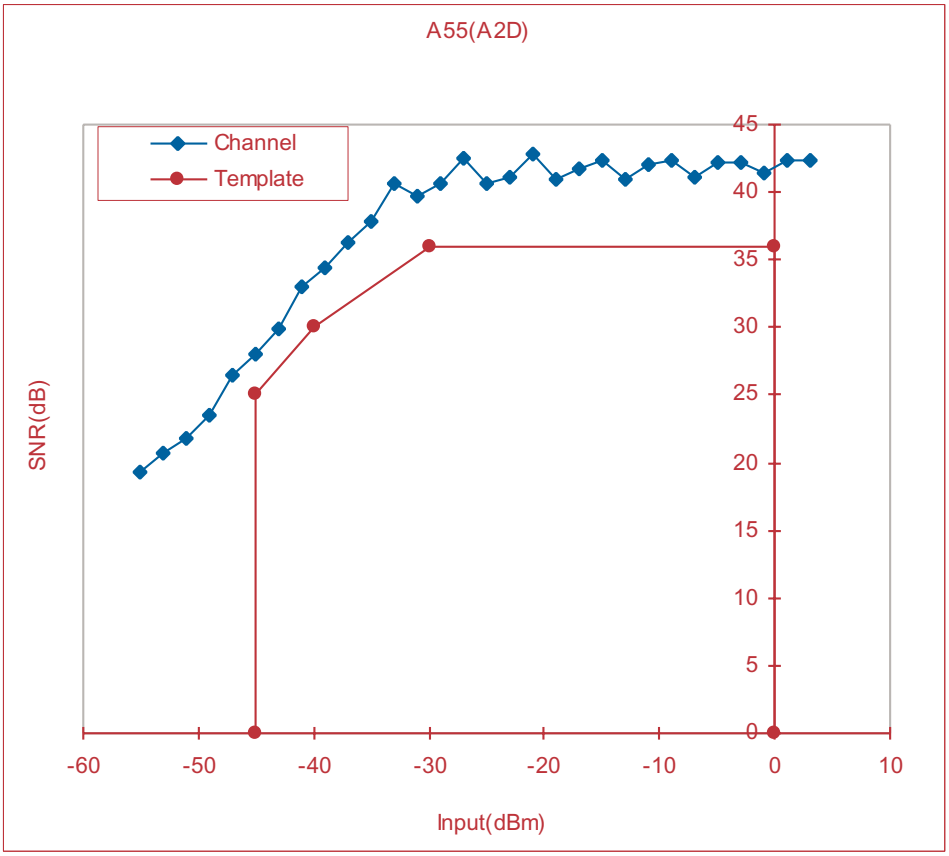
1. Select filter coefficients in the Coe-RAM by setting LREG1 to FFH;
2. Set the analog gain of A/D to 6 dB by setting the GAD bit in LREG9 to "1";
3. Set the analog gain of D/A to -6 dB by setting the GDA bit in LREG9 to "1".

Total Distortion - A55 (A2D)

(For 900Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: -7dB)

Data

Level (dBm0)	Channel
-55	19.3
-53	20.74
-51	21.77
-49	23.57
-47	26.45
-45	27.96
-43	29.89
-41	32.95
-39	34.38
-37	36.22
-35	37.89
-33	40.61
-31	39.71
-29	40.57
-27	42.46
-25	40.71
-23	41.18
-21	42.77
-19	41.02
-17	41.8
-15	42.37
-13	40.94
-11	42
-9	42.36
-7	41.04
-5	42.22
-3	42.27
-1	41.36
1	42.28
3	42.32



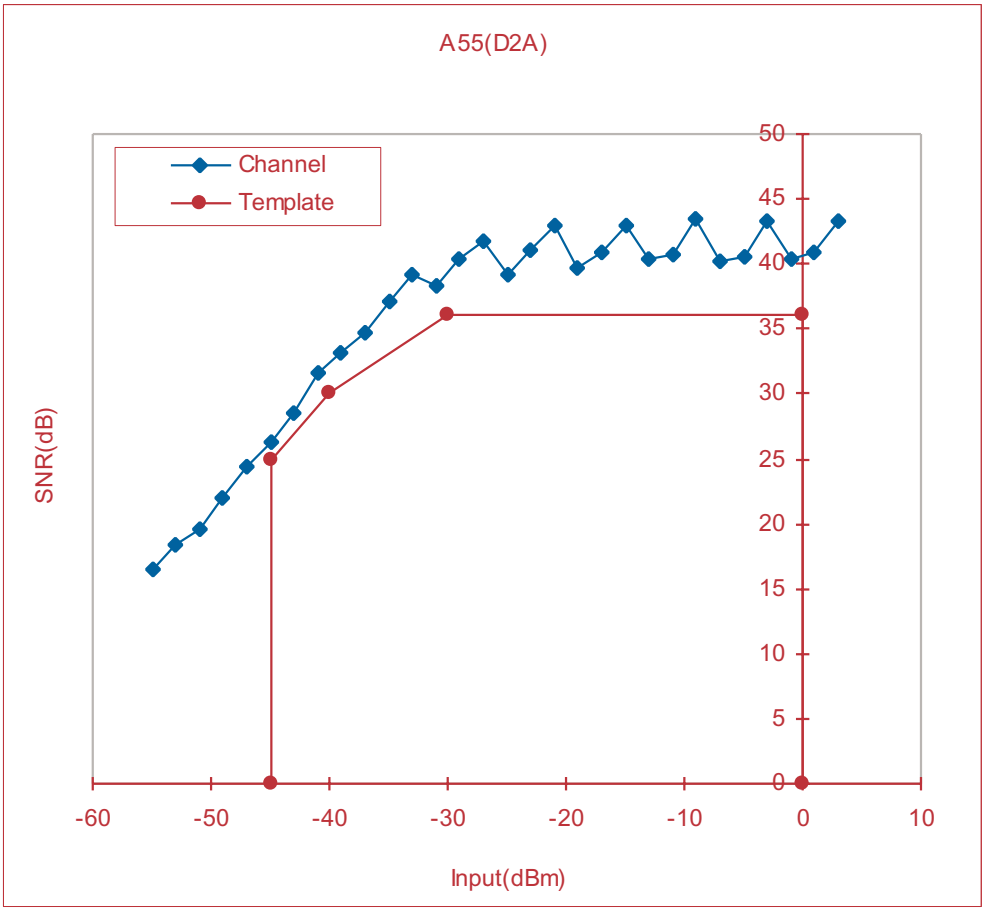
6429drw15

Total Distortion - A55 (D2A)

(For 900Ω impedance, system target gain of A2D: 0dB; system target gain of D2A: -7dB)

Data

Level (dBm0)	Channel
-55	16.51
-53	18.4
-51	19.66
-49	21.92
-47	24.36
-45	26.33
-43	28.59
-41	31.53
-39	33.11
-37	34.77
-35	37.05
-33	39.19
-31	38.24
-29	40.31
-27	41.79
-25	39.17
-23	41.01
-21	42.9
-19	39.65
-17	40.88
-15	42.92
-13	40.32
-11	40.65
-9	43.45
-7	40.14
-5	40.58
-3	43.34
-1	40.46
1	40.96
3	43.22



6429drw16

COEFFICIENTS IN DSP RAM (200Ω & 680 || Ω 0.1μF)

The system target gain from tip / ring to digital port: 0 dB
The system target gain from digital port to tip / ring: 0 dB

Coefficients in the DSP Ram From low address to high address:

IMF Ram:	B8	DC	AF	0D	00	00	00	00	00	00	00	00	00	00	00	00
ECF Ram:	DC	F6	94	10	00	00	00	00	00	00	3A	5B	BC	DF	00	00
GIS + Dual Tone Ram:	00	00	F4	07	00	00	00	00	00	00	00	00	00	00	00	00
FRX + GTX Ram:	51	01	9D	ED	57	27	57	27	9D	ED	51	01	99	31	F4	05
FRR + GRX Ram:	3C	05	19	D7	36	35	36	35	19	D7	3C	05	99	31	85	15

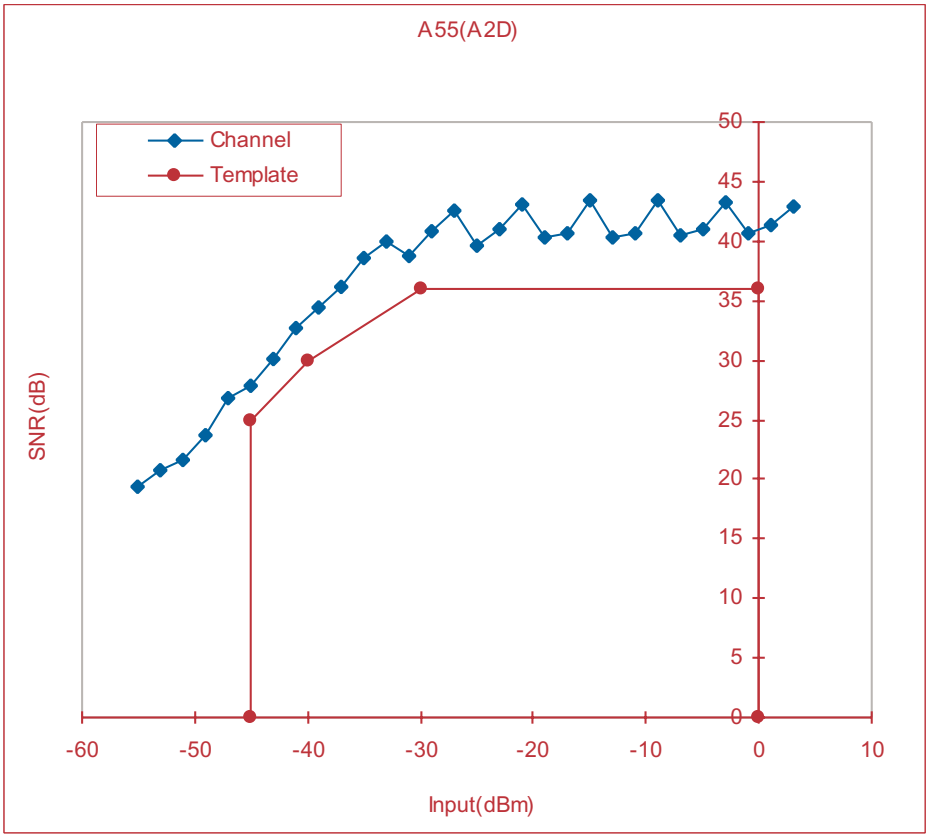
1. Select filter coefficients in the Coe-RAM by setting LREG1 to FFH;
2. Set the analog gain of A/D to 6 dB by setting the GAD bit in LREG9 to "1"'
3. Set the analog gain of D/A to 0 dB by setting the GDA bit in LREG9 to "0".

Total Distortion - A55 (A2D)

(For China complex impedance, system target: gain of A2D is 0dB; gain of D2A is 0dB)

Data

Level (dBm0)	Channel
-55	19.44
-53	20.83
-51	21.63
-49	23.69
-47	26.88
-45	27.93
-43	30.13
-41	32.72
-39	34.36
-37	36.14
-35	38.63
-33	39.94
-31	38.77
-29	40.85
-27	42.52
-25	39.67
-23	40.93
-21	43.05
-19	40.26
-17	40.66
-15	43.42
-13	40.37
-11	40.61
-9	43.48
-7	40.52
-5	40.97
-3	43.19
-1	40.71
1	41.32
3	42.98



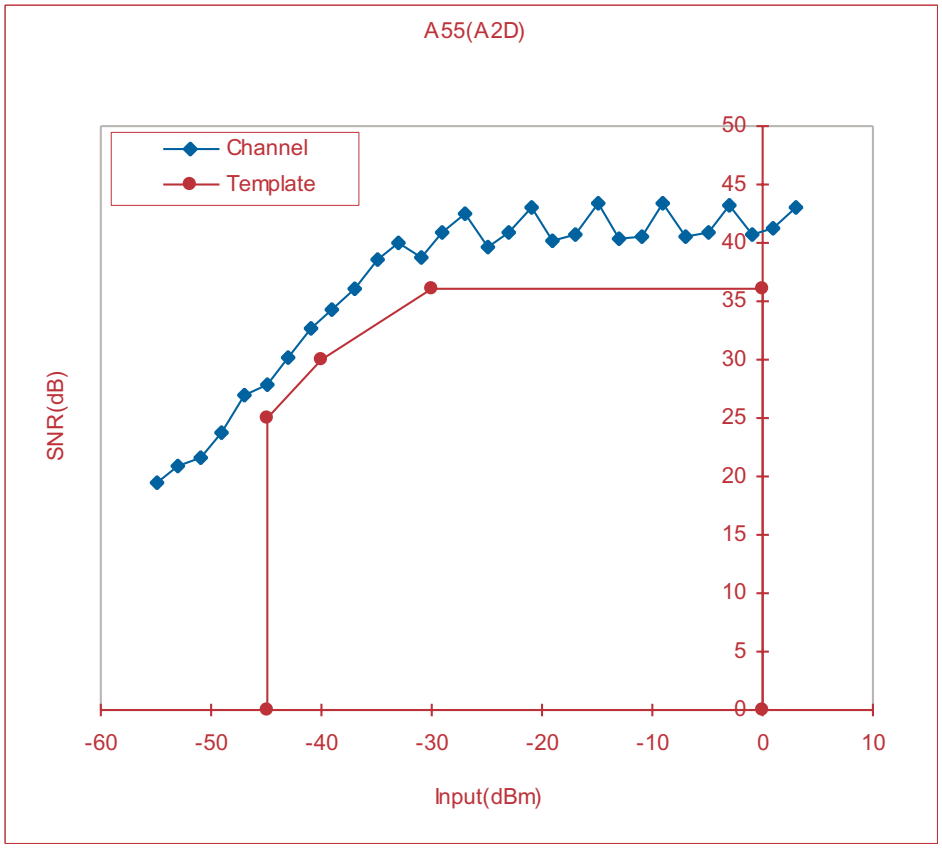
6429drw17

Total Distortion - A55 (D2A)

(For China complex impedance, system target: gain of A2D is 0dB; gain of D2A is 0dB)

Data

Level (dBm0)	Channel
-55	18.3
-53	20.02
-51	21.38
-49	23.48
-47	26.23
-45	28.04
-43	29.93
-41	33.32
-39	34.82
-37	36.48
-35	38.73
-33	41.03
-31	38.99
-29	41.14
-27	42.55
-25	39.3
-23	41.18
-21	43.14
-19	39.67
-17	40.86
-15	42.93
-13	40.27
-11	40.61
-9	43.42
-7	40.08
-5	40.51
-3	43.28
-1	40.4
1	40.89
3	43.15



6429drw18

COEFFICIENTS IN DSP RAM (200Ω &680Ω || 0.1μF)

The system target gain from tip / ring to digital port: 0 dB
The system target gain from digital port to tip / ring: -3.5 dB

Coefficients in the DSP Ram From low address to high address:

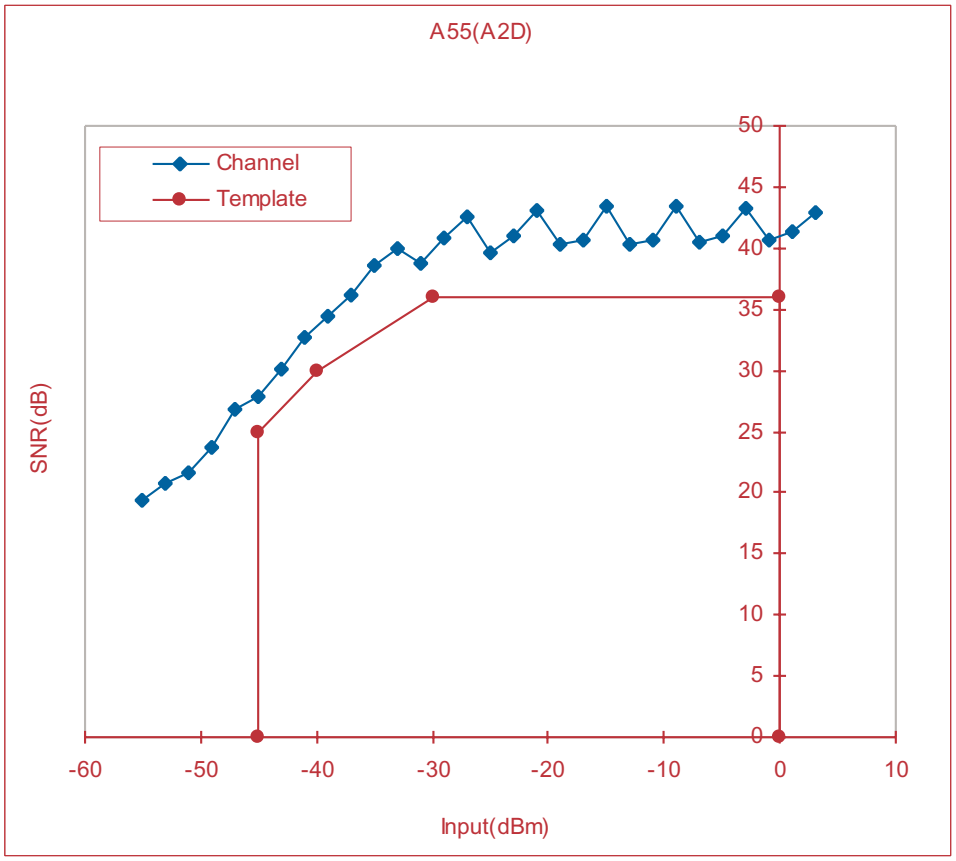
IMF Ram:	B8	DC	AF	0D	00	00	00	00	00	00	00	00	00	00	00	00
ECF Ram:	DC	F6	94	10	00	00	00	00	00	00	3A	5B	BC	DF	00	00
GIS + Dual Tone Ram:	00	00	F4	07	00	00	00	00	00	00	00	00	00	00	00	00
FRX + GTX Ram:	51	01	9D	ED	57	24	57	24	9D	ED	51	01	99	31	F4	05
FRR + GRX Ram:	3C	05	19	D7	36	35	36	35	19	D7	3C	05	99	31	62	0E

1. Select filter coefficients in the Coe-RAM by setting LREG1 to FFH;
2. Set the analog gain of A/D to 6 dB by setting the GAD bit in LREG9 to "1";
3. Set the analog gain of D/A to 0 dB by setting the GDA bit in LREG9 to "0".

Total Distortion - A55 (A2D)

(For China complex impedance, system target: gain of A2D is 0dB; gain of D2A is -3.5dB)

Data Level (dBm0)	Channel
-55	19.44
-53	20.83
-51	21.63
-49	23.69
-47	26.88
-45	27.93
-43	30.13
-41	32.72
-39	34.36
-37	36.14
-35	38.63
-33	39.94
-31	38.77
-29	40.85
-27	42.52
-25	39.67
-23	40.93
-21	43.05
-19	40.26
-17	40.66
-15	43.42
-13	40.37
-11	40.61
-9	43.78
-7	40.52
-5	40.97
-3	43.19
-1	40.71
1	41.32
3	42.98

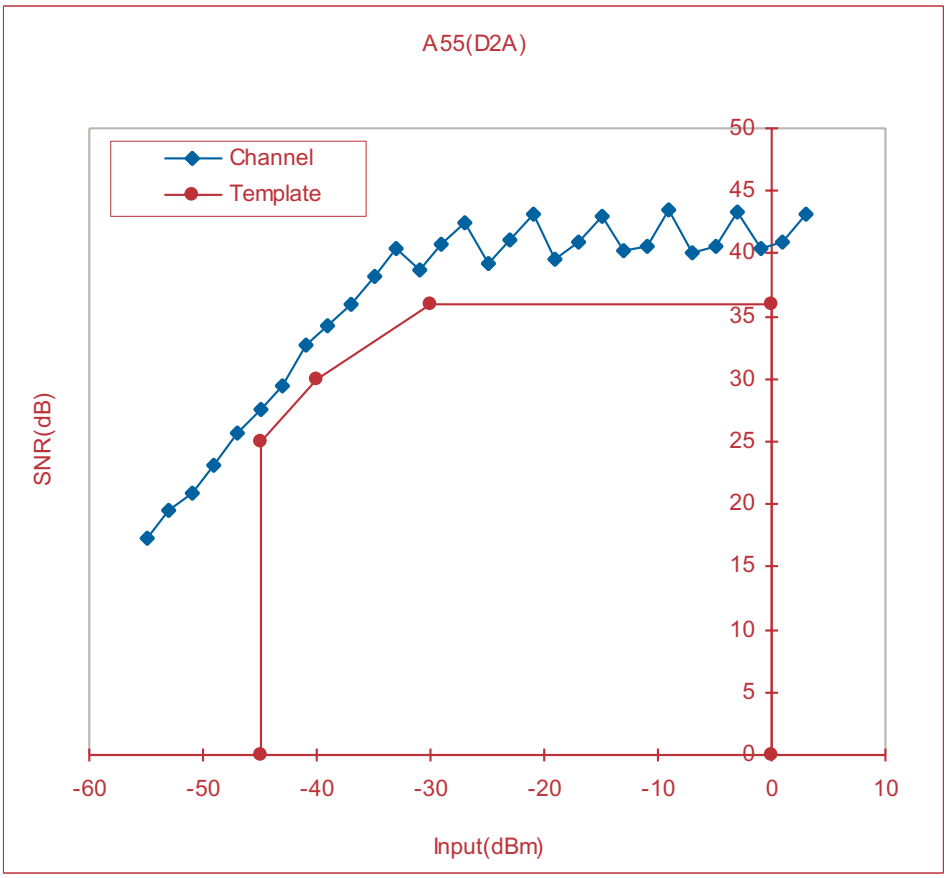


6429drw19

Total Distortion - A55 (D2A)

(For China complex impedance, system target: gain of A2D is 0dB; gain of D2A is -3.5dB)

Data Level (dBm0)	Channel
-55	17.35
-53	19.57
-51	20.85
-49	23.05
-47	25.74
-45	27.62
-43	29.37
-41	32.7
-39	34.2
-37	35.93
-35	38.21
-33	40.41
-31	38.73
-29	40.81
-27	42.39
-25	39.2
-23	41.11
-21	43.07
-19	39.64
-17	40.85
-15	42.92
-13	40.26
-11	40.6
-9	43.42
-7	40.08
-5	40.51
-3	43.28
-1	40.4
1	40.89
3	43.16



6429drw20

COEFFICIENTS IN DSP RAM (200Ω & 680Ω || 0.1μF)

The system target gain from tip / ring to digital port: 0 dB
The system target gain from digital port to tip / ring: -7 dB

Coefficients in the DSP Ram From low address to high address:

IMF Ram:	B8	DC	AF	0D	00	00	00	00	00	00	00	00	00	00	00	00
ECF Ram:	DC	F6	94	10	00	00	00	00	00	00	3A	5B	BC	DF	00	00
GIS + Dual Tone Ram:	00	00	F4	07	00	00	00	00	00	00	00	00	00	00	00	00
FRX + GTX Ram:	51	01	9D	ED	57	24	57	24	9D	ED	51	01	99	31	F4	05
FRR + GRX Ram:	3C	05	19	D7	36	35	36	35	19	D7	3C	05	99	31	97	09

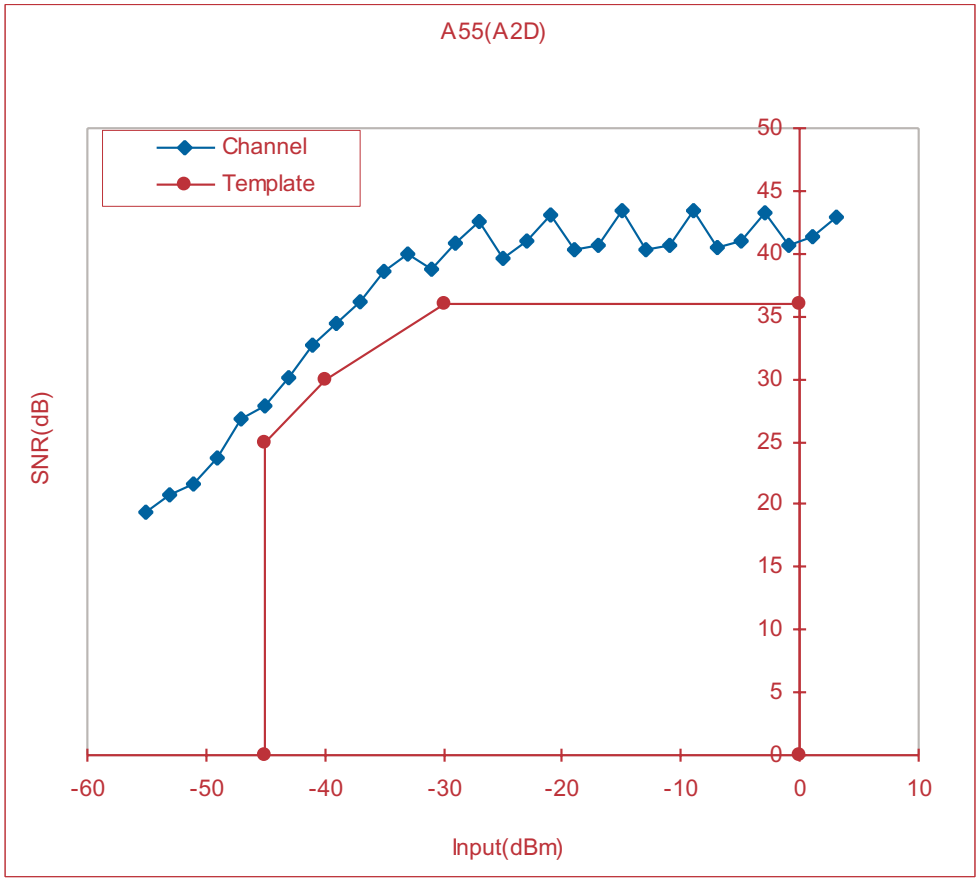
1. Select filter coefficients in the Coe-RAM by setting LREG1 to FFH;
2. Set the analog gain of A/D to 6 dB by setting the GAD bit in LREG9 to "1";
3. Set the analog gain of D/A to 0 dB by setting the GDA bit in LREG9 to "0".

Total Distortion - A55 (A2D)

(For China complex impedance, system target: gain of A2D is 0dB; gain of D2A is -7dB)

Data

Level (dBm0)	Channel
-55	19.44
-53	20.83
-51	21.63
-49	23.69
-47	26.88
-45	27.93
-43	30.13
-41	32.72
-39	34.36
-37	36.14
-35	38.63
-33	39.94
-31	38.77
-29	40.85
-27	42.52
-25	39.67
-23	40.93
-21	43.05
-19	40.26
-17	40.66
-15	43.42
-13	40.37
-11	40..61
-9	43.48
-7	40.52
-5	40.97
-3	43.19
-1	40.71
1	41.32
3	42.98



6429drw21

Total Distortion - A55 (D2A)

(For China complex impedance, system target: gain of A2D is 0dB; gain of D2A is -7dB)

Data Level (dBm0)	Channel
-55	16.14
-53	18.21
-51	19.61
-49	22.09
-47	24.79
-45	26.56
-43	28.68
-41	31.55
-39	33.26
-37	34.86
-35	37.12
-33	39.53
-31	38.31
-29	40.33
-27	41.85
-25	39.07
-23	40.92
-21	42.9
-19	39.64
-17	40.8
-15	42.86
-13	40.25
-11	40.59
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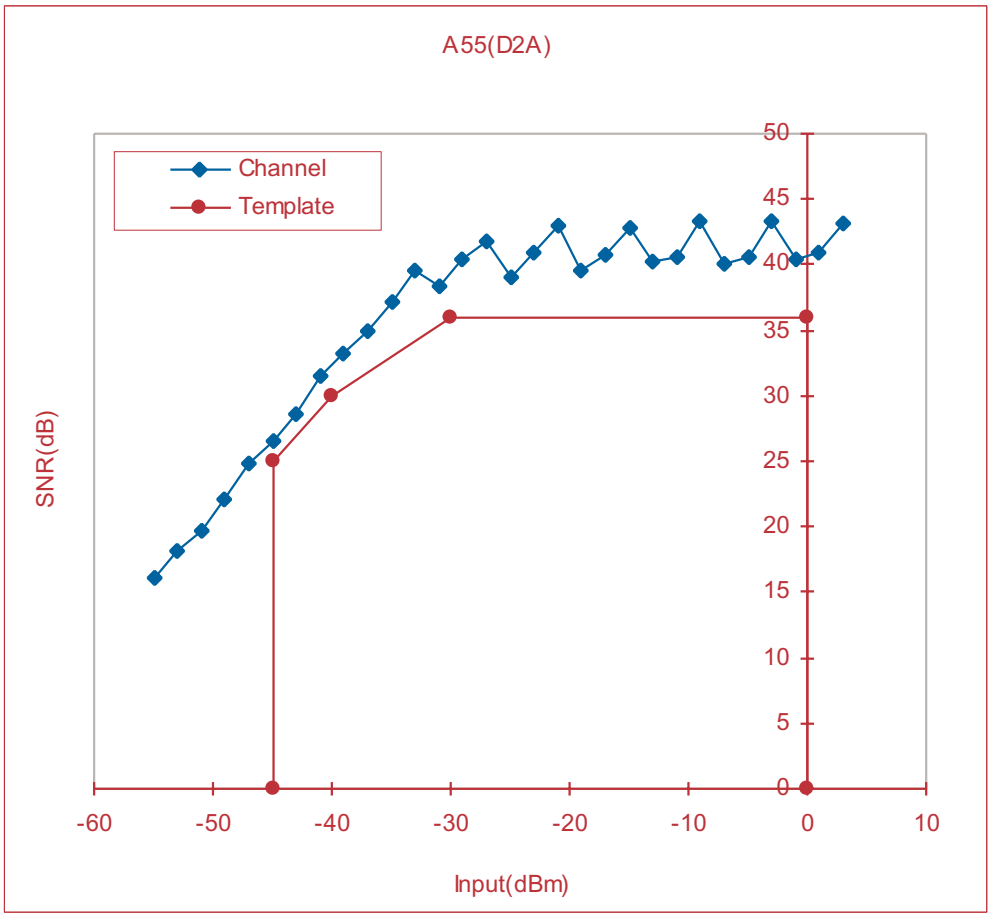
-3	43.27
-1	40.39
1	40.89
3	43.16



6429drw22

Document History

9/27/2004 pgs. 8, 11, 14, 17, 20, 26, 29, 32

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