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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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38D2 Group

Serial I/O 1, 2 (Clock Synchronous Serial I/O Mode: Example 1)

1. Abstract

The following article introduces and shows an example of how to use the Serial I/O 1, 2 (Clock Synchronous Serial I/O Mode: Example 1) on the 38D2 Group device.

2. Introduction

The application explained in this document applies to the following MCU and parameter(s):

Applicable MCU: 38D2 Group

Oscillation frequency: 4 MHz

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

3. Contents

3.1 Communication Using Clock Synchronous Serial I/O (Transmit/Receive)

Outline: 2-byte data is transmitted and received, using the clock synchronous serial I/O.
 $\overline{\text{SRDY}}$ signal is used for communication control.

Specifications:

- Serial I/O is used (clock synchronous serial I/O mode is selected).
- Synchronous clock frequency: 125 kHz ($f(\text{XIN}) = 4 \text{ MHz}$ divided by 32)
- $\overline{\text{SRDY}}$ signal (receivable signal) is used.
- The receive side outputs the $\overline{\text{SRDY}}$ signal at intervals of 2 ms (generated by the timer), and 2-byte data is received.
- The transmit side confirms the $\overline{\text{SRDY}}$ signal by INT1 interrupt request and transmits 2-byte data.

Figure 3.1 shows the Connection Diagram, Figure 3.2 shows the Timing Chart, Figure 3.3 shows the Register Settings Relevant to the Transmit Side, Figure 3.4 shows the Register Settings Relevant to the Receive Side, Figure 3.5 shows the Control Procedure of Transmit Side, and Figure 3.6 shows the Control Procedure of Receive Side.

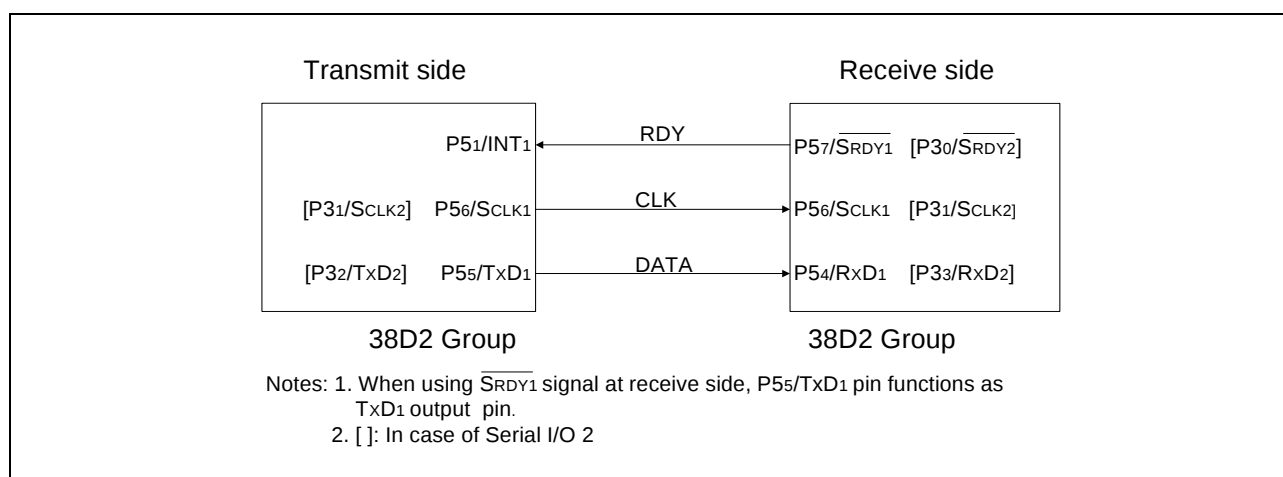


Figure 3.1 Connection Diagram

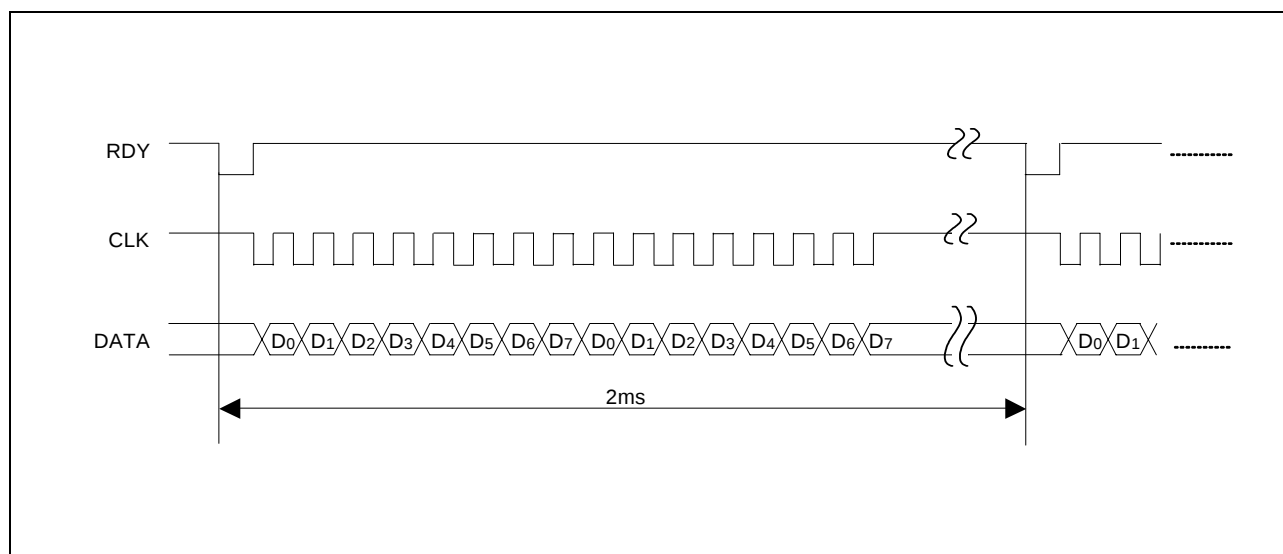
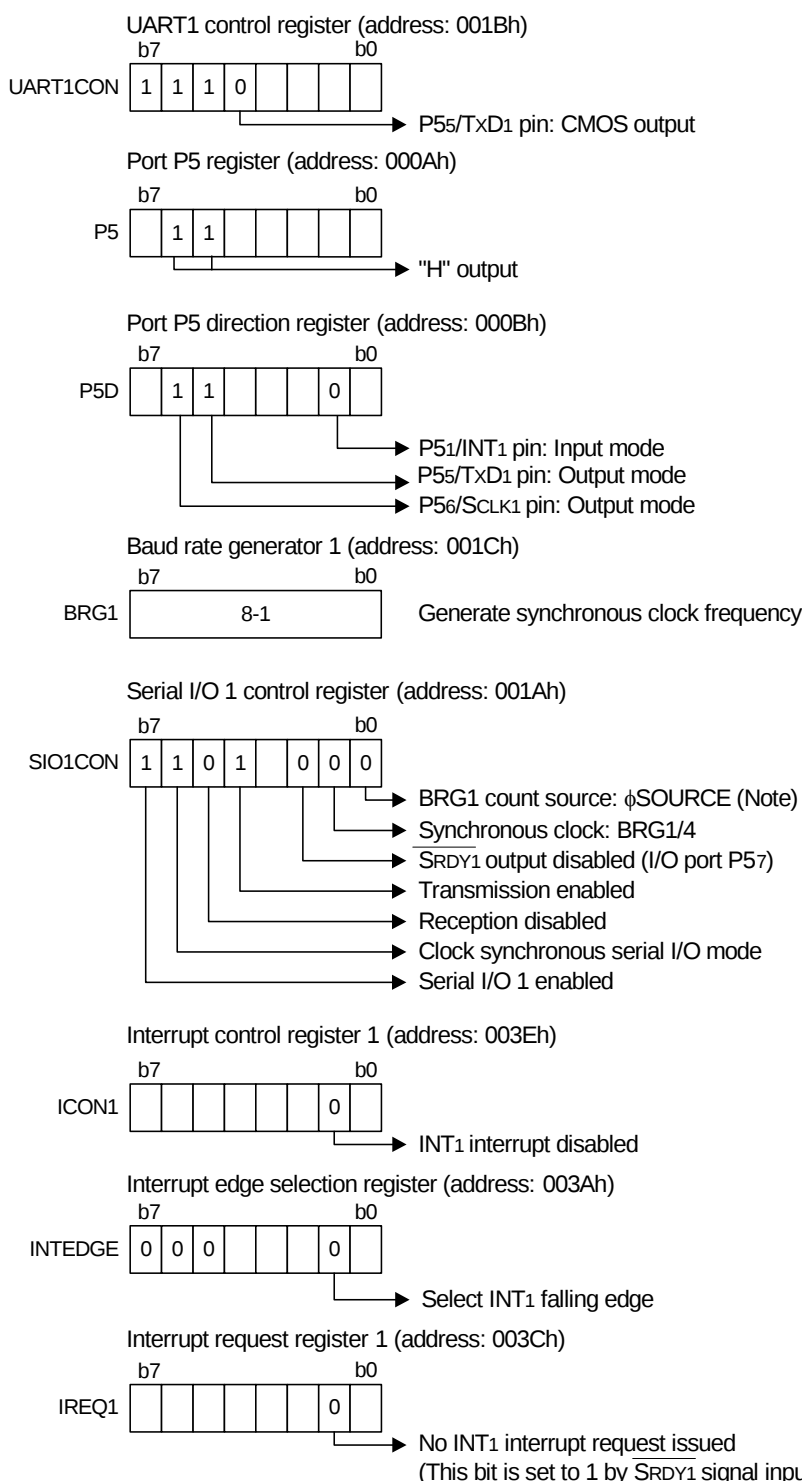


Figure 3.2 Timing Chart

Transmit Side



Note: ϕ SOURCE = XIN input in frequency/2, 4, 8 mode, on-chip oscillator divided by 4 in on-chip oscillator mode, and oscillation frequency of sub-clock in low-speed mode

[Serial I/O 2]

UART2 control register (address: 00FFh)

Port P3 register (address: 0006h)

Port P3 direction register (address: 0007h)
 P32/TxD2 pin
 P31/SCLK2 pin

Port P5 direction register (address: 000Bh)
 P51/INT1 pin

Baud rate generator 2 (address: 0FF2h)

Serial I/O 2 control register (address: 001Fh)

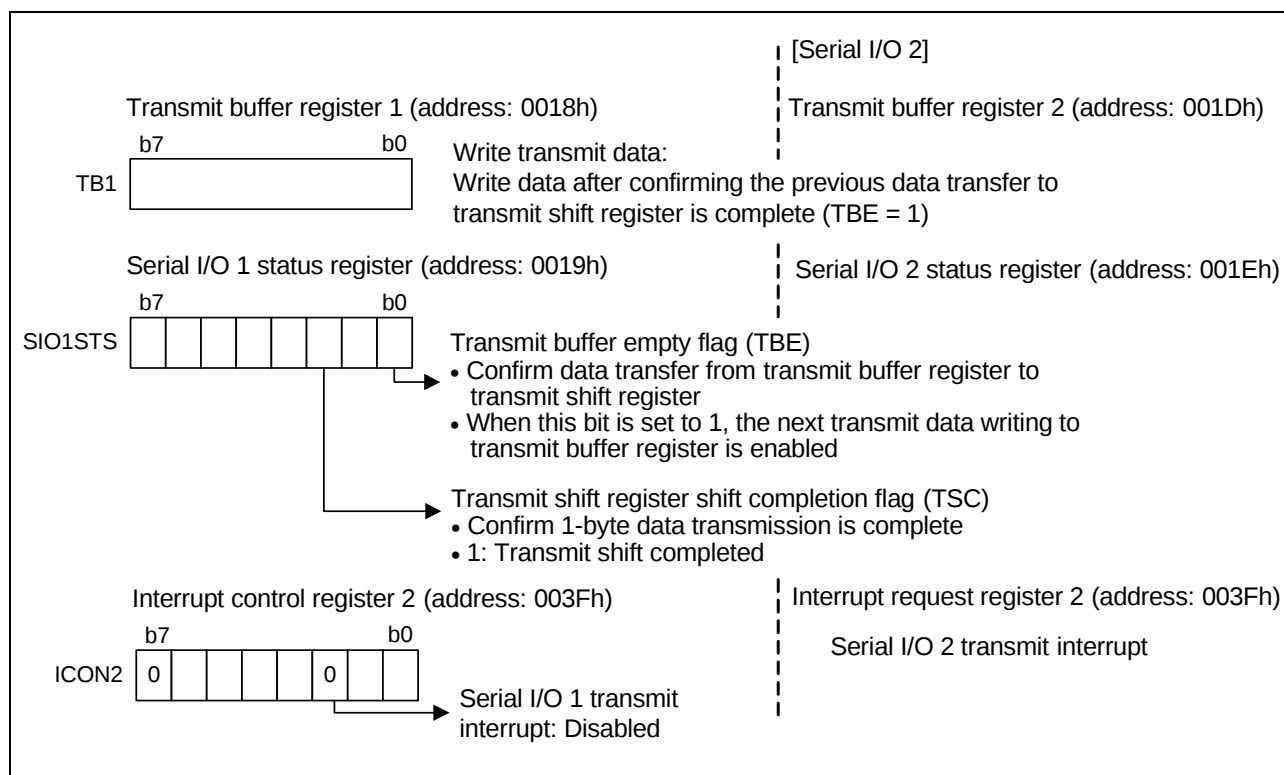


Figure 3.3 Register Settings Relevant to the Transmit Side

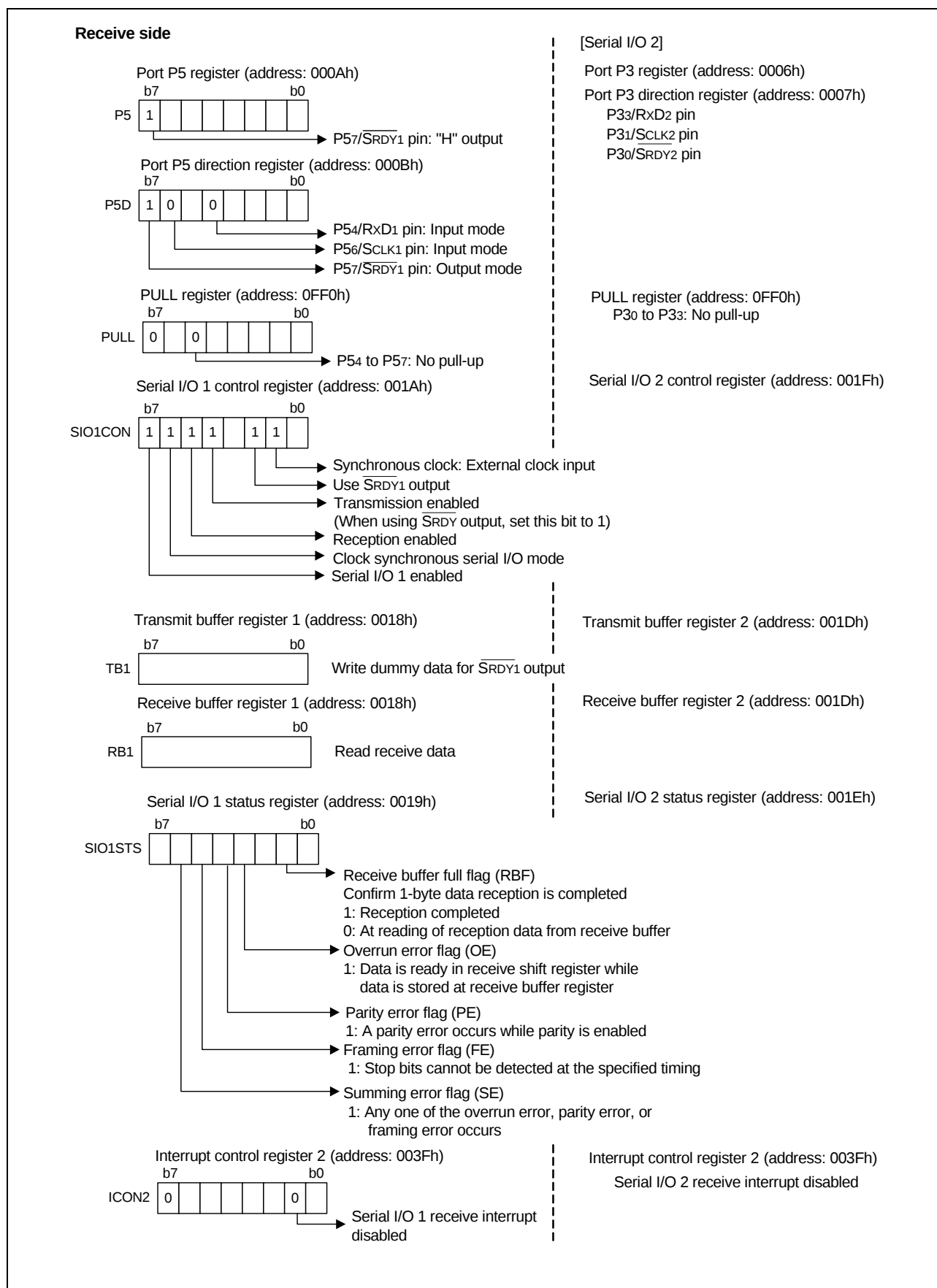


Figure 3.4 Register Settings Relevant to the Receive Side

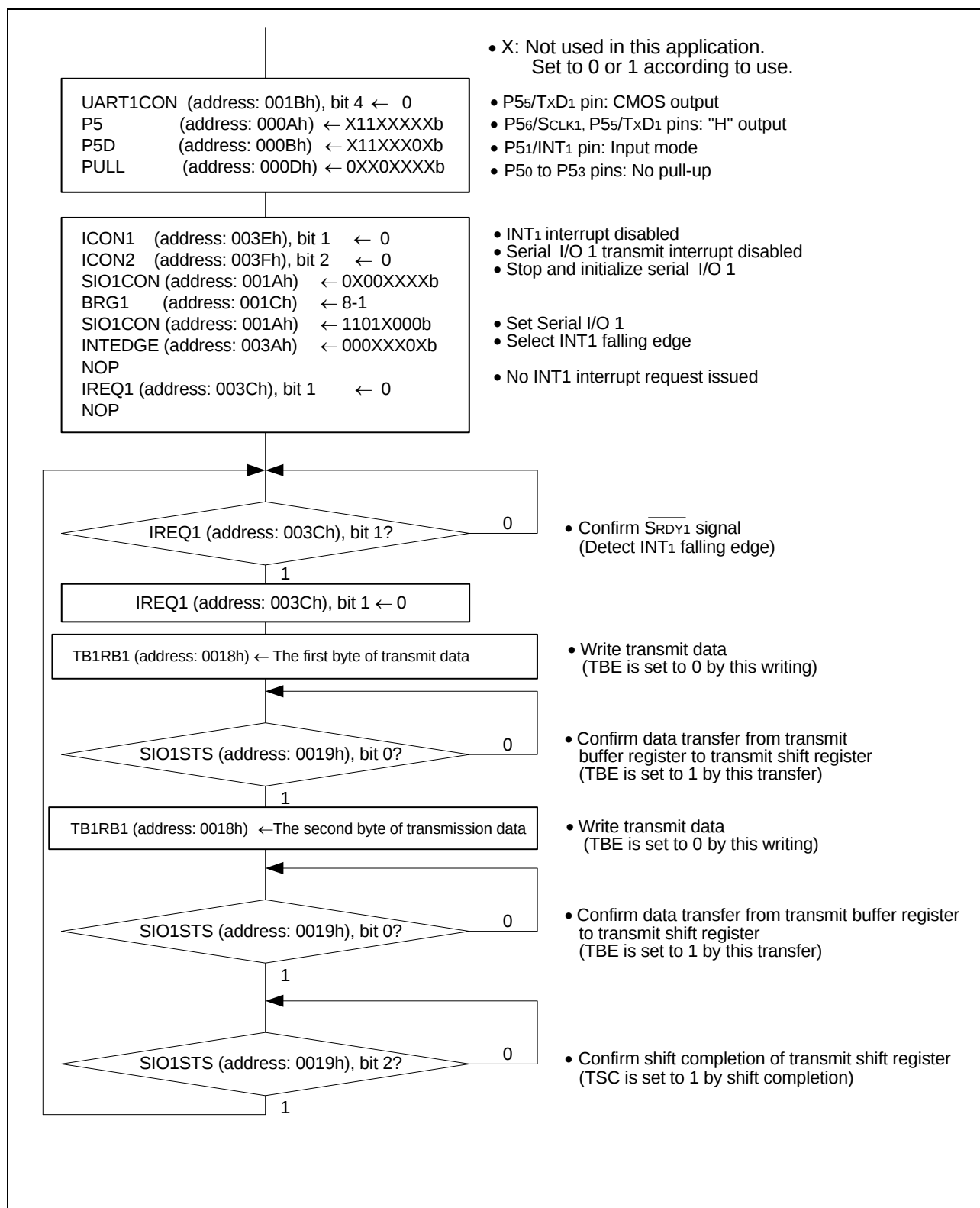


Figure 3.5 Control Procedure of Transmit Side

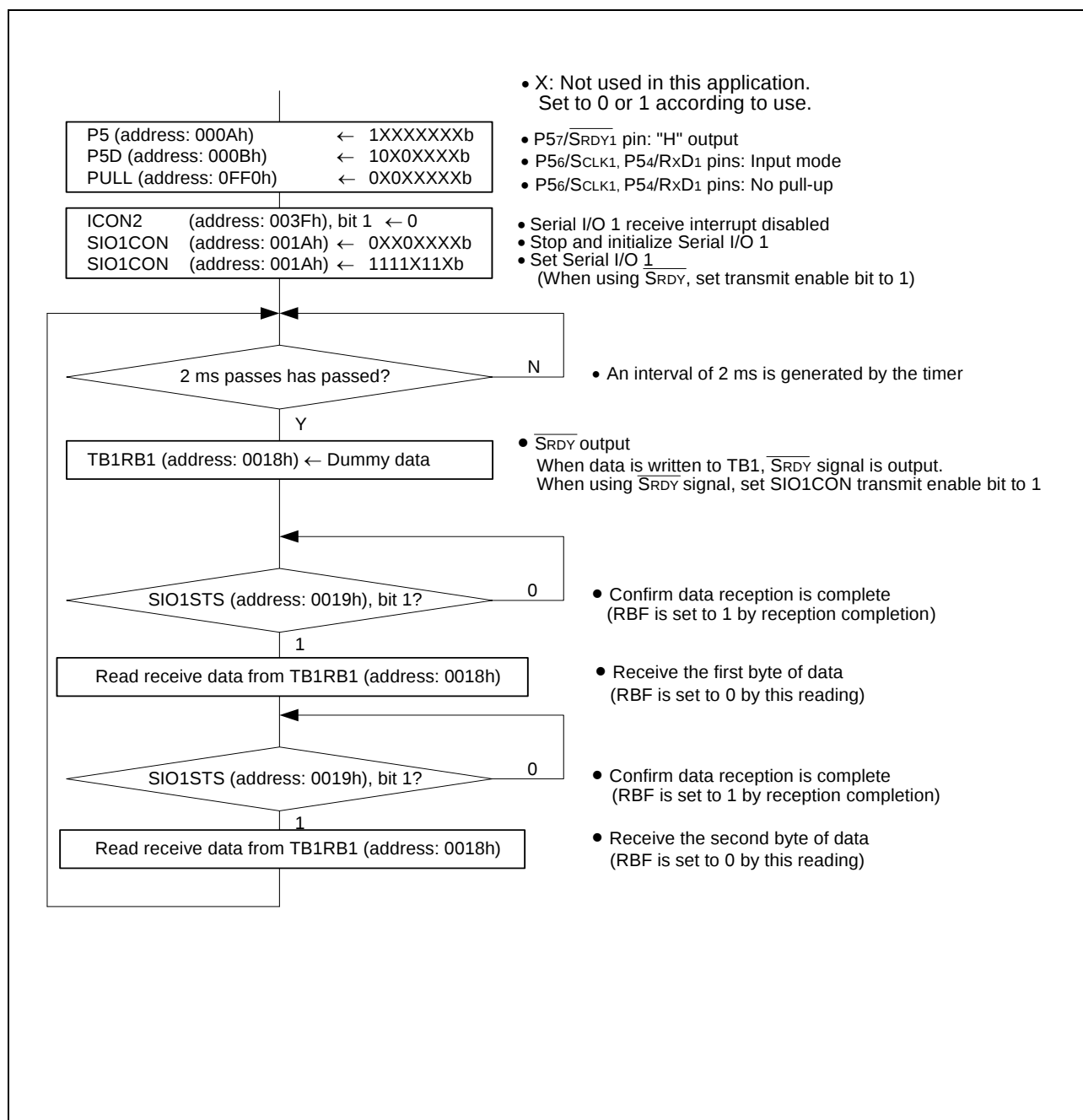


Figure 3.6 Control Procedure of Receive Side

4. Sample Programming Code

Download a sample program from the Renesas Technology website.

To download, click “Application Notes” in the left side menu on the page of the 38D2 Group.

5. Reference Document

Datasheet

38D2 Group Datasheet

Download the latest version from the Renesas Technology website.

Technical News/Technical Update

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Website and Support

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REVISION HISTORY	38D2 Group Serial I/O 1, 2 (Clock Synchronous Serial I/O Mode: Example 1)
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 9, 2007	–	First Edition issued

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