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3858 Group
List of Registers

1. Abstract

This document describes the 3858 Group registers.

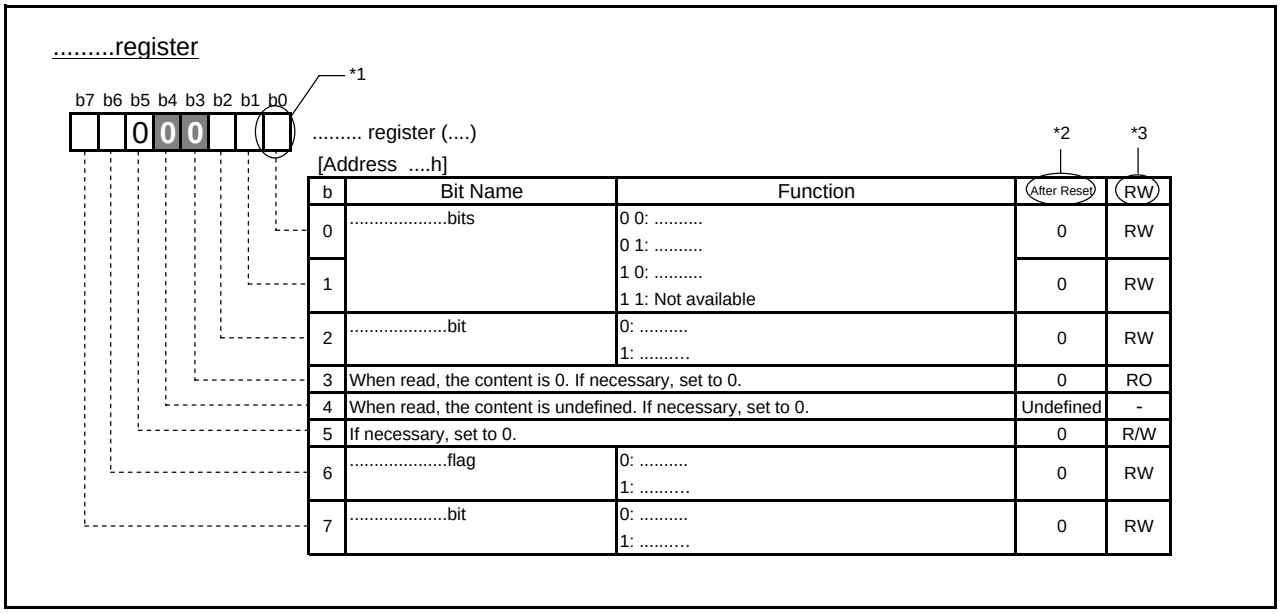
2. Introduction

The registers described in this document apply to the following:

MCU: 3858 Group

3. Structure of Register

The following shows an example of a control register structure diagram in this application note and the definitions of the symbols and terms used in the diagram.



b	Bit Name	Function	After Reset	RW
0	.....bits	0 0: ..... 0 1: ..... 1 0: ..... 1 1: Not available	0	RW
1			0	RW
2	.....bit	0: 1:	0	RW
3	When read, the content is 0. If necessary, set to 0.		0	RO
4	When read, the content is undefined. If necessary, set to 0.		Undefined	-
5	If necessary, set to 0.		0	R/W
6	.....flag	0: 1:	0	RW
7	.....bit	0: 1:	0	RW

*1

Blank	: Set to 0 or 1 according to the application.
0	: If necessary, set to 0.
1	: If necessary, set to 1.
×	: This bit is not used in the specific mode or state. Set to either 0 or 1.
	: Nothing is assigned.

*2

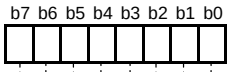
0	: 0 after reset
1	: 1 after reset
Undefined	: Undefined after reset

*3

RW	: Read and Write.
RO	: Read only. When written, the content depends on each bit.
WO	: Write only. When read, the content is undefined.
-	: When read, the content is undefined. When written, the content depends on each bit.

4. List of Registers

Port Pi



Port Pi (Pi) (i = 0 to 2)

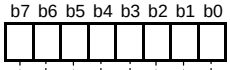
[Addresses 0000h, 0002h, 0004h]

b	Bit Name	Function	After Reset	RW
0	Port P_{i0}	• In output mode Write: Port latch Read: Port latch or peripheral function output (Note) • In input mode Write: Port latch Read: Pin value	0	RW
1	Port P_{i1}		0	RW
2	Port P_{i2}		0	RW
3	Port P_{i3}		0	RW
4	Port P_{i4}		0	RW
5	Port P_{i5}		0	RW
6	Port P_{i6}		0	RW
7	Port P_{i7}		0	RW

Note:
1. The following port reads the output value when the shared output function is selected.
   $P2_7$/CNTR$_0$/$\overline{SRDY1}$

Fig. 4.1 Structure of Port Pi (i = 0 to 2)

Port Pi direction register



Port Pi direction register (PiD) (i = 0 to 2)

[Addresses 0001h, 0003h, 0005h]

b	Bit Name	Function	After Reset	RW
0	Port P_{i0} direction register	0: Input mode 1: Output mode	0	WO
1	Port P_{i1} direction register	0: Input mode 1: Output mode	0	WO
2	Port P_{i2} direction register	0: Input mode 1: Output mode	0	WO
3	Port P_{i3} direction register	0: Input mode 1: Output mode	0	WO
4	Port P_{i4} direction register	0: Input mode 1: Output mode	0	WO
5	Port P_{i5} direction register	0: Input mode 1: Output mode	0	WO
6	Port P_{i6} direction register	0: Input mode 1: Output mode	0	WO
7	Port P_{i7} direction register	0: Input mode 1: Output mode	0	WO

Notes:
1. In the port set as output mode, the pull-up control bit becomes invalid, and the pull-up resistor is not connected.
2. In output mode, ports $P0_1$ and $P0_2$ can select the output structure by the $P0_1$/S_{OUT2}, $P0_2$/S_{CLK2} P-channel output disable bit (bit 7 in the serial I/O2 control register (address 0015h)).
3. In output mode, port $P2_5$ can select the output structure by the $P2_5$/TxD P-channel output disable bit (bit 4 in the UART control register (address 001Bh)).

Fig. 4.2 Structure of Port Pi direction register (i = 0 to 2)

Port Pi

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0					

Port Pi (Pi) (i = 3 or 4)

[Addresses 0006h, 0008h]

b	Bit Name	Function	After Reset	RW
0	Port Pi_0	• In output mode Write: Port latch Read: Port latch or output of peripheral functions (Note)	0	RW
1	Port Pi_1		0	RW
2	Port Pi_2		0	RW
3	Port Pi_3		0	RW
4	Port Pi_4	• In input mode Write: Port latch Read: Pin value	0	RW
5	When read, the value is 0. If necessary, set to 0.		0	RO
6			0	RO
7			0	RO

Note:
1. The following ports read the output value when the shared output function is selected.
$P4_0$/$CNTR_1$, $P4_3$/INT_2/$SCMP_2$, $P4_4$/INT_3/PWM

Fig. 4.3 Structure of Port Pi (i = 3 or 4)

Port Pi direction register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0					

Port Pi direction register (PiD) (i = 3 or 4)

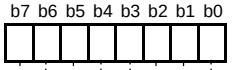
[Addresses 0007h, 0009h]

b	Bit Name	Function	After Reset	RW
0	Port Pi_0 direction register	0: Input mode 1: Output mode	0	WO
1	Port Pi_1 direction register	0: Input mode 1: Output mode	0	WO
2	Port Pi_2 direction register	0: Input mode 1: Output mode	0	WO
3	Port Pi_3 direction register	0: Input mode 1: Output mode	0	WO
4	Port Pi_4 direction register	0: Input mode 1: Output mode	0	WO
5	When read, the value is 0. If necessary, set to 0.		0	RO
6			0	RO
7			0	RO

Note:
1. In the port set as output mode, the pull-up control bit becomes invalid, and the pull-up resistor is not connected.

Fig. 4.4 Structure of Port Pi direction register (i = 3 or 4)

Port Pi pull-up control register (i = 0 to 2)



Port Pi pull-up control register (PULLi) (i = 0 to 2)

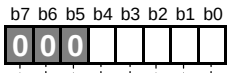
[Addresses 0010h, 0011h, 0012h]

b	Bit Name	Function	After Reset	RW
0	Port P_{i0} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
1	Port P_{i1} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
2	Port P_{i2} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
3	Port P_{i3} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
4	Port P_{i4} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
5	Port P_{i5} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
6	Port P_{i6} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
7	Port P_{i7} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW

Note:
1. In the port set as output mode, the pull-up control bit becomes invalid, and the pull-up resistor is not connected.

Fig. 4.5 Structure of Port Pi pull-up control register (i = 0 to 2)

Port Pi pull-up control register (i = 3 or 4)



Port Pi pull-up control register (PULLi) (i = 3 or 4)

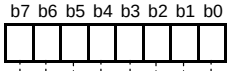
[Addresses 0013h, 0014h]

b	Bit Name	Function	After Reset	RW
0	Port P_{i0} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
1	Port P_{i1} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
2	Port P_{i2} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
3	Port P_{i3} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
4	Port P_{i4} pull-up control bit(1)	0: No pull-up 1: Pull-up	0	RW
5	When read, the value is 0. If necessary, set to 0.		0	RO
6			0	RO
7			0	RO

Note:
1. In the port set as output mode, the pull-up control bit becomes invalid, and the pull-up resistor is not connected.

Fig. 4.6 Structure of Port Pi pull-up control register (i = 3 or 4)

Serial I/O2 control register 1



Serial I/O2 control register 1 (SIO2CON1)

[Address 0015h]

b	Bit Name	Function	After Reset	RW
0	Internal synchronous clock selection bits	b2 b1 b0 0 0 0: f(XIN)/8 (f(XCIN)/8 in low-speed mode) 0 0 1: f(XIN)/16 (f(XCIN)/16 in low-speed mode)	0	RW
1		0 1 0: f(XIN)/32 (f(XCIN)/32 in low-speed mode) 0 1 1: f(XIN)/64 (f(XCIN)/64 in low-speed mode) 1 0 0: Not available	0	RW
2		1 0 1: Not available 1 1 0: f(XIN)/128(f(XCIN)/128 in low-speed mode) 1 1 1: f(XIN)/256(f(XCIN)/256 in low-speed mode)	0	RW
3	Serial I/O2 port selection bit	0: P01 and P02 pins: I/O port 1: P01 and P02 pins: SOUT2, SCLK2 signal output	0	RW
4	$S\overline{RDY2}$ output enable bit	0: P03 pin: I/O port 1: P03 pin: $S\overline{RDY2}$ signal output	0	RW
5	Transfer direction selection bit	0: LSB first 1: MSB first	0	RW
6	Serial I/O2 synchronous clock selection bit	0: External clock 1: Internal clock	0	RW
7	P01/SOUT2, P02/SCLK2 P-channel output disable bit	[Output mode] 0: CMOS output 1: N channel open-drain output In input mode, this bit is invalid.	0	RW

Fig. 4.7 Structure of Serial I/O2 control register 1

Serial I/O2 control register 2

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0

Serial I/O2 control register 2 (SIO2CON2)

[Address 0016h]

b	Bit Name	Function	After Reset	RW
0	Optional transfer bit	b2 b1 b0 0 0 0: 1 bit 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits	1	RW
1			1	RW
2			1	RW
3	When read, the value is 0. If necessary, set to 0.		0	RO
4			0	RO
5			0	RO
6	Serial I/O2 I/O comparison signal control bit	0: P4$_3$ pin: I/O port 1: P4$_3$ pin: SCMP2 signal output	0	RW
7	SOUT2 pin control bit	When SOUT2 output pin and external clock selected 0: Output active 1: Output high-impedance When SOUT2 output pin and internal clock are selected, this bit is invalid.	0	RW

Fig. 4.8 Structure of Serial I/O2 control register 2

Serial I/O2 register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 register (SIO2)

[Address 0017h]

b	Bit Name	Function	After Reset	RW
0	Data is serially transmitted from and received to this shift register. [Transmit] · Write transmission data. Do not write during transmit operation. [Receive] · Received data can be read. Do not read during receive operation.		Undefined	RW
1			Undefined	RW
2			Undefined	RW
3			Undefined	RW
4			Undefined	RW
5			Undefined	RW
6			Undefined	RW
7			Undefined	RW

Fig. 4.9 Structure of Serial I/O2 register

Transmit buffer register

b7 b6 b5 b4 b3 b2 b1 b0

Transmit buffer register (TB)

[Address 0018h]

b	Function	After Reset	RW
0	Transmission data is written to this buffer register.	Undefined	WO
1	Write transmission data to this register.	Undefined	WO
2		Undefined	WO
3		Undefined	WO
4		Undefined	WO
5		Undefined	WO
6		Undefined	WO
7		Undefined	WO

Note:
1. This register is assigned to the same address as the transmit buffer register. It cannot be written to.

Receive buffer register

b7 b6 b5 b4 b3 b2 b1 b0

Receive buffer register (TB)

[Address 0018h]

b	Function	After Reset	RW
0	Received data is read from this buffer register.	Undefined	WO
1	Read received data from this register.	Undefined	WO
2		Undefined	WO
3		Undefined	WO
4		Undefined	WO
5		Undefined	WO
6		Undefined	WO
7		Undefined	WO

Note:
1. This register is assigned to the same address as the transmit buffer register. It cannot be written to.

Fig. 4.10 Structure of Transmit buffer register and Receive buffer register

Serial I/O1 status register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O1 status register (SIOSTS)

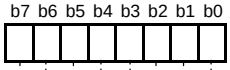
[Address 0019h]

b	Bit Name	Function	After Reset	RW
0	Transmit buffer empty flag (TBE)(1)	0: Buffer full 1: Buffer empty	0	RO
1	Transmit buffer full flag (RBF)(1, 2)	0: Buffer empty 1: Buffer full	0	RO
2	Transmit shift completion flag (TSC)(1)	0: Transmit shift in progress 1: Transmit shift completed	0	RO
3	Overrun error flag (OE)(3)	0: No error 1: Overrun error	0	RO
4	Parity error flag (PE)(3)	0: No error 1: Parity error	0	RO
5	Framing error flag (FE)(3)	0: No error 1: Framing error	0	RO
6	Summing error flag (SE)(3)	0: (OE) U (PE) U (FE) = 0 1: (OE) U (PE) U (FE) = 1	0	RO
7	When read, the value is 1. If necessary, set to 1.		1	RO

Notes:
1. If necessary, set to 0.
2. Reading the transmit register returns 0.
3. Writing to this register sets this bit to 0. If necessary, set to 0.

Fig. 4.11 Structure of Serial I/O1 status register

Serial I/O1 control register



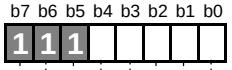
Serial I/O1 control register (SIOCON)

[Address 001Ah]

b	Bit Name	Function	After Reset	RW
0	BRG count source selection bit (CSS)	0: f(X_{IN}) (f(XC_{IN}) in low-speed mode) 1: f(X_{IN})/4 (f(XC_{IN})/4 in low-speed mode)	0	RW
1	Serial I/O1 synchronous clock selection bit (SCS)	[Clock synchronous serial I/O mode] 0: BRG output divided by 4 1: External clock input [UART mode] 0: BRG output divided by 16 1: External clock divided by 16	0	RW
2	$\overline{S_{RDY1}}$ output enable bit (SRDY)	0: Output disabled ($P2_7$ pin: I/O port) 1: Output pin ($P2_7$ pin: $\overline{S_{RDY1}}$ pin)	0	RW
3	Transmit interrupt source selection bit (TIC)	0: Transmit buffer register has emptied (TBE = 1) 1: Transmit shift register operation is completed (TSC = 1)	0	RW
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	RW
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	RW
6	Serial I/O1 mode selection bit (SIOM)	0: UART mode 1: Clock synchronous serial I/O mode	0	RW
7	Serial I/O1 enable bit (SIOE)	0: Serial I/O1 disabled ($P2_4$ to $P2_7$ pins: I/O port) 1: Serial I/O1 enabled ($P2_4$ to $P2_7$ pins: Serial I/O1 function pin)	0	RW

Fig. 4.12 Structure of Serial I/O1 control register

UART control register



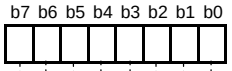
UART control register (UARTCON)

[Address 001Bh]

b	Bit Name	Function	After Reset	RW
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	RW
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	RW
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	RW
4	P25/TXD P-channel output disable bit (POFF)	[Output mode] 0: CMOS output 1: N-channel open-drain output In input mode, this bit is invalid.	0	RW
5	When read, the value is 1. If necessary, set to 1.		1	RO
6			1	RO
7			1	RO

Fig. 4.13 Structure of UART control register

Baud rate generator



Baud rate generator (BRG)

[Address 001Ch]

b	Bit Name	Function	After Reset	RW
0	Set the division frequency of the BRG count source.		Undefined	RW
1	The baud rate generator divides the BRG count source by (n+1),		Undefined	RW
2	where n is the setting value.		Undefined	RW
3			Undefined	RW
4			Undefined	RW
5			Undefined	RW
6			Undefined	RW
7			Undefined	RW

Note:
1. Write data to this register while transmit and receive operations are stopped.

Fig. 4.14 Structure of Baud rate generator

PWM control register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

PWM control register (PWMCON)
[Address 001Dh]

b	Bit Name	Function	After Reset	RW
0	PWM function enable bit	0: PWM disabled 1: PWM enabled	0	RW
1	Count source selection bit	0: f(XIN) (f(XCIN) in low-speed mode) 1: f(XIN)/2 (f(XCIN)/2 in low-speed mode)	0	RW
2	When read, the value is 0. If necessary, set to 0.		0	RO
3			0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.15 Structure of PWM control register

PWM prescaler

b7	b6	b5	b4	b3	b2	b1	b0

PWM prescaler (PREPWM)
[Address 001Eh]

b	Function	After Reset	RW
0	• Set the PWM period. • The value set in this register is written to both PWM prescaler prelatch and PWM prescaler latch simultaneously. • When data is written to this register during PWM output, pulses corresponded to the changed value are output from the next period. • When this registers is read, the value of PWM prescaler latch is read.	Undefined	RW
1		Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Fig. 4.16 Structure of PWM prescaler

PWM register

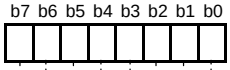
b7	b6	b5	b4	b3	b2	b1	b0

PWM register (PWM)
[Address 001Fh]

b	Function	After Reset	RW
0	• Set the PWM period. • The value set in this register is written to both PWM register prelatch and PWM register latch simultaneously. • When data is written to this register during PWM output, pulses corresponded to the changed value are output from the next period. • When this registers is read, the value of PWM register latch is read.	Undefined	RW
1		Undefined	RW
2		Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Fig. 4.17 Structure of PWM register

Prescaler 12, Prescaler X, Prescaler Y



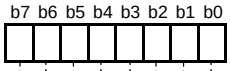
Prescaler 12 (PRE12), Prescaler X (PREX), Prescaler Y (PREY)

[Addresses 0020h, 0024h, 0026h]

b	Function	After Reset	RW
0	• Set the count initial value. These registers count (n+1) times, where the setting value is n. [Write] • Write to the prescaler latch and the corresponding prescaler simultaneously. [Read] • The content is the count value of the corresponding prescaler.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.18 Structure of Prescaler 12, Prescaler X, Prescaler Y

Timer 1



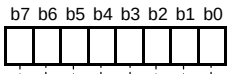
Timer 1 (T1)

[Address 0021h]

b	Function	After Reset	RW
0	• Set the count initial value. Timer 1 register counts (n+1) times, where the setting value is n. [Write] • Write to timer 1 latch and timer 1simultaneously. [Read] • The content is the count value of timer 1.	1	RW
1		0	RW
2		0	RW
3		0	RW
4		0	RW
5		0	RW
6		0	RW
7		0	RW

Fig. 4.19 Structure of Timer 1

Timer 2



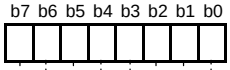
Timer 2 (T2)

[Address 0022h]

b	Function	After Reset	RW
0	• Set the count initial value. Timer 2 register counts (n+1) times, where the setting value is n. [Write] • Write to timer 2 latch and timer 2 simultaneously. [Read] • The content is the count value of timer 2.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.20 Structure of Timer 2

Timer X, Timer Y



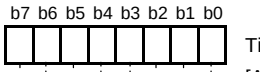
Timer X (TX), Timer Y (TY)

[Addresses 0025h, 0027h]

b	Function	After Reset	RW
0	• Set the count initial value. These registers count (n+1) times, where the setting value is n. [Write] • Write to the timer latches and corresponding timers simultaneously. [Read] • The content is the count value of the corresponding timer.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.21 Structure of Timer X, Timer Y

Timer XY mode register



Timer XY mode register (TM)
[Address 0023h]

b	Function		After Reset	RW
0	Timer X operating mode bits	b1 b0 0 0: Timer mode 0 1: Pulse output mode 1 0: Event counter mode 1 1: Pulse width measurement mode	0	RW
1			0	RW
2	$CNTR_0$ active edge switch bit	Function varies depending on timer X operating mode. (Refer to Table 4.1)	0	RW
3	Timer X count stop bit	0: Count start 1: Count stop	0	RW
4	Timer Y operating mode bits	b5 b4 0 0: Timer mode 0 1: Pulse output mode 1 0: Event counter mode 1 1: Pulse width measurement mode	0	RW
5			0	RW
6	$CNTR_1$ active edge switch bit	Function varies depending on timer Y operating mode. (Refer to Table 4.2)	0	RW
7	Timer Y count stop bit	0: Count start 1: Count stop	0	RW

Fig. 4.22 Structure of Timer XY mode register

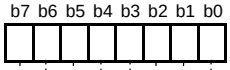
Table 4.1 $CNTR_0$ active edge switch bit function

Timer X operation mode	Setting value	Timer function selection	$CNTR_0$ interrupt request occurrence source
Timer mode	0	—	$CNTR_0$ input signal falling edge (No influence on timer count)
	1	—	$CNTR_0$ input signal rising edge (No influence on timer count)
Pulse output mode	0	Pulse output start: "H" output	Output signal falling edge
	1	Pulse output start: "L" output	Output signal rising edge
Event counter mode	0	Count at rising edge	Input signal falling edge
	1	Count at falling edge	Input signal rising edge
Pulse width measurement mode	0	Measurement of "H" width	Input signal falling edge
	1	Measurement of "L" width	Input signal rising edge

Table 4.2 $CNTR_1$ active edge switch bit function

Timer Y operation mode	Setting value	Timer function selection	$CNTR_1$ interrupt request occurrence source
Timer mode	0	—	$CNTR_1$ input signal falling edge (No influence on timer count)
	1	—	$CNTR_1$ input signal rising edge (No influence on timer count)
Pulse output mode	0	Pulse output start: "H" output	Output signal falling edge
	1	Pulse output start: "L" output	Output signal rising edge
Event counter mode	0	Count at rising edge	Input signal falling edge
	1	Count at falling edge	Input signal rising edge
Pulse width measurement mode	0	Measurement of "H" width	Input signal falling edge
	1	Measurement of "L" width	Input signal rising edge

Timer Z1 mode register



Timer Z1 mode register (TZ1M)

[Address 0028h]

b	Function		After Reset	RW
0	Timer Z1 operating mode bits	b2 b1 b0 0 0 0: Timer/Event counter mode 0 0 1: Pulse output mode 0 1 0: Pulse period measurement mode 0 1 1: Pulse width measurement mode 1 0 0: Programmable waveform generating mode 1 0 1: Programmable one-shot generating mode 1 1 0: Not available 1 1 1: Not available	0	RW
1			0	RW
2			0	RW
3	Timer Z1 write control bit	0: Write to both the latch and the timer simultaneously 1: Write to the latch only	0	RW
4	Output level latch	0: "L" output 1: "H" output	0	RW
5	$CNTR_2$ active edge switch bit	Function varies depending on timer Z1 operating mode. (Refer to Table 4.3)	0	RW
6	Timer Z1 count stop bit	0: Count start 1: Count stop	0	RW
7	Timer mode/Event counter mode switch bit (Note)	0: Timer mode 1: Event counter mode	0	RW

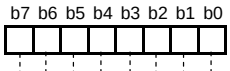
Note:
1. When selecting the modes other than the timer /event counter mode, set 0 to this bit.

Fig. 4.23 Structure of Timer XY mode register

Table 4.3 $CNTR_2$ active edge switch bit function

Timer Z1 operation mode	Setting value	Timer function selection	$CNTR_2$ interrupt request occurrence source
Timer mode	0	—	$CNTR_2$ input signal falling edge (No influence on timer count)
	1	—	$CNTR_2$ input signal rising edge (No influence on timer count)
Event counter mode	0	Count at rising edge	Input signal falling edge
	1	Count at falling edge	Input signal rising edge
Pulse output mode	0	Pulse output start: “H” output	Output signal falling edge
	1	Pulse output start: “L” output	Output signal rising edge
Pulse period measurement mode	0	Falling: Measurement b/w falling edges	Input signal falling edge
	1	Rising: Measurement b/w rising edges	Input signal rising edge
Pulse width measurement mode	0	Measurement of “H” width	Input signal falling edge
	1	Measurement of “L” width	Input signal rising edge
Programmable one-shot generating mode	0	After “L” output start, "H" one-shot pulse output	Output signal falling edge
	1	After “H” output start, "L" one-shot pulse output	Output signal rising edge

Timer Z1 high-order register, Timer Z1 low-order register

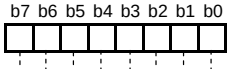


Timer Z1 high-order register (TZ1H), Timer Z1 low-order register (TZ1L)
[Addresses 002Ah, 0029h]

b	Function	After Reset	RW
0	• Set the count initial value. These registers count (n+1) times, where the setting value is n. [Write] Depending on timer Z1 write control bit, these registers operate as follows. 0: Write to both timer Z1 latch and timer Z1 simultaneously. 1: Write to timer Z1 latch only. Write to these registers in order from low-order to high-order. This operation is not affected by timer Z1 stop control bit. [Read] The content is the count value of timer Z1. Read from these registers in order from high-order to low-order.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.24 Structure of Timer Z1 high-order register, Timer Z1 low-order register

Timer Z2 high-order register, Timer Z2 low-order register

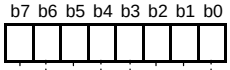


Timer Z2 high-order register (TZ2H), Timer Z2 low-order register (TZ2L)
[Addresses 002Dh, 002Ch]

b	Function	After Reset	RW
0	• Set the count initial value. These registers count (n+1) times, where the setting value is n. [Write] Depending on timer Z2 write control bit , these registers operate as follows. 0: Write to both timer Z2 latch and timer Z2 simultaneously. 1: Write to timer Z2 latch only. Write to these registers in order from low-order to high-order. This operation is not affected by timer Z2 stop control bit. [Read] The content is the count value of timer Z2. Read from these registers in order from high-order to low-order.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Fig. 4.25 Structure of Timer Z2 high-order register, Timer Z2 low-order register

Timer Z2 mode register



Timer Z2 mode register (TZ2M)

[Address 002Bh]

b	Bit Name	Function	After Reset	RW
0	Timer Z2 operating mode bits	b2 b1 b0 0 0 0: Timer/Event counter mode 0 0 1: Pulse output mode	0	RW
1		0 1 0: Pulse period measurement mode 0 1 1: Pulse width measurement mode 1 0 0: Programmable waveform generating mode	0	RW
2		1 0 1: Programmable one-shot generating mode 1 1 0: Not available 1 1 1: Not available	0	RW
3	Timer Z2 write control bit	0: Write to both the latch and the timer simultaneously 1: Write to the latch only	0	RW
4	Output level latch	0: "L" output 1: "H" output	0	RW
5	$CNTR_3$ active edge switch bit	Function varies depending on timer Z2 operating mode. (Refer to Table 4.4.)	0	RW
6	Timer Z2 count stop bit	0: Count start 1: Count stop	0	RW
7	Timer mode/Event counter mode switch bit (Note)	0: Timer mode 1: Event counter mode	0	RW

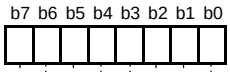
Note:
1. When selecting the modes other than the timer /event counter mode, set 0 to this bit.

Fig. 4.26 Structure of Timer Z2 mode register

Table 4.4 $CNTR_3$ active edge switch bit function

Timer Z2 operation mode	Setting value	Timer function selection	$CNTR_3$ interrupt request occurrence source
Timer mode	0	—	$CNTR_3$ input signal falling edge (No influence on timer count)
	1	—	$CNTR_3$ input signal rising edge (No influence on timer count)
Event counter mode	0	Count at rising edge	Input signal falling edge
	1	Count at falling edge	Input signal rising edge
Pulse output mode	0	Pulse output start: “H” output	Output signal falling edge
	1	Pulse output start: “L” output	Output signal rising edge
Pulse period measurement mode	0	Falling: Measurement b/w falling edges	Input signal falling edge
	1	Rising: Measurement b/w rising edges	Input signal rising edge
Pulse width measurement mode	0	Measurement of “H” width	Input signal falling edge
	1	Measurement of “L” width	Input signal rising edge
Programmable one-shot generating mode	0	After “L” output start, "H" one-shot pulse output	Output signal falling edge
	1	After “H” output start, "L" one-shot pulse output	Output signal rising edge

Timer 12, X count source selection register



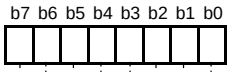
Timer 12, X count source selection register (T12XCSS)

[Address 002Eh]

b	Function		After Reset	RW
0	Timer 12 count source selection bits	b3 b2 b1 b0 0 0 0 0: f(XIN)/2 (f(XCIN)/2 in low-speed mode) 0 0 0 1: f(XIN)/4 (f(XCIN)/4 in low-speed mode) 0 0 1 0: f(XIN)/8 (f(XCIN)/8 in low-speed mode)	1	RW
1		0 0 1 1: f(XIN)/16 (f(XCIN)/16 in low-speed mode) 0 1 0 0: f(XIN)/32 (f(XCIN)/32 in low-speed mode) 0 1 0 1: f(XIN)/64 (f(XCIN)/64 in low-speed mode) 0 1 1 0: f(XIN)/128 (f(XCIN)/128 in low-speed mode)	1	RW
2		0 1 1 1: f(XIN)/256 (f(XCIN)/256 in low-speed mode) 1 0 0 0: f(XIN)/512 (f(XCIN)/512 in low-speed mode) 1 0 0 1: f(XIN)/1024 (f(XCIN)/1024 in low-speed mode) 1 0 1 0: Not available	0	RW
3		1 0 1 1: Not available 1 1 0 0: Not available 1 1 0 1: Not available 1 1 1 0: Not available 1 1 1 1: Not available	0	RW
4	Timer X count source selection bits	b7 b6 b5 b4 0 0 0 0: f(XIN)/2 (f(XCIN)/2 in low-speed mode) 0 0 0 1: f(XIN)/4 (f(XCIN)/4 in low-speed mode) 0 0 1 0: f(XIN)/8 (f(XCIN)/8 in low-speed mode)	1	RW
5		0 0 1 1: f(XIN)/16 (f(XCIN)/16 in low-speed mode) 0 1 0 0: f(XIN)/32 (f(XCIN)/32 in low-speed mode) 0 1 0 1: f(XIN)/64 (f(XCIN)/64 in low-speed mode) 0 1 1 0: f(XIN)/128 (f(XCIN)/128 in low-speed mode)	1	RW
6		0 1 1 1: f(XIN)/256 (f(XCIN)/256 in low-speed mode) 1 0 0 0: f(XIN)/512 (f(XCIN)/512 in low-speed mode) 1 0 0 1: f(XIN)/1024 (f(XCIN)/1024 in low-speed mode) 1 0 1 0 : f(XCIN)	0	RW
7		1 0 1 1: Not available 1 1 0 0: Not available 1 1 0 1: Not available 1 1 1 0: Not available 1 1 1 1: Not available	0	RW

Fig. 4.27 Structure of Timer 12, X count source selection register

Timer Y, Z1 count source selection register



Timer Y, Z1 count source selection register (TYZ1CSS)

[Address 002Fh]

b	Function		After Reset	RW
0	Timer Y count source selection bits	b3 b2 b1 b0 0 0 0 0: f(XIN)/2 (f(XCIN)/2 in low-speed mode) 0 0 0 1: f(XIN)/4 (f(XCIN)/4 in low-speed mode) 0 0 1 0: f(XIN)/8 (f(XCIN)/8 in low-speed mode)	1	RW
1		0 0 1 1: f(XIN)/16 (f(XCIN)/16 in low-speed mode) 0 1 0 0: f(XIN)/32 (f(XCIN)/32 in low-speed mode) 0 1 0 1: f(XIN)/64 (f(XCIN)/64 in low-speed mode) 0 1 1 0: f(XIN)/128 (f(XCIN)/128 in low-speed mode)	1	RW
2		0 1 1 1: f(XIN)/256 (f(XCIN)/256 in low-speed mode) 1 0 0 0: f(XIN)/512 (f(XCIN)/512 in low-speed mode) 1 0 0 1: f(XIN)/1024 (f(XCIN)/1024 in low-speed mode) 1 0 1 0 : f(XCIN)	0	RW
3		1 0 1 1: Not available 1 1 0 0: Not available 1 1 0 1: Not available 1 1 1 0: Not available 1 1 1 1: Not available	0	RW
4	Timer Z1 count source selection bits	b7 b6 b5 b4 0 0 0 0: f(XIN)/2 (f(XCIN)/2 in low-speed mode) 0 0 0 1: f(XIN)/4 (f(XCIN)/4 in low-speed mode) 0 0 1 0: f(XIN)/8 (f(XCIN)/8 in low-speed mode)	1	RW
5		0 0 1 1: f(XIN)/16 (f(XCIN)/16 in low-speed mode) 0 1 0 0: f(XIN)/32 (f(XCIN)/32 in low-speed mode) 0 1 0 1: f(XIN)/64 (f(XCIN)/64 in low-speed mode) 0 1 1 0: f(XIN)/128 (f(XCIN)/128 in low-speed mode)	1	RW
6		0 1 1 1: f(XIN)/256 (f(XCIN)/256 in low-speed mode) 1 0 0 0: f(XIN)/512 (f(XCIN)/512 in low-speed mode) 1 0 0 1: f(XIN)/1024 (f(XCIN)/1024 in low-speed mode) 1 0 1 0 : f(XCIN)	0	RW
7		1 0 1 1: Not available 1 1 0 0: Not available 1 1 0 1: Not available 1 1 1 0: Not available 1 1 1 1: Not available	0	RW

Fig. 4.28 Structure of Timer Y, Z1 count source selection register

Timer Z2 count source selection register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

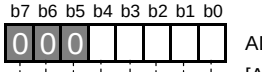
Timer Z2 count source selection register (TZ2CSS)

[Address 0030h]

b	Function		After Reset	RW
0	Timer Z2 count source selection bits	b3 b2 b1 b0 0 0 0 0: f(XIN)/2 (f(XCIN)/2 in low-speed mode) 0 0 0 1: f(XIN)/4 (f(XCIN)/4 in low-speed mode) 0 0 1 0: f(XIN)/8 (f(XCIN)/8 in low-speed mode)	1	RW
1		0 0 1 1: f(XIN)/16 (f(XCIN)/16 in low-speed mode) 0 1 0 0: f(XIN)/32 (f(XCIN)/32 in low-speed mode) 0 1 0 1: f(XIN)/64 (f(XCIN)/64 in low-speed mode) 0 1 1 0: f(XIN)/128 (f(XCIN)/128 in low-speed mode)	1	RW
2		0 1 1 1: f(XIN)/256 (f(XCIN)/256 in low-speed mode) 1 0 0 0: f(XIN)/512 (f(XCIN)/512 in low-speed mode) 1 0 0 1: f(XIN)/1024 (f(XCIN)/1024 in low-speed mode) 1 0 1 0 : f(XCIN)	0	RW
3		1 0 1 1: Not available 1 1 0 0: Not available 1 1 0 1: Not available 1 1 1 0: Not available 1 1 1 1: Not available	0	RW
4	When read, the value is 0. If necessary, set to 0.		0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.29 Structure of Timer Z2 count source selection register

AD control register



AD control register (ADCON)

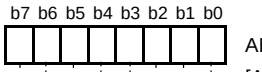
[Address 0034h]

b	Bit Name	Function	After Reset	RW
0	Analog input pin selection bits	b3 b2 b1 b0 0 0 0 0 : P3$_0$/AN$_0$ 0 0 0 1 : P3$_1$/AN$_1$ 0 0 1 0 : P3$_2$/AN$_2$	0	RW
1		0 0 1 1 : P3$_3$/AN$_3$ 0 1 0 0 : P3$_4$/AN$_4$ 0 1 0 1 : P0$_4$/AN$_5$ 0 1 1 0 : P0$_5$/AN$_6$	0	RW
2		0 1 1 1 : P0$_6$/AN$_7$ 1 0 0 0 : P0$_7$/AN$_8$ 1 0 0 1: Not available 1 0 1 0: Not available	0	RW
3		1 0 1 1: Not available 1 1 0 0: Not available 1 1 0 1: Not available 1 1 1 0: Not available 1 1 1 1: Not available	0	RW
4	AD conversion complete bit	0: Conversion in progress 1: Conversion completed	1	RW (1)
5	When read, the value is 0. If necessary, set to 0.		0	RO
6			0	RO
7			0	RO

Note:
1. This bit can be set to 0, but not to 1 by a program.

Fig. 4.30 Structure of AD control register

AD conversion register



AD conversion register (AD)

[Address 0035h]

b	Function	After Reset	RW
0	AD conversion results are read from this register.	Undefined	RO
1	If necessary, set to 00h.	Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note:
1. Do not read this register while A/D conversion is in progress.

Fig. 4.31 Structure of AD conversion register

Interrupt source selection register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0					

Interrupt source selection register (INTSEL)

[Address 0036h]

b	Bit Name	Function	After Reset	RW
0	INT_3/Serial I/O2 interrupt source selection bit	0: INT_3 interrupt 1: Serial I/O2 interrupt	0	RW
1	TimerZ1/$CNTR_2$ interrupt source selection bit	0: Timer Z1 interrupt 1: $CNTR_2$ interrupt	0	RW
2	TimerZ2/$CNTR_3$ interrupt source selection bit	0: TimerZ2 interrupt 1: $CNTR_3$ interrupt	0	RW
3	$CNTR_0$/$CNTR_2$ interrupt source selection bit	0: $CNTR_0$ interrupt 1: $CNTR_2$ interrupt	0	RW
4	$CNTR_1$/$CNTR_3$ interrupt source selection bit	0: $CNTR_1$ interrupt 1: $CNTR_3$ interrupt	0	RW
5	When read, the value is 0. If necessary, set to 0.		0	RO
6			0	RO
7			0	RO

Fig. 4.32 Structure of Interrupt source selection register

MISRG

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

MISRG(MISRG)

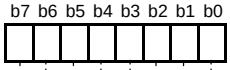
[Address 0038h]

b	Bit Name	Function	After Reset	RW
0	Oscillation stabilizing time set bit after STP instruction released	0: Sets 01h to timer 1 and FFh to prescaler 12 automatically. 1: Does not set automatically.	0	RW
1	Middle-speed mode automatic switch set bit	0: Disabled 1: Automatic switch enabled (Note)	0	RW
2	Middle-speed mode automatic switch wait time set bit	0: 6.5 to 7.5 machine cycles 1: 4.5 to 5.5 machine cycles	0	RW
2	Middle-speed mode automatic switch start bit (software dependent)	0: Invalid 1: Automatic switch start (Note)	0	RW
4	When read, the value is 0. If necessary, set to 0.		0	RO
5			0	RO
6			0	RO
7			0	RO

Note:
1. When the mode is automatically switched from the low-speed mode to the middle-speed mode, the value of CPU mode register (address 003Bh) also changes.

Fig. 4.33 Structure of MISRG

Watchdog timer control register



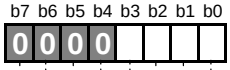
Watchdog timer control register (WDTCON)

[Address 0039h]

b	Bit Name	Function	After Reset	RW
0	Watchdog timer H		1	RO
1	(for read-out of high-order 6 bits)		1	RO
2			1	RO
3			1	RO
4			1	RO
5			1	RO
6	STP instruction function selection bit	0: Enter to stop mode by execution of STP instruction 1: Internal reset by execution of STP instruction	0	RW
7	Watchdog timer H count source selection bit	0: Watchdog timer L underflow 1: f(X_{IN})/16 (f(X_{CIN})/16 in low-speed mode)	0	RW

Fig. 4.34 Structure of Watchdog timer control register

Interrupt edge selection register



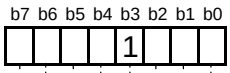
Interrupt edge selection register (INTEDGE)

[Address 003Ah]

b	Bit Name	Function	After Reset	RW
0	INT_0 active edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
1	INT_1 active edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
2	INT_2 active edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
2	INT_3 active edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
4	When read, the value is 0. If necessary, set to 0.		0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.35 Structure of Interrupt edge selection register

CPU mode register



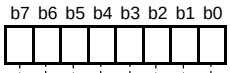
CPU mode register (CPUM)

[Address 003Bh]

b	Bit Name	Function	After Reset	RW
0	Processor mode bits	b1 b0 0 0: Single-chip mode	0	RW
1		0 1: Not available 1 0: Not available 1 1: Not available	0	RW
2	Stack page selection bit	0: 0 page 1: 1 page	0	RW
3	If necessary, set to 1.		1	RW
4	Port X_C switch bit	0: I/O port function (Oscillation stop) 1: X_{CIN}-X_{COUT} oscillation function	0	RW
5	Main clock (X_{IN}-X_{OUT}) stop bit	0: Oscillation 1: Stop	0	RW
6	Clock division ratio selection bits	b7 b6 0 0: f = f(X_{IN})/2 (High-speed mode)	1	RW
7		0 1: f = f(X_{IN})/8 (Middle-speed mode) 1 0: f = f(X_{CIN})/2 (Low-speed mode) 1 1: Not available	0	RW

Fig. 4.36 Structure of CPU mode register

Interrupt request register 1



Interrupt request register 1 (IREQ1)

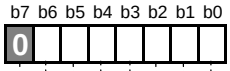
[Address 003Ch]

b	Bit Name	Function	After Reset	RW
0	INT_0 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
1	Timer Z1/$CNTR_2$ interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
2	INT_1 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
3	INT_2 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
4	INT_3/Serial I/O2 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
5	Timer Z2/$CNTR_3$ interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
6	Timer X interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
7	Timer Y interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)

Note:
1. Each of these bits can be set to 0, but not to 1 by a program.

Fig. 4.37 Structure of Interrupt request register 1

Interrupt request register 2



Interrupt request register 2 (IREQ2)

[Address 003Dh]

b	Bit Name	Function	After Reset	RW
0	Timer 1 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
1	Timer 2 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
2	Serial I/O1 receive interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
3	Serial I/O1 transmit interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
4	$CNTR_0$/$CNTR_2$ interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
5	$CNTR_1$/$CNTR_3$ interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
6	AD conversion interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
7	When read, the value is 0. If necessary, set to 0.		0	RO

Note:
1. Each of these bits can be set to 0, but not to 1 by a program.

Fig. 4.38 Structure of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1)

[Address 003Eh]

b	Bit Name	Function	After Reset	RW
0	INT_0 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
1	Timer Z1/CNTR2 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
2	INT_1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
3	INT_2 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
4	INT_3/Serial I/O2 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
5	Timer Z2/$CNTR_3$ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
6	Timer X interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
7	Timer Y interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW

Fig. 4.39 Structure of Interrupt control register 1

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt control register 2 (ICON2)

[Address 003Fh]

b	Bit Name	Function	After Reset	RW
0	Timer 1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
1	Timer 2 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
2	Serial I/O1 receive interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
3	Serial I/O1 transmit interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
4	$CNTR_0$/$CNTR_2$ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
5	$CNTR_1$/$CNTR_3$ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
6	AD conversion interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
7	When read, the value is 0. If necessary, set to 0.		0	RW

Fig. 4.40 Structure of Interrupt control register 2

5. Reference

Datasheet
3858 Group Datasheet
The latest version can be downloaded from the Renesas Technology website.

Technical News/Technical Update
The latest information can be downloaded from the Renesas Technology website.

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