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April 1st, 2010
Renesas Electronics Corporation

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3858 Group

Clock Generation Circuit (Processing During Power Failure)

1. Abstract

This document describes how to set up and use the clock generation circuit (processing during power failure) on the 3858 Group.

2. Introduction

The application example described in this document is applied to the following:

MCU: 3858 Group
Oscillation frequency (f(XIN): 8 MHz
Oscillation frequency (f(XCIN): 32.768 MHz

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operating conditions of the user system.

3. Contents

3.1 Clock Generated Circuit (Processing During Power Failure)

Outline: During a power failure, the backup power supply enables the clock count in low-speed and wait modes, making low power consumption possible.

Specifications:

- The MCU normally operates in high-speed mode.
- When a power failure is detected, the system clock is switched to low-speed mode and the main clock oscillation stops.
- Using wait mode, exit conditions from a power failure are confirmed in the timer interrupt routine generated every one second.
- When an exit from a power failure is detected, the main clock oscillation starts. After the oscillation stabilizes, the system clock is switched to high-speed mode.

Figure 3.1 shows the Mode Transition Example of System Clock During Power Failure, Figure 3.2 shows the Relevant Register Settings, and Figure 3.3 shows the Control Procedure.

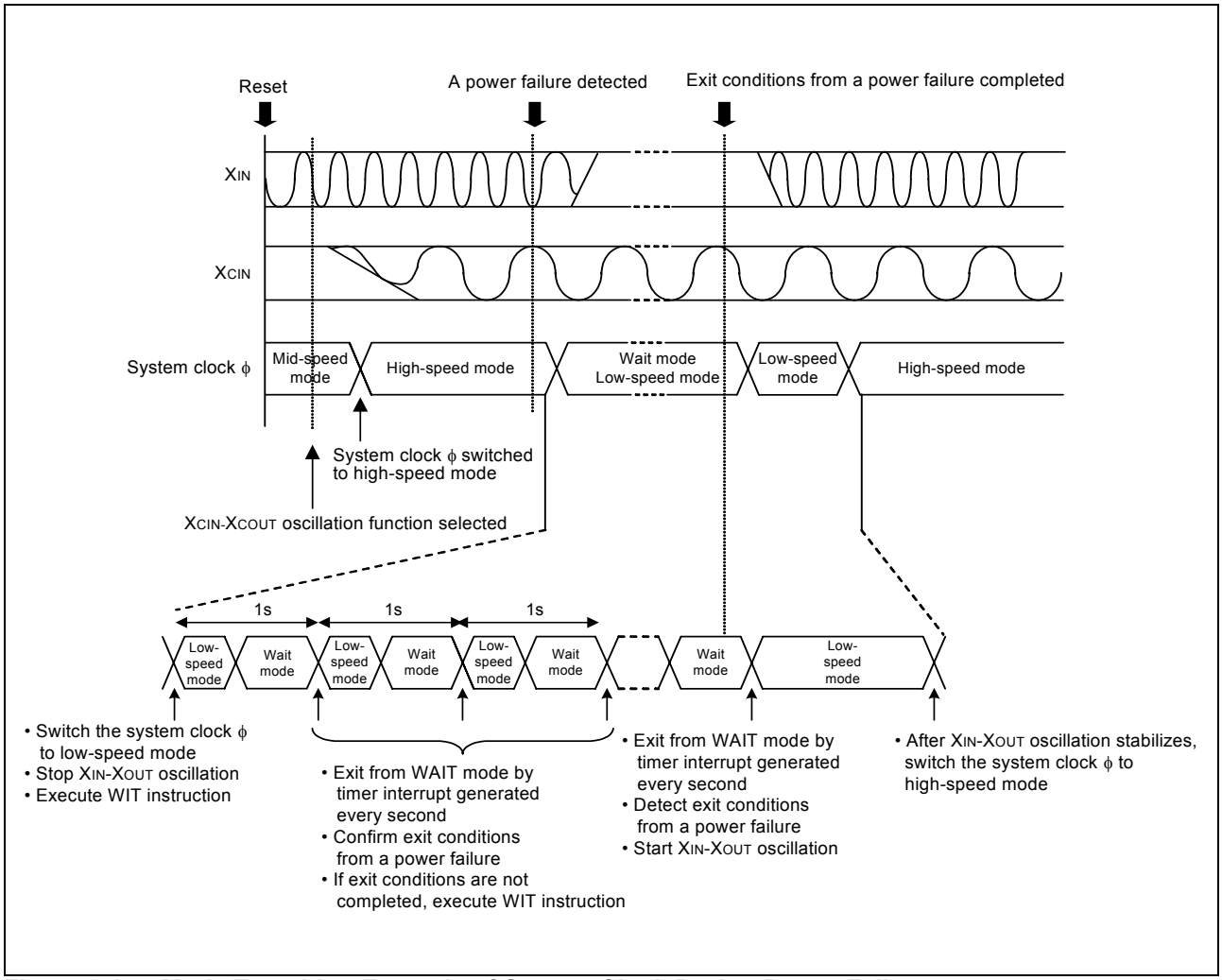

Figure 3.1 Mode Transition Example of System Clock During Power Failure

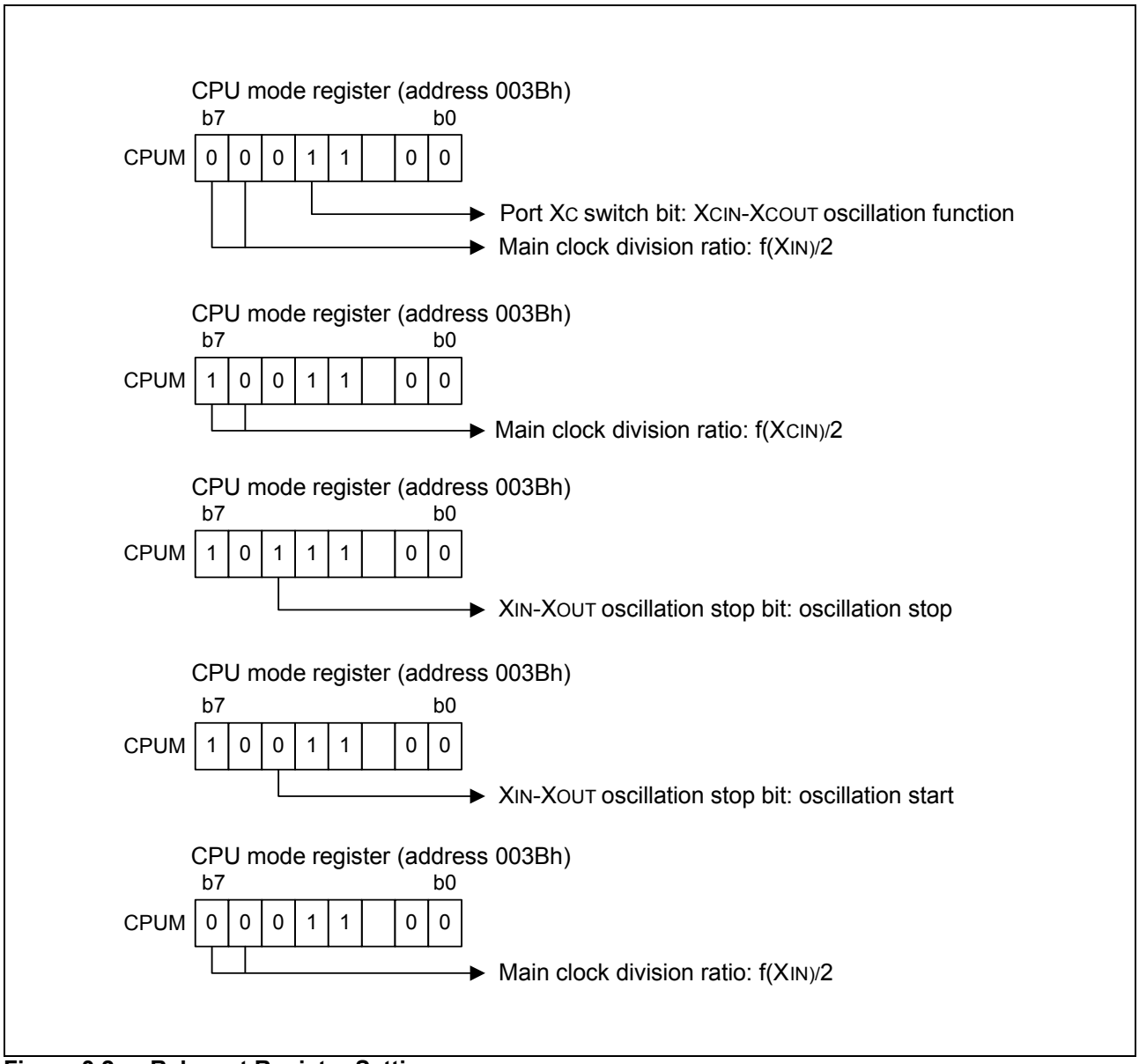

Figure 3.2 Relevant Register Settings

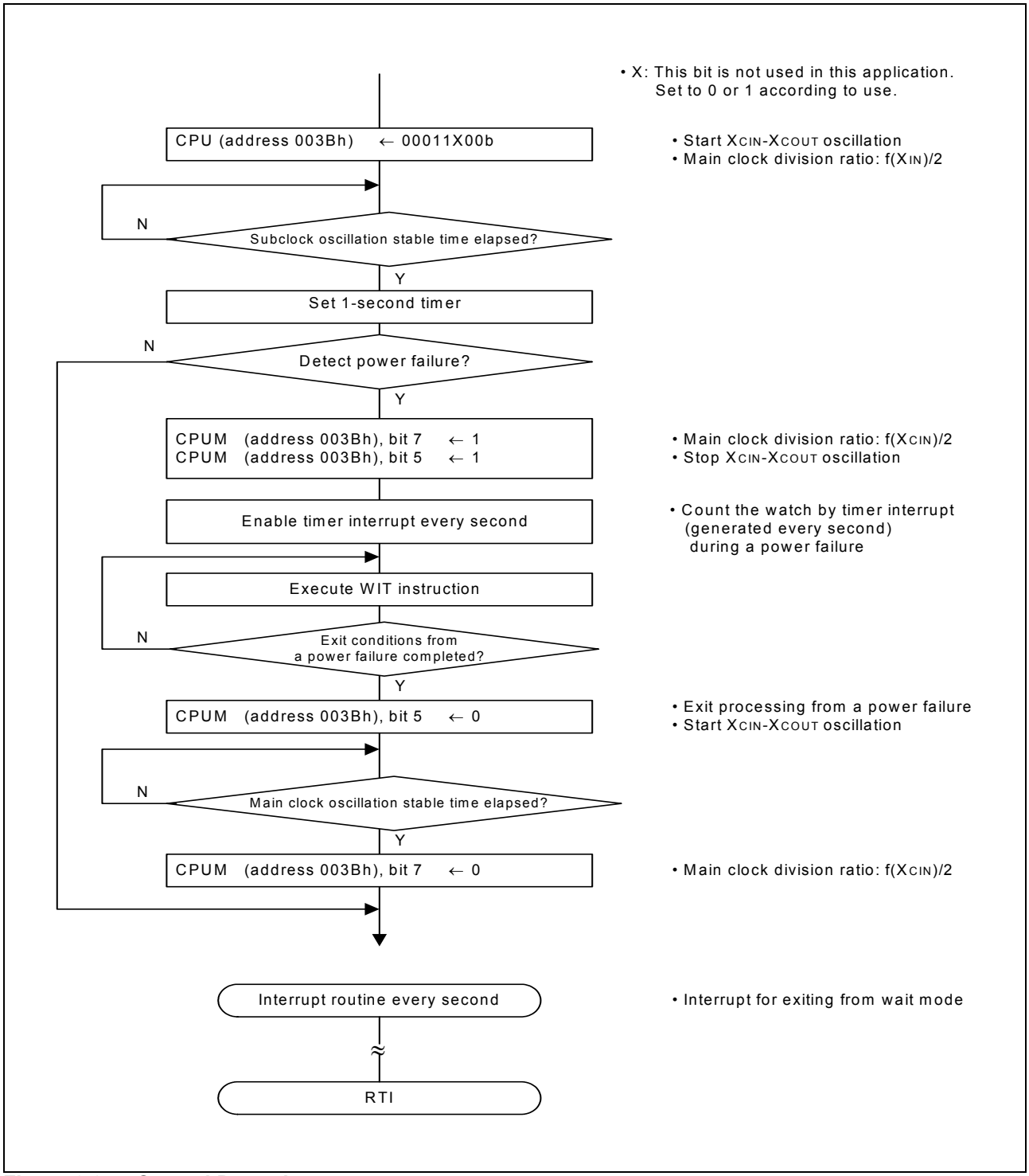

Figure 3.3 Control Procedure

4. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click “Application Notes” in the left-side hand menu on the page of the 3858 Group.

5. Reference Document

Datasheet
3858 Group Datasheet
Download the latest version from the Renesas Technology website.

Technical News/Technical Update
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REVISION HISTORY	3858 Group Clock Generation Circuit (Processing During Power Failure) Application Note

Rev.	Date	Description	
		Page	Summary
1.00	Aug 10, 2006	–	First Edition issued

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