1+1 PROTECTION WITHOUT RELAYS USING IDT82V2044/48/48L & IDT82V2054/58/58L HITLESS PROTECTION SWITCHING

APPLICATION NOTE
AN-357

1.0 INTRODUCTION

In today's highly competitive market, high quality of service, QOS, and reliability is one of the most important factors in bringing a product to market. Toward that end, redundancy is one way to ensure reliability. Although, protection schemes already exist in high-speed communications networks, to minimize vulnerability and failures, redundancy in a 1+1 protection scheme will allow failures to be isolated without minimal disruption of service.

A 1+1 protection scheme is comprised of two line cards, a primary and secondary, and a line monitoring circuit. When the line monitoring circuit detects a line failure, traffic is simply switched from the primary line card to the secondary line card without the use of external relays. As each line card communicates directly to the backplane, a primary to secondary switch occurs in a minimal amount of time with little traffic disruption. This application note will provide some guidelines for implementing redundancy for both T1 and E1 operation using the IDT82V2044 (Quad T1/E1 LIU), IDT82V2048 (Octal T1/E1 LIU), IDT82V2048L (Octal T1/E1 AFE), IDT82V2054 (Quad E1 LIU), IDT82V2058 (Octal E1 LIU), IDT82V2058L (Octal E1 AFE). This application note will focus on IDT82V2048. All items dicussed about the IDT82V2048 will also apply to all other products covered in this document.

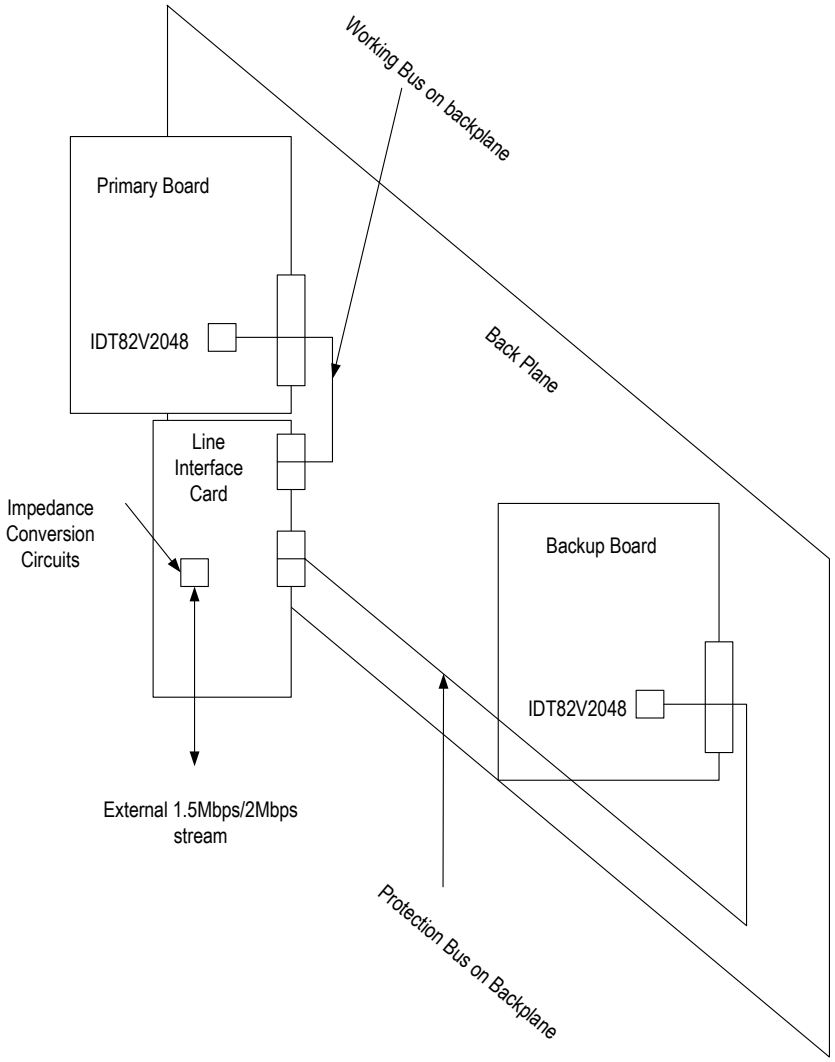

Figure 1 Coarse description of protection structure

November 2004

Figure 1 presents the typical architecture found in most T1/E1 systems with redundancy protection. This approach is common in rack based systems where several boards share a common backplane. The primary and backup boards are similar or same in function and access the same basic data signals. A separate Line Interface Card (LIC) includes the connectors and metallics that can be shared among the primary and backup boards. The common LIC approach reduces the cost in the primary and backup boards by reducing the number of components duplicated in these cards. It also offers a simple mechanical solution for supporting several connector options and different line impedances (T1 100 and E1 120/75). An independent control board supervises the system operation and determines which board (primary or backup) is being used. Naturally, depending on the equipment functionality, other boards may also exist.

In normal operation, the primary board is actively transmitting and receiving T1 or E1 signals. In this state, the backup board will be in standby mode with a minimum number of circuits activated. In the event of failure in the primary board, the control board will place it in standby mode and activate the backup board.

In a redundancy protection implementation it is crucial to ensure that the backup board does not load or alter the T1/E1 signal in the primary board. The fundamental electrical performance requirements such as pulse shaping receive sensitivity and return loss must still be met. In addition, switching between primary and backup board must be as fast as possible in order to minimize the number of bit errors.

As it will be shown in the following paragraphs, the IDT82V2044/48/48L and the IDT82V2054/58/58L will ease the design of redundancy protection implementations and guarantee excellent T1/E1 analog performance and minimize the switching time and associated number of bit errors.

2.0 PROTECTED STRUCTURE

The following features included in IDT82V2044/48/48L and IDT82V2054/58/58L ease the development of redundant protection systems:

1. Output tristating by freezing the TCLK signal
2. Fast output tristating by using the OE pin
3. Software controllable output driver tristate by using the OER register
4. High receiver input impedance of 70 K typ
5. Constant delay jitter attenuator

The driver tristate feature allows the designer to connect the protection driver output in parallel with the working driver output when one of them is tristated. Similarly, because the receiver impedance is very high, two receivers can be connected in parallel.

The constant delay jitter attenuator guarantees that, if a few conditions are met, the throughput delay in the primary and backup boards will be closely matched. This means that the number of bit errors resulting from switching boards will be minimized.

In the following paragraphs we will suggest solutions for the line interface circuit design using the IDT82V2044/48/48L and the IDT82V2054/58/58L.

For equipment protection purposes, T1/E1 signals passing through Line Interface Card I interface connectors should be extracted/inserted either from/to a primary Board or from/to the backup board (see **Figure 1**).

This solution protects against primary or backup unit failures or removal. However, it does not protected against hardware failures on the Line Interface Card (LIC).

2.1 RECEIVE LINE INTERFACE

Figure 2 shows the recommended receive configuration for redundancy protection. For simplicity, only one channel is represented.

The LIC (Line Interface Card) contains the receive 1:2 transformer TV1 is a transient voltage suppressor. This device is recommended when there are stringent surge immunity requirements. In the primary and backup boards the series 1K resistors at the RTIP/RRING inputs further improve the surge and ESD immunity by decreasing the current coupled into the device.

Primary and backup boards are connected together in the backplane and are capacitively coupled. Because of the high receiver input impedance, the backup board will not interfere with the primary board operation. **Table 1** lists the components that were used in our tests for 100ohm T1 twisted pair, 120ohm E1 twisted pair and 75ohm E1 coaxial.

2.2 TRANSMIT LINE INTERFACE

Figure 3 represents the recommended transmit interface. The LIC contains the transmit transformer and 560 pF capacitor shared between the primary and backup boards. It also includes a first level of surge protection in the form of TV2. This protection is complemented by the Schottky diodes D1-D8 in each board.

Primary and backup boards are connected in the backplane and are capacitively coupled. When tristated, the output driver impedance in the backup board is very high and will not affect the pulse shaping in the primary board.

Table 2 lists the components that were used in our tests for 100ohm T1 twisted pair, 120ohm E1 twisted pair and 75ohm E1 coaxial.

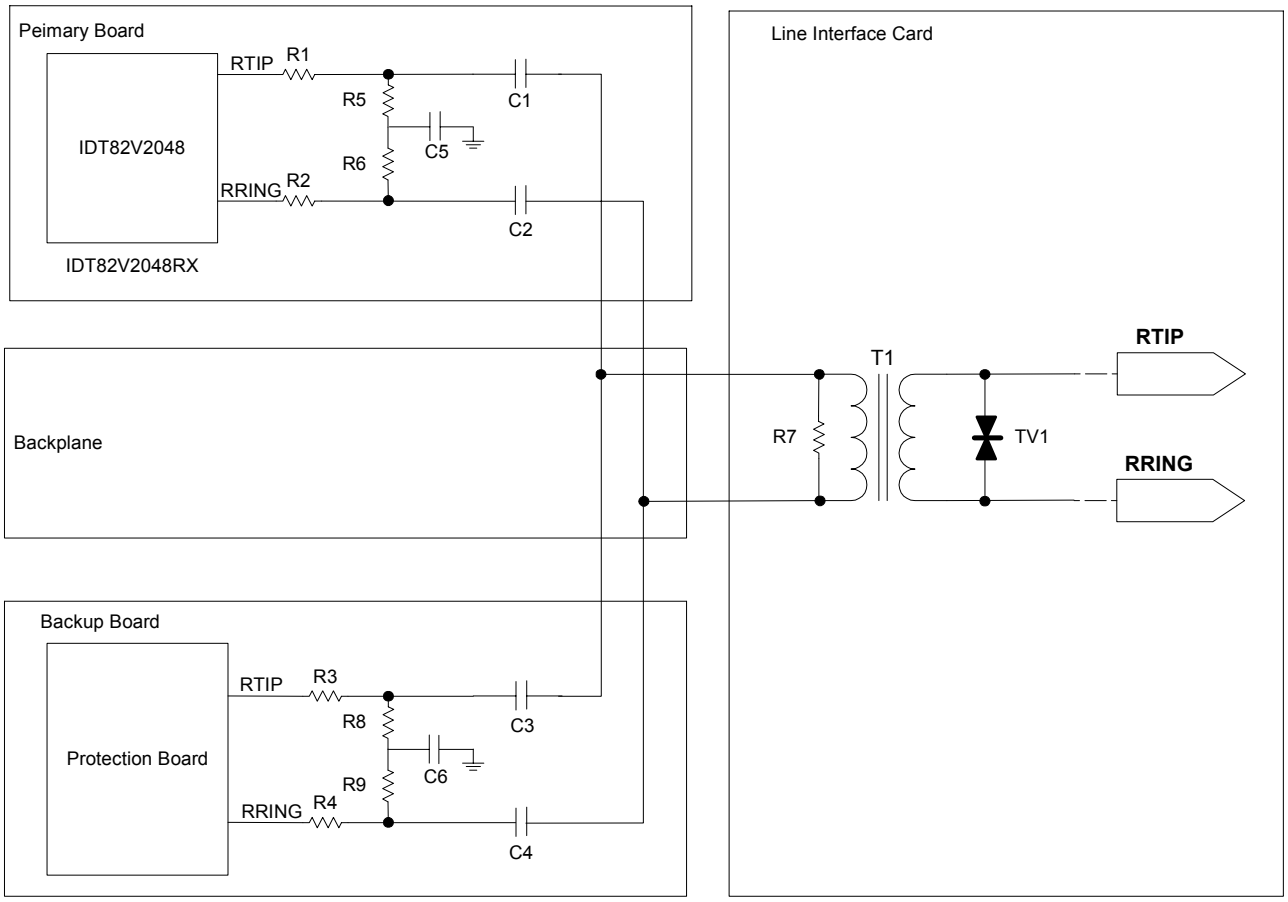

Figure 2 IDT82V2048 Receive Interface Circuit

Table 1 Receive Line Interface Component List

Component	E1		T1
	Coax Cable	Twisted Pair	
TV1	LC03-6, Semtech (or equivalent)		
T1	1:2 T1124, PULSE (or equivalent)		
R1, R2, R3, R4	1KΩ ± 1%		
R7	19.6Ω ± 1%	32.4Ω ± 1%	26.1 Ω ± 1%
R5, R6, R8, R9	470Ω		
C5, C6	0.22μF		
C1, C2, C3, C4	0.47μF		

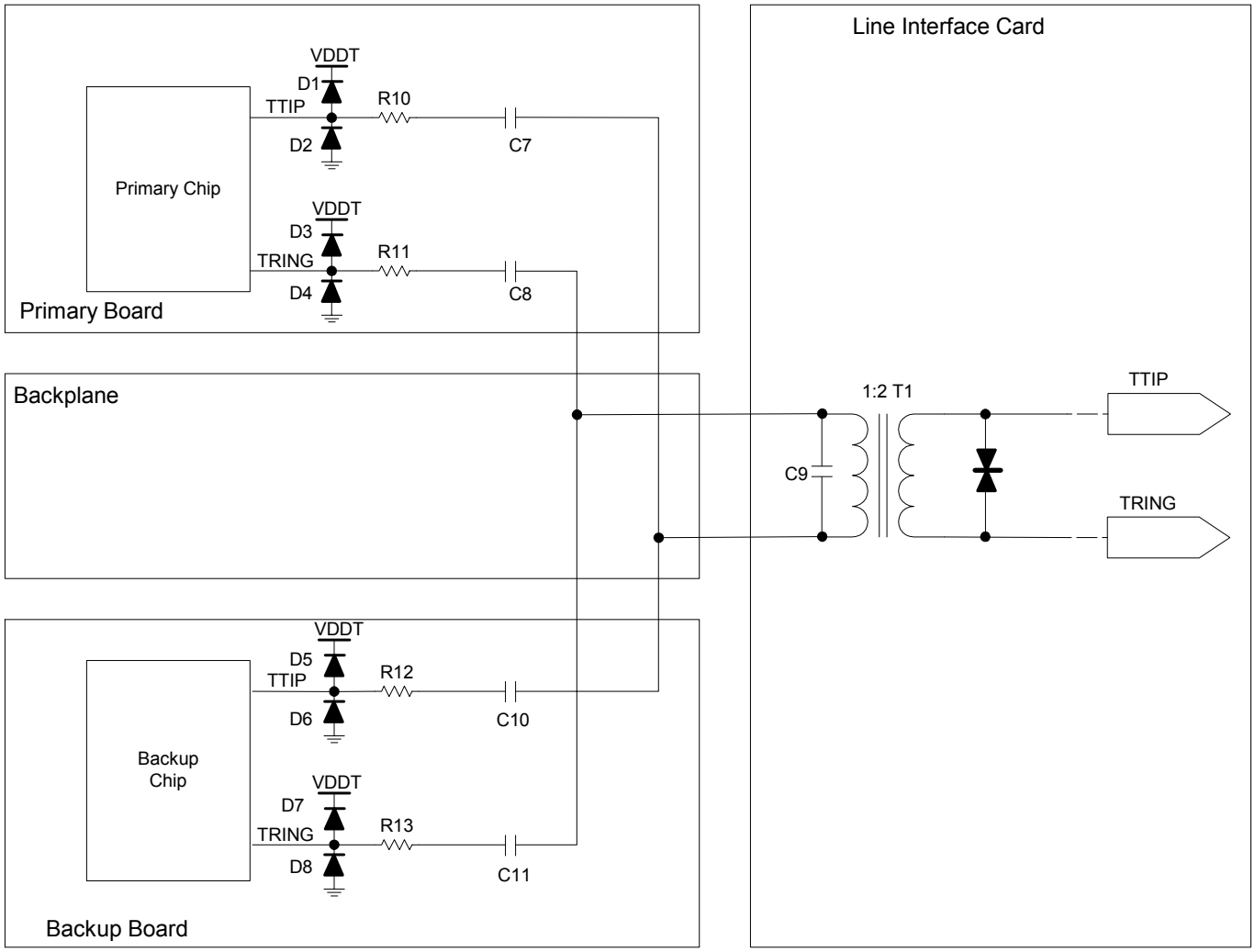

Figure 3 IDT82V2048 Transmit Interface Circuit

Table 2 Transmit Line Interface Component List

Component	E1		T1
	Coax Cable	Twisted Pair	VDDT=5V
TV2	LC03-6, Semtech (or equivalent)		
T1	1:2 T1124, PULSE (or equivalent)		
C9	2200pf		
C7, C8, C10, C11	0.47μF		
R10, R11, R12, R13	9.5Ω ± 1%	9.5Ω ± 1%	9.1Ω ± 1%
D1-D8	Nihon Inter Electronics - EP05Q03L, 11EQS03L,EC10QS04,EC10QS03L; MOTOROLA - MBR0540T1 (or equivalent)		

2.3 DESIGN CONSIDERATIONS

2.3.1 Minimize Trace/Cable Lengths

As cable and trance lengths reduce output amplitude care should be taken minimize where possible. In the experiments that were conducted, the cable connecting the primary, backup and LIC boards did not exceed 25cm. If longer cables are required, the transmit series resistors R10 - R13 can be reduced to increase the amplitude and compensate for the amplitude loss through the cables and traces.

2.3.2 Minimize Parasitic Capacitance

Long cable lengths, long leaded components or poorly selected protection components all have high parasitic capacitance, which will affect both return loss performance and pulse shaping. As result components which have a very low capacitance at the nominal operating voltage should be chosen. In some cases, the transmit capacitor C9 may have to be adjusted to optimize pulse shaping and transmit return loss performance.

2.3.3 Surge Immunity

The protection elements recommended in **Figure 2** and **Figure 3** are sufficient for compliance with IEC 1000-4-5 (EN-6100-4-5) with up to 24A peak current on a 1.2/50 μs surge. If additional protection is required, a different line TVS may be necessary.

2.3.4 Place the TVS Close to the Connector

If a surge elements such as a TVS is required, it should be placed as close as possible to the connector or disturbance source.

2.3.5 Include TVS Protection in the Power Supply

In addition to protection diodes D1-D8, which will couple current to the power supply in the event of a lightning surge, a 3.3V TVS should be included in the power supply. This will protect other circuits on the board.

2.3.6 Avoid Crossing Transmit and Receive Signals

As a general design rule, routing digital signals near analog signals may cause coupling and cross-talk. At the receiver input, this is especially important as cross-talk here may induce bit errors.

2.3.7 EMI Filtering

Some designs may require EMI filtering depending on the applicable emissions standards, total number of ports and shielding strategy. In these applications, common mode chokes may be added near the connectors.

2.3.8 Defect Detectors and Protection Switch Requests (PSRs)

Failure condition related information coming from the primary/backup Board or from other boards (such as the framer boards or cross connect Board etc.) When a related defect (such as primary board functional fail or primary board removal (absence)) is reported and correlated by the SW fault subsystem as a valid PSR (Protection Switch Requests), switch commands will be sent, then correspond traffics will be switched for primary board to backup board.

2.3.9 Switch Performance

Switch performance dependence on time duration to complete the switch and traffic interruption interval.

2.4 HITLESS PROTECTION SWITCHING (HPS)

The IDT's IDT82V2044/48/48L and IDT82V2054/58/58L includes a fast tristatability feature that allows switching between boards in less than 1 microsecond. So it can be used in Hitless Protection Switching networks to make switching event cause no frame synchronization loss in the equipment downstream. The following paragraphs show that HPS can be achieved using IDT's IDT82V2044/48/48L and IDT82V2054/58/58L.

2.4.1 Hitless Protection Switching Using IDT82V2044/48/48L & IDT82V2054/58/58L Test Setup

Figure 4 represents the setup used for hitless switching testing. A standard T1/E1 pattern generator/analyzer transmits a framed pseudo-random pattern (2^15-1 in E1, 2^20-1 in T1). Both the primary and the backup boards receive this pattern. A clock generator was used to provide MCLK references to the using IDT's IDT82V2044/48/48L and IDT82V2054/58/58L LIUs. One of the boards is kept active while the other board's driver is tristated (OE=Low). The "switching control" block, in this case a simple clock generator, determines which board is active at any given point in time. In order to obtain statistics on the number of bit errors caused by a switching event, the switching control block was set to generate a 1 Hz clock. This effectively generates 1 switching events per second.

The pattern analyzer was used to keep track of the number of bit errors and to verify frame synchronization status.

2.4.2 Test Conditions

- Input frequency range: +/- 50 ppm.
- MCLK frequency range: +/- 100 ppm.
- Room temperature.
- Nominal power supply voltage.
- Jitter attenuator is disabled in the IDT's IDT82V2044/48/48L and IDT82V2054/58/58L.
- Jitter added to the input signal.

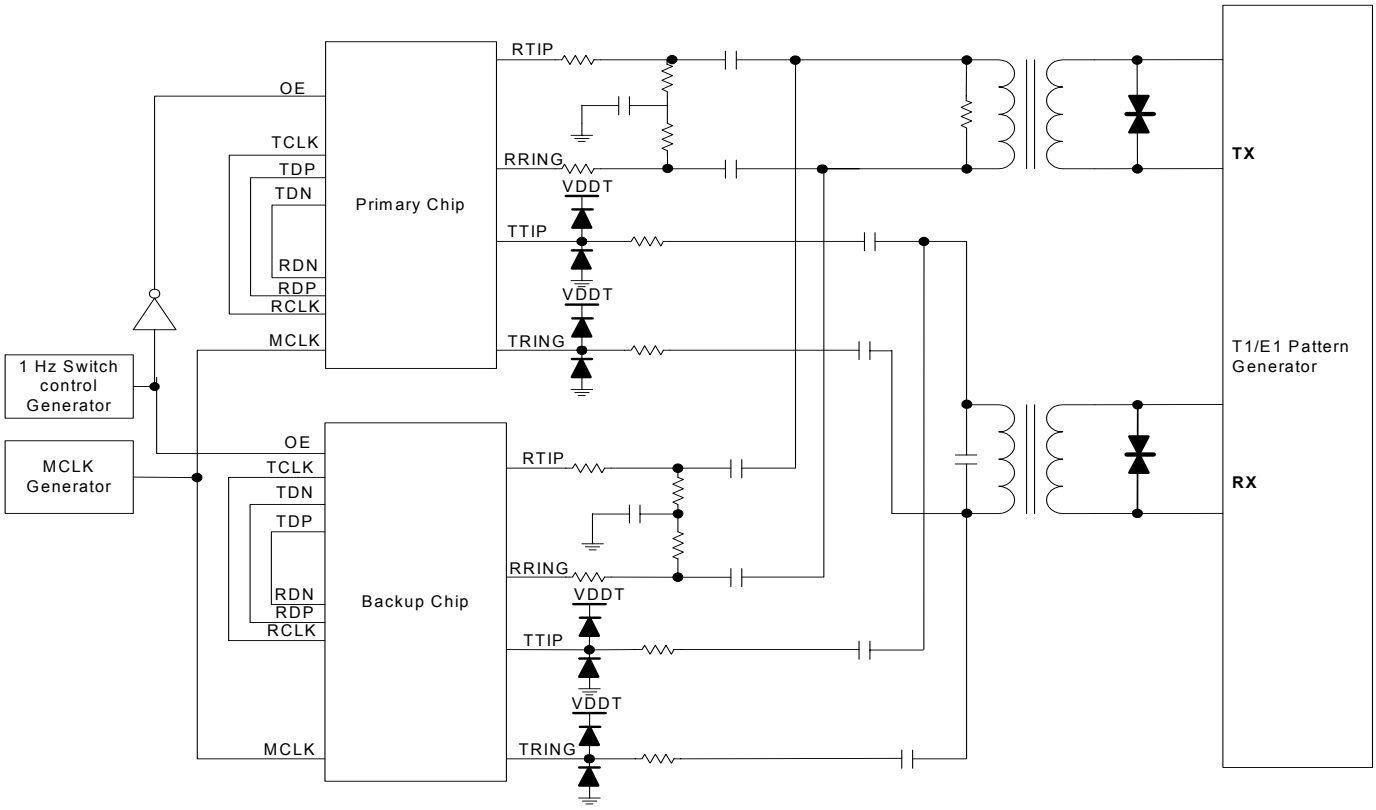

Figure 4 Hitless Switching Test Setup

3.0 TEST RESULTS

Standard frame synchronization algorithms require errors in two or more consecutive frame alignment words in order to declare loss of frame synchronization. Since the number of errors is limited to one, frame loss will not be declared.

The following results were obtained using the setup in **Figure 4** for both T1 and E1 operation:

- Maximum number of errors per switching event: 1 error.
- Probability of an error during a switching event: 50%.
- No frame synchronization loss.

The circuits in **Figure 2** and **Figure 3** were tested using the IDT82EBV2048 Evaluation board. The following performance parameters were tested for both coaxial and twisted pair cable where applicable:

- Receiver sensitivity per ITU-T G.703.
- Pulse template per ITU-T G.703.
- Receive return loss per ITU-T G.703.
- Transmit return loss per ETSI ETS 300 166.

3.1 RECEIVER SENSITIVITY

3.1.1 Test Result

The devices were able to correctly recover data with cable attenuation up to 12 dB at 772 KHz for T1 and 1024 KHz for E1. For T1, this figure exceeds the requirements in ANSI T1.102 of 3 dB (655 feet of cable) at 772 KHz. For E1, the figure exceeds the 6 dB minimum limit set (at 1024KHz) by ITU-T G.703.

3.2 PULSE TEMPLATE

3.2.1 E1 Mode

3.2.1.1 Requirements

Figure 5 represent the output pulses obtained for twisted pair.
Figure 6 represent the output pulses obtained for coaxial cable.

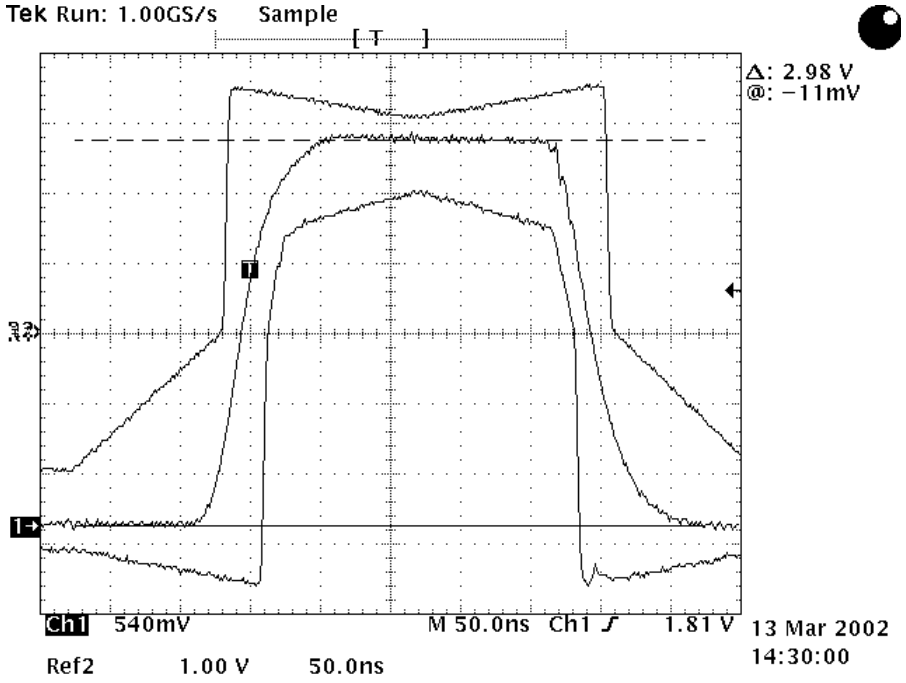

Figure 5 E1 Twisted Pair Cable Output

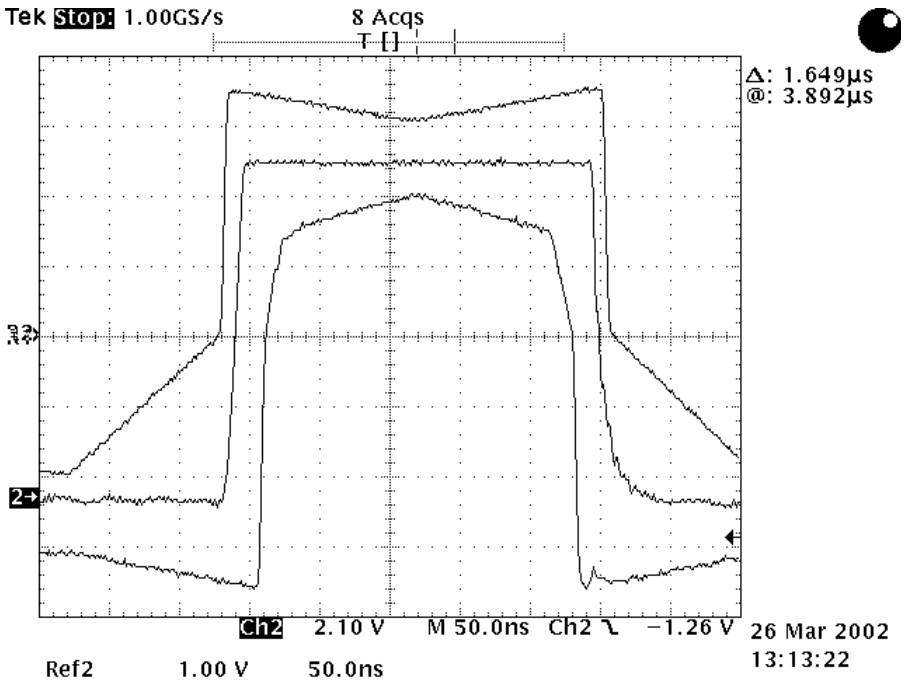

Figure 6 E1 Coaxial Cable Output

3.2.1 T1 Mode

Figure 7 shows T1 output pulse.

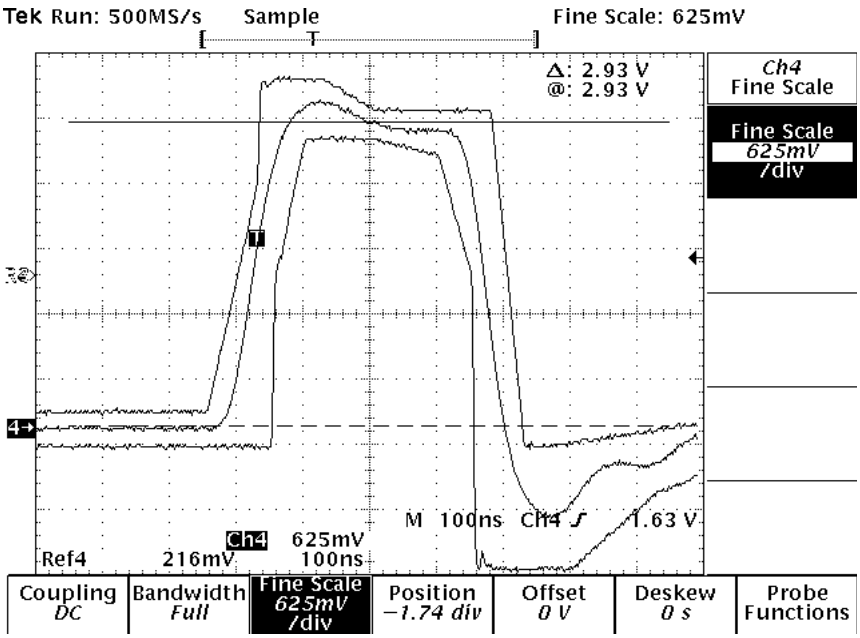

Figure 7 T1 Output Pulse

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