Connecting RC32355 TDM Interface to I²S Interface

Notes

By Fred Santilo

Revision History

February 11, 2001: Initial publication.

Background

The RC32355 is an integrated processor that combines a 32-MIPS instruction set (ISA) CPU core with a number of on-chip peripherals to enable direct connection to boot memory, main memory, IO, and PCI. The RC32355 also includes system logic for DMA, reset, interrupts, timers, and UART. The RC32355 integrates all of the peripherals commonly associated with an embedded system to reduce real estate board consumption, design time, and system cost.

This application note describes the operation of the RC32355 Time Division Multiplexing (TDM) interface, how to connect the TDM interface to an audio device that supports the Inter-IC Sound (I^2S) specification, and how to configure the TDM registers.

RC32355 TDM Interface

The RC32355 incorporates a highly configurable TDM interface that is suitable to be used with interfaces supporting protocols other than TDM, such as I^2S. The transmit and receive directions of the RC32355 TDM interface are programmed individually and do not need to be configured in the same manner. In most cases, some amount of external logic is required to reshape particular signals of the TDM transmit and receive protocol to match that of the device being connected to the TDM interface, such as an Audio DAC device that supports the I^2S specification.

The standard form of the TDM protocol is similar for both the transmit and receive directions; both transmit and receive are referenced from the RC32355. All transmit and receive timing parameters are specified with respect to the TDMCLKP. Data is transferred in time slot frames, with each time slot frame being a multiple of 8-bits and having a value between 8-bits and 128-bits.

The TDM interface is comprised of five signal pins and fourteen 32-bit registers, which are described below. A detailed description of all the RC32355 registers can be obtained in the RC32355 User Reference Manual, and a detailed description of all the RC32355 signal pins can be found in the RC32355 Data Sheet.

TDM Interface Signal Pins

TDM Bus Clock (TDMCLK) controls the rate at which data is transmitted and received on the TDM interface. TDM Transmit Bus Enable (TDMTEN) is an active low transmit buffer enable which is asserted by the RC32355 when data is transmitted on the TDM bus. This signal is typically used to control an external buffer when multiple devices are connected to a single TDM interface. TDM Frame Pulse (TDMFP) marks the beginning of the TDM frame and asserts for one TDMCLK period prior to the start of a TDM frame. It asserts one TDMCLKP edge prior to the TDMCLKP edge it is sampled on.

TDM Data Out (TDMDOP) is a tri-stateable serial output data signal. The TDMDOP signal is active when the RC32355 is transmitting data on the TDM bus and is tri-stated when the RC32355 is not transmitting data on the TDM bus. The TDMDOP and TDMDIP can be tied together when connected to a device that has a bi-directional serial data bus. TDM Data In (TDMDIP) is a serial input data signal. The TDMDIP signal is active when the RC32355 is receiving data from a device.

Notes

TDM Registers

The TDM Bus Control (TDMC) register is one of the 32-bit registers used to configure the RC32355 TDM interface.

- The Enable (EN) bit is used to enable the TDM interface. When this bit is set to zero, the interface is disabled, and when it is set to one, the interface is enabled. The EN bit must be set to disable in order to initialize and configure the TDMC register.
- The Clock Mode Select (CMS) bit selects whether the TDMCLKP frequency is equal to, or twice, the frequency of the transmit data rate. When this bit set to zero, the TDMCLKP frequency equals the transmit data rate, and when it is set to one, the TDMCLKP frequency is twice the frequency of the transmit data rate.
- The Frame Master (FM) bit determines whether the RC32355 TDM interface is in Master mode or Slave mode. When this bit is set to zero, the interface is in Slave mode and the TDMFP signal is an input. When this bit is set to one, the TDM interface is in Master mode and the TDMFP signal is an output generated by the RC32355.
- The Frame Polarity (FP) bit determines whether the FP signal is delineated on the high to low transition or on the low to high transition. When this bit is set to zero, the TDMFP signal is delineated on the high to low transition, and when it is set to one, the TDMFP signal is delineated on the low to high transition.
- The Frame Edge (FE) bit selects whether the TDMFP signal is sampled by the RC32355 on the rising edge of TDMCLKP or the falling edge of TDMCLKP. The TDMFP is output one TDMCLKP edge prior to the TDMCLKP edge it is sampled on.
- The Transmit Bit Offset (XBOFF) field selects the fixed offset of TDMCLKP edges that the data will be output on TDMDOP, as referenced from the TDMFP signal. The offset value is a function of the FE and XCE fields of this register.
- The Transmit Clock Edge (XCE) bit selects whether or not the data will be transmitted by the RC32355 on the rising or falling edge of the TDMCLKP.
- The Receive Bit Offset (RBOFF) field selects the fixed offset of TDMCLKP edges that the data will be input on TDMDIP, as referenced from the TDMFP signal. The offset value is a function of the FE and RCE fields of this register.
- The Receive Clock edge (RCE) bit selects whether data will be sampled by the RC32355 on the rising or falling edge of the TDMCLKP.
- The Time Slots (TSLOTS) field encodes the number of time slots on the TDM interface. Valid values are from 1 to 128.
- The DMA Burst Size (DMABS) field encodes the number of bytes transferred during a DMA transfer. Valid options are one byte (8-bits), one word (32-bits), two words (64-bits), or four words (128-bits).

The TDM Bus Status (TDMS) register provides information about each TDM time slot and can be used to generate interrupts if enabled. The TDM Bus Status Mask (TDMSM) register is used to mask corresponding bits of the TDMS register. When the mask bit is set to one, the corresponding status bit is masked from generating an interrupt, and when it is set to zero, the bit is not masked from generating an interrupt.

The TDM Bus GPIO Pin Control (TDMPC) register allows the four TDM signals to be used as general purpose I/O signals when the TDM interface is disabled. The TDM Bus Output Selector (TDMOSS[3:0]) registers are used to enable each time slot for transmission. The TDM Bus Input Selector (TDMISS[3:0]) registers are used to enable each time slot for reception. The TDM Bus Input Data (TDMID) register is used to read a byte of data from the TDM input FIFO. The TDM Bus Output Data (TDMID) register is used to write a byte of data to the TDM output FIFO.

TDM Transmit Data Flow

In the transmit direction TDMFP indicates the start of the TDM time slot frame. TDMTEN asserts low on the same TDMCLKP cycle as the first bit of transmit data. TDMTEN is typically used to control an output buffer when there are multiple devices connected to a single RC32355; it is not required when the RC32355 is connected to a single device. TDMDOP outputs the first bit of valid data on the same TDMCLKP cycle that TDMTEN asserts low. Additional data for the current time slot is valid on subsequent sampled edges of the TDMCLKP. See Figure 1 for a typical transmit data timing diagram which illustrates one of the many possible configurations.

Notes

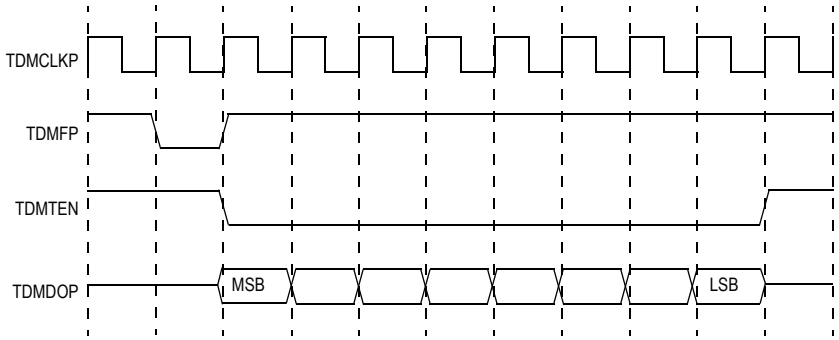

Figure 1 Typical TDM Transmit Data Timing

TDM Receive Data Flow

In the receive direction, TDMFP indicates the start of the TDM time slot frame, which asserts either in conjunction with or prior to the first bit of valid data. Additional data for the current time slot on the TDMDIP signal is valid on subsequent sampled edges of the TDMCLKP. See Figure 2 for a typical receive data timing diagram which illustrates one of the many possible configurations.

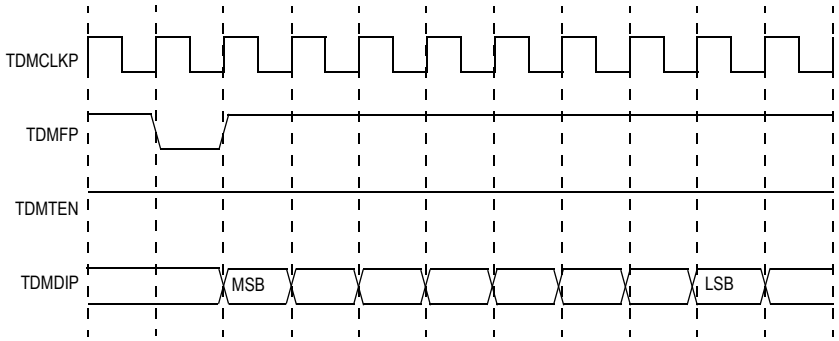

Figure 2 Typical TDM Receive Data Timing

I^2S Interface

The I^2S interface is a standardized interface and protocol used by many audio devices. It was developed specifically for digital audio. The interface consists of three signals (SCK, WS, and SD) which are described below. In its most basic form the protocol requires a transmitter and a receiver, with either the transmitter or receiver acting as a master. In more complex designs, there may be a transmitter or receiver acting as a master to several devices, or there may be a dedicated controller which is neither a transmitter nor a receiver, acting as the master to several devices that are transmitters and receivers. Only the basic configuration of the transmitter acting as a master to the receiver will be discussed in this document. A detailed description of all possible configurations and timing parameters can be obtained in the I^2S Bus Specification.

I^2S Interface Signal Pins

Serial Clock (SCK) is a continuous serial clock provided by the master device. All timing is derived from this clock.

Notes

Word Select (WS) indicates which channel is being transmitted to and is provided by the master device. When WS is a logical zero data is being transmitted to the left channel, while WS being a logical one indicates data is being transmitted to the right channel.

Serial Data (SD) is a bi-directional serial data bus used to transmit and receive data.

I²S Transmit Data Flow

Serial data is transmitted in two's compliment format with the MSB being transmitted first. Data can be synchronized to be output on the positive or negative edge of SCK. WS transitions one SCK cycle prior to the first bit of valid data (MSB). Refer to Figure 3.

I²S Receive Data Flow

Serial data is received in two's compliment format with the MSB being received first. Data is sampled by the receiving device on the positive edge of SCK. WS transitions one SCK cycle prior to the first bit of valid data (MSB). Refer to Figure 3.

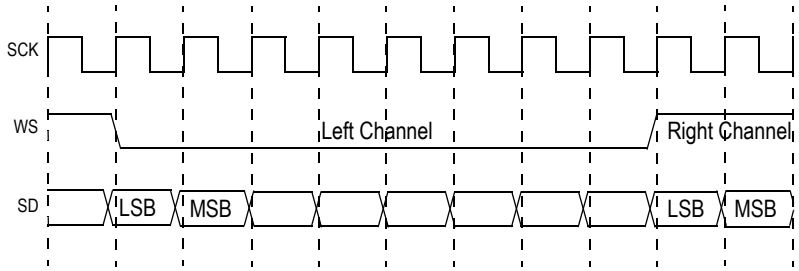

Figure 3 I²S Transmit and Receive Data Timing

TDM to I²S Example

This example assumes the user is already familiar with both the RC32355 and CS43L42 Stereo DAC so that only the signal pin connections, timing parameters, and register configurations of the TDM and I²S interfaces will be described. Audio data will be transferred in the transmit direction only, which is from the RC32355 (I²S Transmitter) to the CS43L42 (I²S Receiver). The RC32355 will be configured as a master device, thus providing the WS signal to the CS43L42. The RC32355 TDMCLKP signal is configured to equal the RC32355 data transmission rate. The TDMTEN signal is not required since there is only one device connected to the RC32355. Data will be transferred in 8-bit frames.

This example also assumes that either software or a DSP will provide the RC32355 with the appropriate left and right channel data in the proper sequence.

Signal Pin Connection

To maintain the I²S protocol, a D-Type Flip-Flop, such as an IDT74LVC74A, needs to be incorporated between the TDMFP and the WS signals, as shown in Figure 4. This, along with the correct TDM register configuration, will reshape the TDMFP signal output of the RC32355 to meet the timing requirements of the I²S specification. The TDMCLKP signal of the RC32355 is directly connected to the LRCLK signal of the CS43L42 and to an oscillator that has a frequency of 64KHz. The TDMDOP and TDMDIP signals of the RC32355 are tied together, and they are directly connected to the SDATA signal of the CS43L42.

> **Note:** An alternative to this example would be to connect the TDMDOP signal to the SDATA signal and connect a pull up or pull down resistor to the TDMDIP signal.

The TDMFP signal is connected to the Clock input of the 74LVC74A. The D input of the 74LVC74A is connected to the $\overline{Q}$ output of the 74LVC74A. The Q output of the 74LVC74A is connected to the WS input signal of the CS43L42. The $\overline{CLR}$ input signal of the 74LVC74A is connected to the System Reset signal and

Notes

the $\overline{PRE}$ signal is connected to a pull up resistor. This will guarantee the Q output to be a logical zero and the $\overline{Q}$ output to be a logical one after reset and prior to the first low to high transition on the 74LVC74A clock signal. This post reset state will determine whether the left or right channel is the first active channel. Once the RC32355 asserts TDMFP with the first actual frame of valid data, the opposite channel will be selected. Thus, the initial channel selected after a reset condition will not be the first channel to receive valid data. Note that the and signals may be swapped to select the opposite state after reset.

The CP/$\overline{SA}$, SDA/CDIN/DIF0, SCL/CCLK/DIF1, and AD0/$\overline{CS}$/DEMO signals of the CS43L42 are each connected to a separate General Purpose I/O (GPIO) signal pin of the RC32355. The $\overline{RST}$ signal of the CS43L42 is connected to the system reset.

RC32355 Register Configuration

The TDM registers are initialized with the values shown below. Once all register values are written, the EN bit of the TDMC register can be set to a one to enable the TDM interface.

The TDMC register is initialized as follows:

- EN = 0. This enables bits[24:1] of the TDMC register to be written to, and it disables the TDM interface from normal operation.
- CMS = 0. This sets the frequency of the TDMCLKP to be equal to the data transmission rate.
- FM = 1. This sets the RC32355 as the Master, which will generate the TDMFP signal.
- FP = 0. This synchronizes the TDMFP delineation to a high to low transition.
- FE = 1. This sets TDMFP to be sampled on the positive edge of TDMCLKP.
- XBOFF = 0x1. This sets the transmit fixed offset to be three TDMCLKP edges.
- XCE = 0. This sets transmit data to be output on the falling edge of TDMCLKP.
- RBOFF = 0x0. This field is not required for this example, but it must be set to a valid value.
- RCE = 0. This field is not required for this example, but it must be set to a valid value.
- TSLOTS = 0x00. This sets the number of time slots to one, or 8-bits.
- DMABS = 0x0. This sets the DMA Burst Size to one byte, or 8-bits.

The TDMSM register is initialized to a value of 0x00000000, which does not mask any of the possible interrupts. The TDMPC register is initialized to a value 0x00000000 and is not used in this example. The TDMOSS[3:0] and TDMISS[3:0] registers are not used in this example.

CS43L42 Configuration

The Control Port Interface of the CS43L42 provides read/write access to its internal registers. This connection is required for this example in order to clear the PDN bit in the Power and Muting Control register (addr 0x01) of the CS43L42, which places the CS43L42 in normal operational mode. The CS3L42 Control Port Interface is shown connected for Two-Wire mode of operation, thus the AD0/$\overline{CS}$ signal is tied to Ground.

The CS43L42 is configured for Stand Alone mode of operation and to use the Digital Interface Format (DIF) of 0x00, which is the I^2S format. The Mode Control 2 register is initialized with a value of 0x00. MCLK has a frequency of 8.192MHz and is configured to be 128 times the frequency of SCLK. LRCLK has a frequency of 64KHz.

Other CS43L42 registers not mentioned are design specific and are not explained in this document. However, they must contain valid values for normal operation. Refer to the CS43L42 data sheet for a detailed description of all internal registers and the proper procedure to access the registers via the Control Port Interface.

Notes

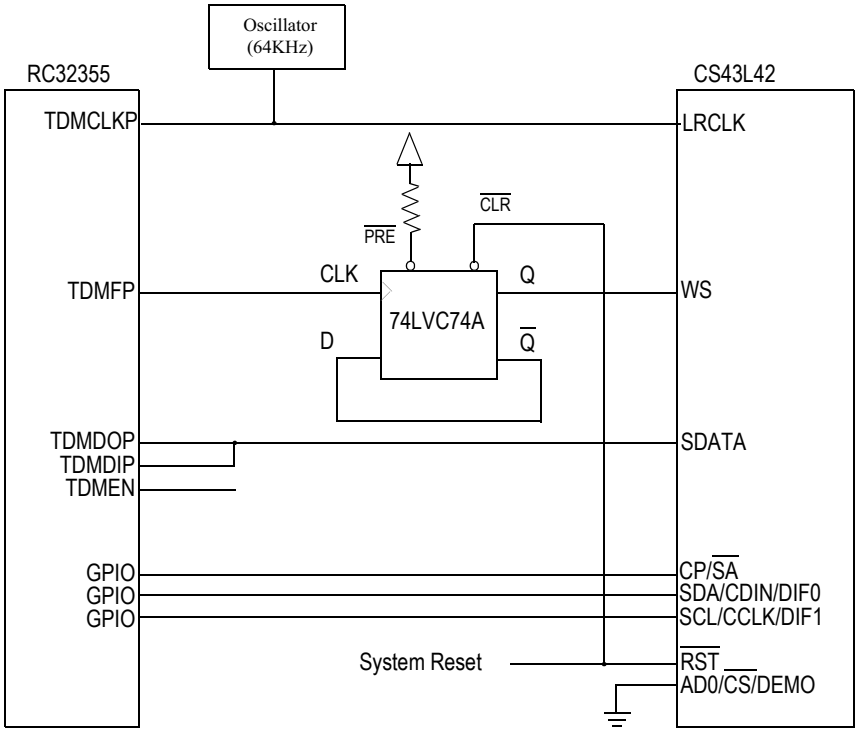

Figure 4 TDM to I²S Block Diagram

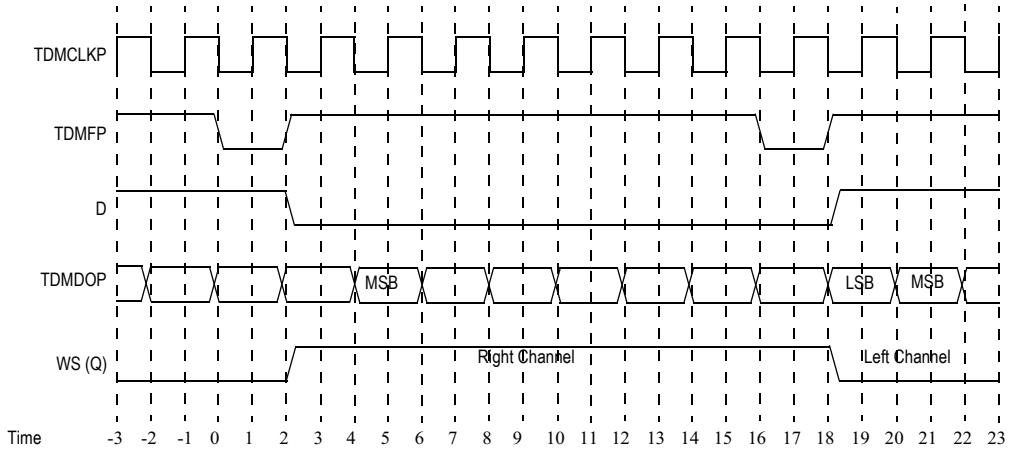

Figure 5 TDM to I²S Timing Waveform

Example Data Flow

Figure 5 illustrates the operation of an 8-bit data transfer from the RC32355 to the CS43L42.

At time 0, the TDMFP signal asserts from high to low on the falling edge of TDMCLKP. The D input and $\overline{Q}$ output of the 74LVC74A are a logical one and the WS input and Q output signals are a logical zero.

Notes

At time 1, the TDMFP signal is a logical zero.

At time 2, the D input of the 74LVC74A is latched and propagated to the Q and $\overline{Q}$ outputs of the 74LVC74A and the WS input. The TDMFP signal changes from low to high.

At time 3, the WS and Q output are a logical one, and the D input and $\overline{Q}$ output are a logical zero. The MSB of data for the new frame is not output by the RC32355 since the XOFF value is set for a three clock edge offset from TDMFP at time 1. The WS signal is sampled by the CS43L42.

At time 4, the MSB of data for the right channel frame is output by the RC32355.

At time 5, the MSB of data for the right channel is sampled by the CS43L42.

At time 6, the MSB-1 of data for the right channel is output by the RC32355.

At time 7, the MSB-1 of data for the right channel is sampled by the CS43L42.

At time 8, the MSB-2 of data for the right channel is output by the RC32355.

At time 9, the MSB-2 of data for the right channel is sampled by the CS43L42.

At time 10, the MSB-3 of data for the right channel is output by the RC32355.

At time 11, the MSB-3 of data for the right channel is sampled by the CS43L42

At time 12, the MSB-4 of data for the right channel is output by the RC32355.

At time 13, the MSB-4 of data for the right channel is sampled by the CS43L42.

At time 14, the MSB-5 of data for the right channel is output by the RC32355.

At time 15, the MSB-5 of data for the right channel is sampled by the CS43L42.

At time 16, the MSB-6 of data for the right channel is output by the RC32355. The TDMFP signal is asserted from high to low by the RC32355.

At time 17, the MSB-6 of data for the right channel is sampled by the CS43L42.

At time 18, the LSB of data for the right channel is output by the RC32355. The TDMFP signal asserts from low to high. The D input and $\overline{Q}$ output change to a logical one and the Q output and WS signals change to a logical zero.

At time 19, the LSB of data for the right channel is sampled by the CS43L42. The high to low transition of the WS signal is detected by the CS43L42, which indicates the end of the right channel data transfer.

At time 20, the MSB of data for the left channel is output by the RC32355 and the 8-bit transfer process repeats for the left channel.

Conclusion

The high degree of flexibility offered by the RC32355 TDM interface allows it to be used as the audio data interface with audio devices that support protocols other than the TDM protocol.

References

IDT 79RC32355 User Reference Manual

IDT 79RC32355 Data Sheet

IDT 74LVC74A Data Sheet

I^2S Bus Specification

Cirrus Logic CS43L42 Data Sheet

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.