Q1. What controls the Programmable Clock 5V9885 VCO operating frequency?

A1. The VCO frequency is controlled by the input frequency, the input divider, and the feedback divider.

$$\text{Fout} = \frac{Fref \cdot \frac{M}{D}}{\text{V}}$$

To program the device, the user would have to determine D, M, and V such that the desired output frequency is generated. Then the user has to use the equations in the table to determine N, A, and Q. The N, A, and Q are values that should be written into the registers. Our software will make this process effortless and easy.

	M	V
PLL0	$M = \begin{cases} 2.N, if A=0 \\ 2.N+A+1, if A>0 \end{cases}$	V = 2*P(1)
PLL1	$M = \begin{cases} 2.N, if A=0 \\ 2.N+A+1, if A>0 \end{cases}$	V = 2*P(1)
PLL2	M = N	V = 2*P(1)

NOTE:
1. P can be disabled, div/1, div/2, or Q + 2.

Q2. Can the 5V9885 be put in a JTAG chain with FPGAs?

A2. Yes. Please note that the 5V9885 JTAG pins are not dedicated. TDO, for example, doubles as PLL_LOCK. Make sure the mode of operation is set properly when using these dual-use pins.

Q3. How long does it take to execute the restore and save instructions?

A3. It takes less than 5ms (128bytes x 8bits/byte x 1/300kHz + overhead).

Q4. What should I do with unused outputs?

A4. The unused outputs can be powered down with the OS (Address 0x1D) bits, tristated, or disabled with the OE (Address 0x1C) bits. The outputs can also be disabled by disabling the output divider, set Q =0.

Q5. What happens to the I/Os during programming?

A5. The clock outputs are unaffected. During programming, the I/Os will revert to their I^2C or JTAG programming mode as appropriate, and will be enabled if required (eg: if GIN0 is disabled, it will be enabled when entering I^2C mode). The state of GIN[4:0] will be latched when entering programming mode, in order not to disturb the configuration select.

Q6. What happens if the reference frequency is removed?

A6. If you are in Auto-revertive or Auto-non-revertive modes, the alternate clock source will be selected. If both XTAL & CLKIN are removed, or the selected clock source is removed in manual switchover mode, the outputs will slew down to the minimum VCO frequency.

Q7. What models are available for 5V9885?

A7. There are IBIS and HSPICE models for inputs and outputs, and JTAG and BSDL files for boundary-scan.

Q8. Is it possible to re-program 5V9885 on the fly without affecting EEPROM contents?

A8. Yes. All programming is done direct to RAM. You must issue a separate command to write to the EEPROM.

Q9. What would be the impact on the outputs (glitch, phase offset, stabilization) if the 5V9885 was to be re-programmed on the fly?
A9. Programming the currently-used input, feedback or output dividers may result in a glitch. The minimum glitch width would be the VCO period*2. Programming loop filter parameters may result in a momentarily unstable loop. This is unlikely to cause loss of frequency lock, but may cause a phase jump. It is safer to program an unused configuration and then switch to it using the GIN/Frequency control pins.

Q10. Is there a SVF file provided for JTAG programming?
A10. Yes. The IDT Software Kit can generate SVF files.

Q11. What is the maximum period deviation during a switchover?
A11. There is no set maximum. The device will slew to the new clock frequency during switchover. The frequency slew rate and characteristic (eg: overshoot) will depend on the loop filter parameters.

Q12. Can I read data from the EEPROM, or simply get the data through the chip with the instruction register BYPASS?
A12. No to both.

Q14. Can the JTAG clock run at a frequency other than 10MHz?
A14. Yes. Any frequency that is less than 10MHz is okay. Note that decreasing the JTAG clock frequency will increase the time it takes to program the part using JTAG.

Q15. What are the sequence of events during power-up?
A15. The events are as following:
- Device performs internal POR (Power-On Reset)
- EEPROM contents loaded and CRC checked
- PLLs powered up

Q16. What are the sequences of events after re-programming?
A16. Reprogramming is active. For example, new register contents are used immediately. There is no reset or initialization performed.

Q17. When the device is busy executing an I^2C command, and more commands are issued to it, what happens to those new commands?
A17. When the device is not finished with executing an I^2C command, the device will not issue an acknowledgement. Consequently, the I^2C master should not be issuing more commands. If the I^2C master does issue more commands without receiving an acknowledgement of the previous command, then those new commands are lost. Note that the I^2C busy is held "busy" while the device is executing the commands. PROGSAVE or PROGRESTORE are the commands that take any significant amount of time to execute.

Q18. Which programming bits will cause glitches on the outputs?
A18. Programming any of the output dividers, feedback dividers, and input dividers may cause glitches on the outputs. Glitches (min width 2xVCO period) may also be caused if the output dividers are reprogrammed. Reprogramming input divider or feedback dividers (also loop filter parameters) may momentarily generate an unstable loop, which may be seen as a loss of lock. The VCO frequency rate of change will still be limited by Ip/Rz/Cz, so while the output will not glitch, it may slew beyond the desired frequency before relocking.

Q19. What comes out of the part on powerup before the customer programs it for the first time?
A19. A default RAM table is in the datasheet.

Q20. What type of I²C connector and cable is used for the evaluation board and programmer kit?

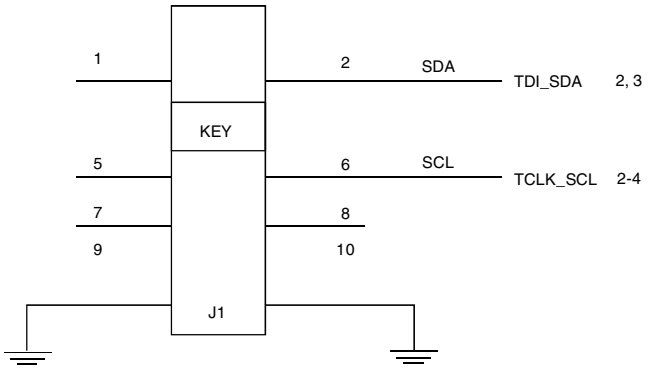
A20. Part Number:

IDT STG Library Part Number: 52-492-000

MEC1-105-02-S-D-LC (CONN,SM,2 x 5,Edge-Card Skt,1.0mm PT,STR)

Drawing:

http://www.samtec.com/ftppub/cpdf/MEC1-1XX-XX-X-D-XX-XX-MKT.pdf



Q21. Can the outputs OUT4* and OUT5* be configured as 3.3V LVTTL outputs with an option for them to be either inverted or non-inverted copies of their companion true output?

A21. Yes. In LVTTL mode, all the outputs (OUT1 to OUT6) can be individually inverted or non-inverted. For example, OUT4 and $\overline{OUT4}$ can be programmed to be synchronous or 180 degrees out of phase.

Q22. What the expected failure mode would be if t_{PU} (monotonic power up time for V_{DD}) was violated?

A22. For slow power-up (like 0.5V/ms), the part should still power on without trouble, as long as the supply is monotonic. If it is not monotonic (eg: rises slowly to something like 2V and then dips to 1V again), the EEPROM load sequence, which loads the internal registers with the values from EEPROM, can be corrupted. The user could run a PROGRESTORE command to ensure proper loading, or check the GOS1/LOSS_CLKIN pin. The pin will be asserted if there's a CRC error in the data loaded from the EEPROM. Note that the pin can also be asserted if there is a lost of CLKIN.

Q23. How should I set the crystal oscillator drive strength and capacitance?

A23. There are actually four XTAL drive strength settings: MAX/XTAL_IN, 3.2V, 2.3V, and 1.4V. When external clock on XTAL_IN is used, it will be necessary to set drive strength to MAX and load cap to min (3.5pF).

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