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April 1st, 2010
Renesas Electronics Corporation

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SH7137 Group

12-Bit A/D Converter: Example of Settings for Conversion in Single-Scan Mode

Introduction

This application note describes an example of settings for the 12-bit A/D converter in single-scan mode as an example of application of the A/D converter of the SH7137.

Target Device

SH7137

Contents

| | |
|--|----|
| 1. Preface..... | 2 |
| 2. Description of the Sample Application | 3 |
| 3. Listing of Sample Program..... | 8 |
| 4. Documents for Reference..... | 11 |

1. Preface

1.1 Specifications

- A/D conversion in single-scan mode by the 12-bit A/D converter
- Three rounds of A/D conversion are performed on analog input channels 0 to 3 (AN0 to AN3), and the converted data are stored in RAM.

1.2 Module Used

- 12-bit A/D converter (12-bit A/D)

1.3 Applicable Conditions

- MCU SH7137/SH7136
- Operating frequency Internal clock: 80 MHz
Bus clock: 40 MHz
Peripheral clock: 40 MHz
- Compiler SuperH RISC engine Family C/C++ Compiler Package Ver.9.01 Release01
from Renesas Technology
- Compiler options -cpu = sh2a -include = "\${WORKSPDIR}\inc"
-object = "\${CONFIGDIR}\\${FILELEAF}.obj" -debug -gbr = auto -chgincpath
-errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0
-del_vacant_loop = 0 -struct_alloc = 1 -nologo

1.4 Related Application Note

None

2. Description of the Sample Application

The sample program employs the single-scan mode of the 12-bit A/D converter to perform three rounds of A/D conversion on input channels 0 to 3 (AN0 to AN3), and then stores converted data in RAM.

2.1 Operational Overview of Module Used

The operating modes of the 12-bit A/D converter are single-cycle scan mode and continuous scan mode. In single-cycle scan mode, A/D conversion is performed once on each of one or more specified channels and then ends. The ADST bit is automatically cleared to 0. In continuous scan mode, A/D conversion is performed sequentially on one or more specified channels until the ADST bit is cleared to 0.

Additionally, channels 0 to 2 and 8 to 10 have dedicated sample-and-hold circuits, so multiple channels are capable of simultaneous sampling.

Table 1 gives an overview of the module used in this sample application (i.e. the A/D converter) and figure 1 is a block diagram of 12-bit A/D converter. For details on the 12-bit A/D converter, see the section on the A/D converter in the *SH7137 Group Hardware Manual*.

Table 1 Overview of the Module (A/D Converter) Used in the Sample Application

| Item | Description |
|--|---|
| Resolution | 12 bits |
| Minimum conversion time | 1.25 μ s per channel ($P\phi = 40$ MHz) |
| Number of modules | 2 |
| Input channels | 16 (SH7137), 12 (SH7136) |
| Operating modes | Single-cycle scan mode Continuous scan mode |
| Sample-and-hold function | Common to 0 to 7 channels: 1 circuit Common to 8 to 15 channels: 1 circuit Dedicated for individual channels: 1 circuit each for ch0 to 2 and 8 to 10 (6 in all) |
| Sources for activation of A/D conversion | Software: Setting of the ADST bit Timer: TRGAN, TRG0N, TRG4AN, and TRG4BN signals from the MTU2 module TRGAN, TRG4AN, and TRG4BN signals from the MTU2S module External trigger: ADTRG |

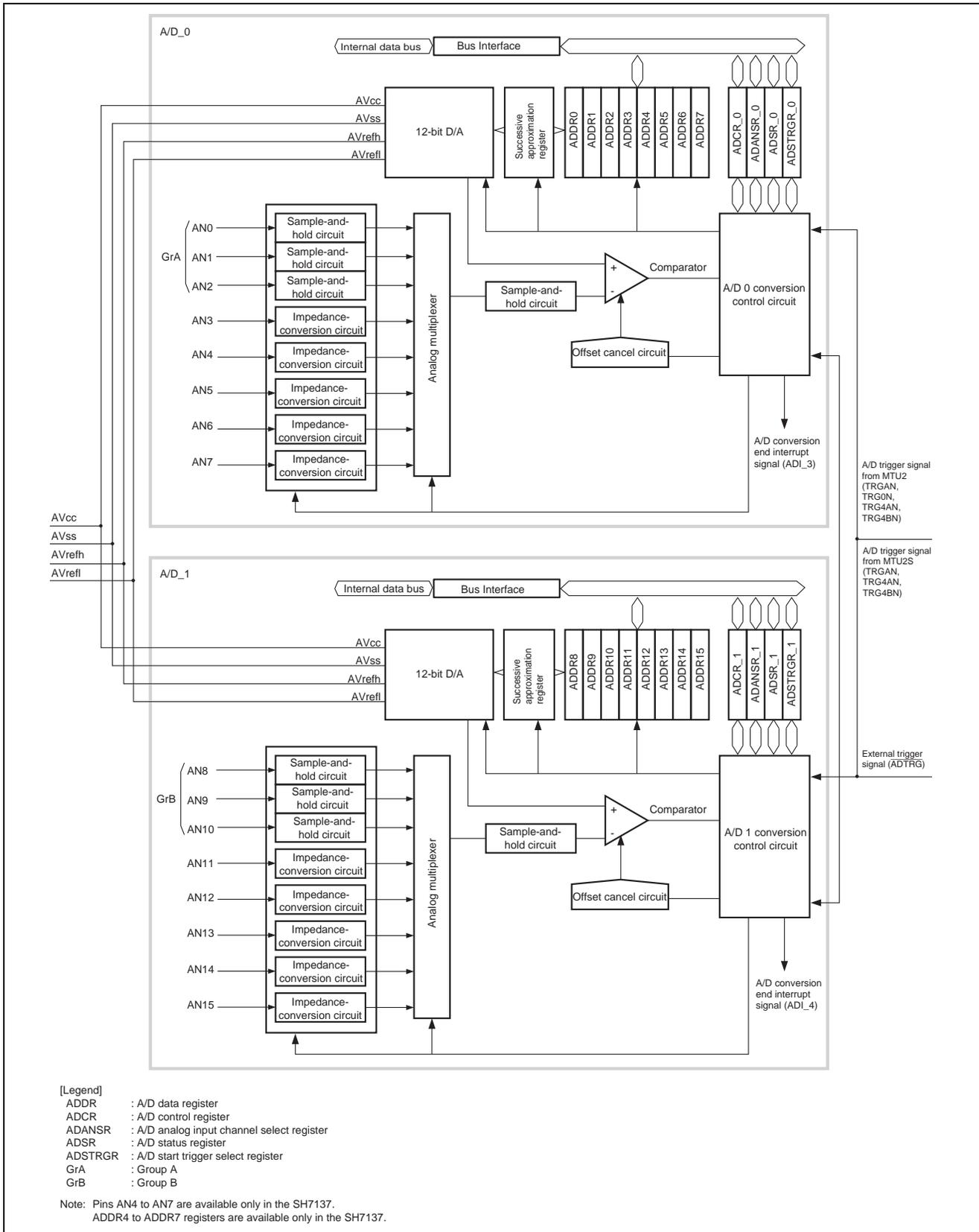


Figure 1 Block Diagram of the 12-Bit A/D Converter

2.2 Procedure for Setting Module Used

Figure 2 shows an example of the initialization sequence for A/D conversion in single-scan mode. For details on the settings of individual registers, see the *SH7137 Group Hardware Manual*.

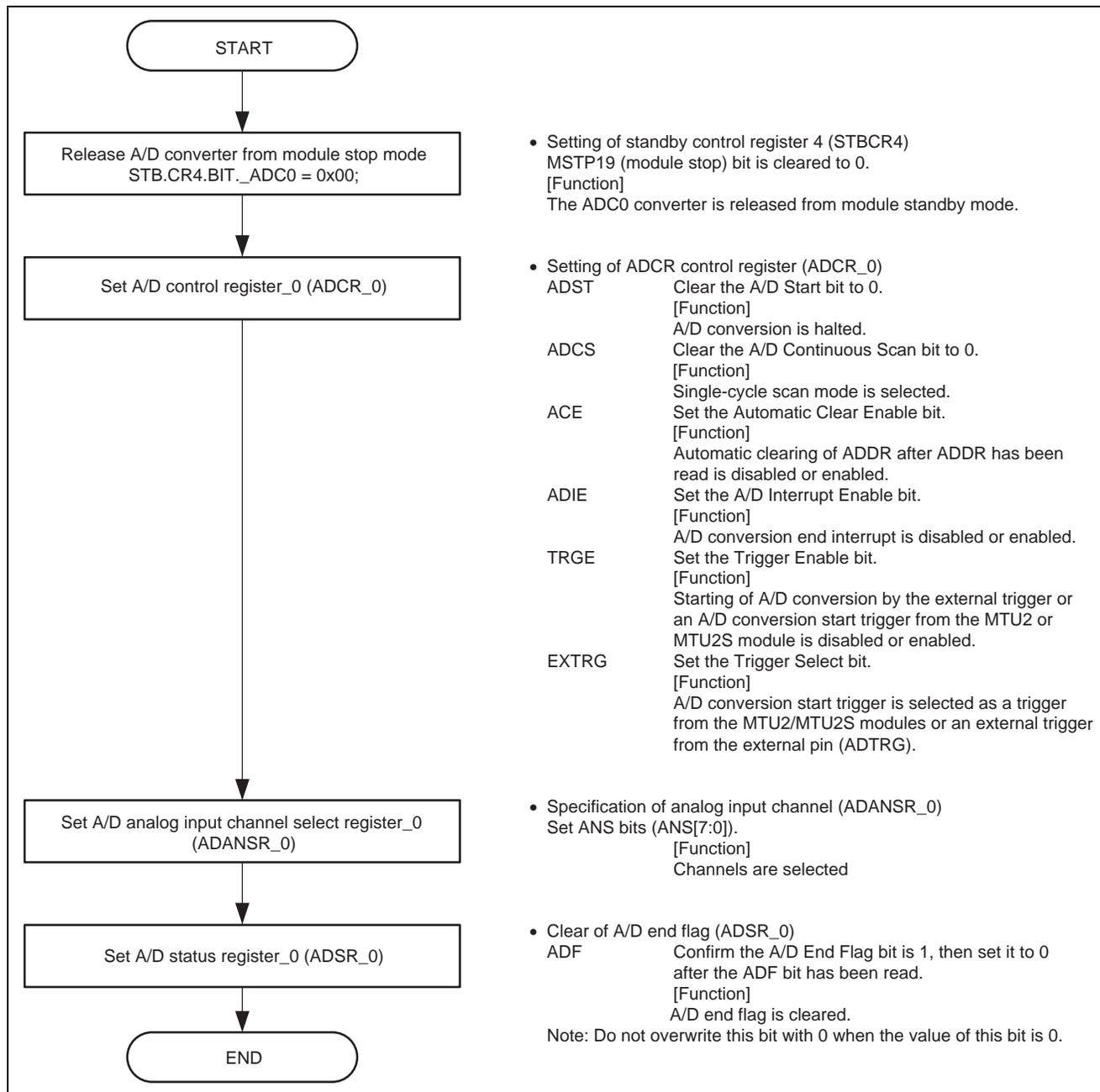


Figure 2 Initialization Sequence for 12-Bit A/D Conversion

2.3 Operation of the Sample Program

In this sample program, A/D conversion in single-scan mode is performed on channels 0 to 3 (AN0 to AN3). The A/D converter is activated by software and converted data are stored in RAM. This processing is repeated three times.

Table 2 gives a description of RAM usage in this sample program.

Table 2 Variables Used in the Sample Program

| Variable Name | Description | Area | Name of Employing Module |
|-----------------------------------|--|-------------|--|
| unsigned short Ad_data[AD][CH] | Array for storing A/D-converted data (2 bytes/datum) | On-chip RAM | io_ad_1cyc_scan (unsigned short*ad_buf) |

2.4 Sequence of Processing by the Sample Program

Table 3 gives settings for registers used in the sample program and figure 3 shows the flow of handling the sample program.

Table 3 Register Settings Used in Sample Program

| Register Name | Address | Setting | Description |
|------------------------------------|-------------|---------|---|
| A/D control register_0 (ADCR_0) | H'FFFF D400 | H'00 | <ul style="list-style-type: none"> ADST = 0: Halts A/D conversion ADCS = 0: Single-cycle scan ACE = 0: Disables automatic clearing of ADDR ADIE = 0: Disables A/D conversion end interrupt TRGE = 0: Disables starting of A/D conversion by an external trigger or by the MTU2 and MTU2S modules |
| | | H'80 | <ul style="list-style-type: none"> ADST = 1: Starts A/D conversion |

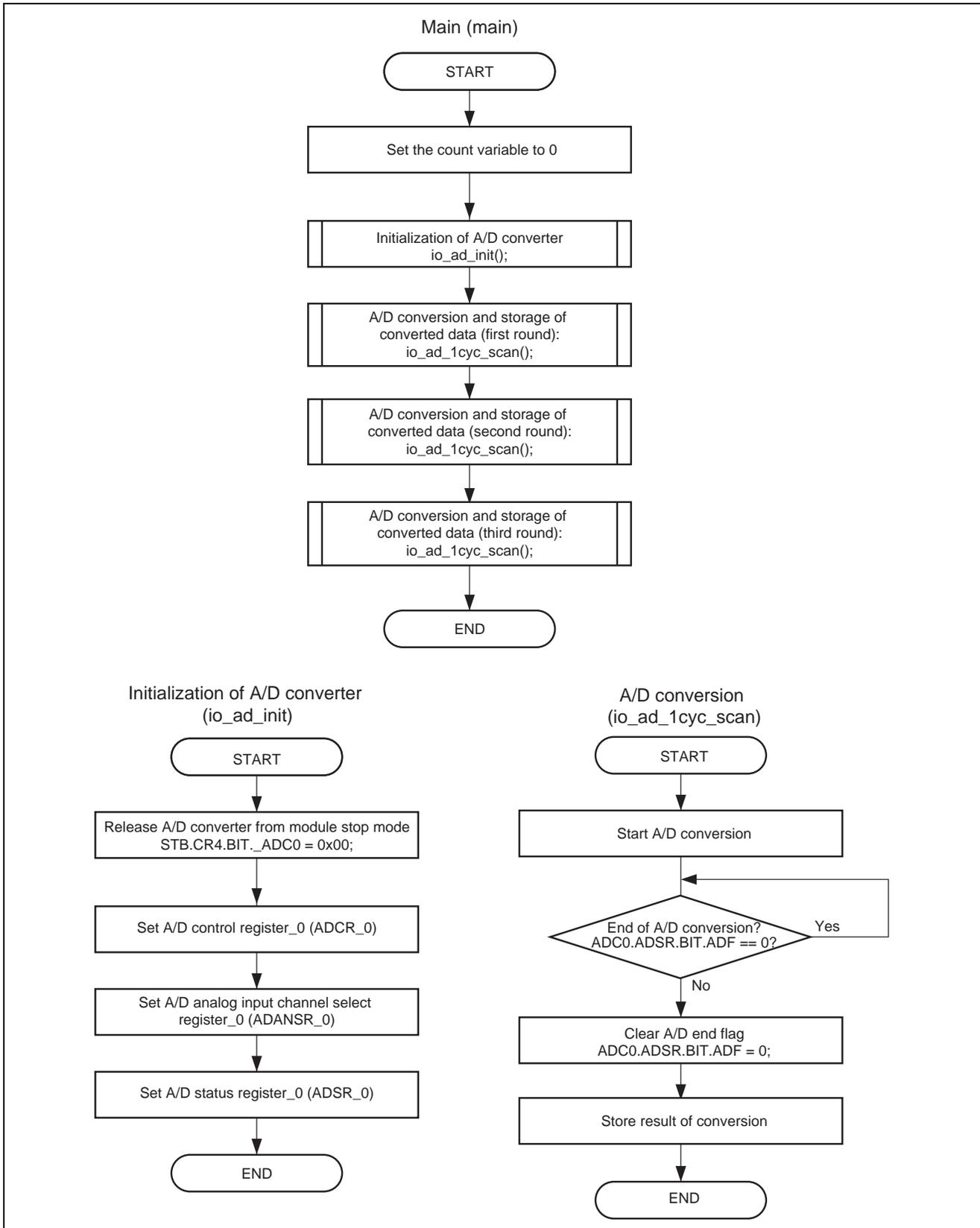


Figure 3 Flow of Handling the Sample Program

3. Listing of Sample Program

1. Sample Program Listing: "main.c" (1)

```

1  /*"FILE COMMENT"*****
2  *
3  *      System Name      : SH7137 Sample Program
4  *      File Name       : main.c
5  *      Contents        : Sample program for A/D conversion in single-scan mode
6  *      Version         : 1.00.00
7  *      Model           : M3A-HS37
8  *      CPU             : SH7137
9  *      Compiler        : SHC9.1.1.0
10 *      note            : A/D conversion in single-scan mode is performed by the A/D converter.
11 *                      Three rounds of A/D conversion on analog input channels 0 to 3
12 *                      (AN0 to AN3) proceed, and the converted data are stored in RAM.
13 *
14 *      The information described here may contain technical inaccuracies or
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19 *      Copyright (C) 2008 Renesas Technology Corp. All Rights Reserved
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21 *
22 *      history          : 2008.02.26 ver.1.00.00
23 *"FILE COMMENT END"*****/
24 #include <machine.h>
25 #include "iodefine.h"          /* SH7137 iodefine */
26
27 /* ==== prototype declaration ==== */
28 void main(void);
29 void io_ad_init(void);
30 void io_ad_lcyd_scan(unsigned short *ad_buf);
31
32 /* ==== symbol definition ==== */
33 #define AD 3
34 #define CH 4
35
36 /* ==== RAM allocation variable declaration ==== */
37 unsigned short Ad_data[AD][CH];
38

```

2. Sample Program Listing: "main.c" (2)

```

39  /*"FUNC COMMENT"*****
40  * Outline      : main
41  *-----
42  * Include      : #include "iodefine.h"
43  *              : #include <machine.h>
44  *-----
45  * Declaration  : void main(void);
46  *-----
47  * Function     : A/D conversion with 1 cycle scan mode
48  *-----
49  * Argument     : void
50  *-----
51  * Return Value : none
52  *-----
53  * Notice      :
54  /*"FUNC COMMENT END"*****/
55  void main(void)
56  {
57      unsigned char count;
58      count = 0;
59
60      /* ==== Initial Setting of ADC ==== */
61      io_ad_init();
62
63      /* ==== A/D conversion ==== */
64      io_ad_1cyc_scan(&Ad_data[count][0]);
65      count++;
66      io_ad_1cyc_scan(&Ad_data[count][0]);
67      count++;
68      io_ad_1cyc_scan(&Ad_data[count][0]);
69
70      while(1){
71          /* loop */
72      }
73  }
74
75  /*"FUNC COMMENT"*****
76  * Outline      : Initial setting of ADC
77  *-----
78  * Include      : #include "iodefine.h"
79  *-----
80  * Declaration  : void io_ad_init(void);
81  *-----
82  * Function     : Initial setting of ADC
83  *-----
84  * Argument     : void
85  *-----
86  * Return Value : none
87  *-----
88  * Notice      :
89  /*"FUNC COMMENT END"*****/

```

3. Sample Program Listing: "main.c" (3)

```

90 void io_ad_init(void)
91 {
92     /* ==== Release of power down mode (ADC0) ==== */
93     STB.CR4.BIT._ADC0 = 0x00;
94
95     /* ==== Setting of ADC ==== */
96     /* ---- A/D Control Register (ADCR) ---- */
97     ADC0.ADCR.BYTE = 0x00;
98     /* 7   = b'0       : A/D conversion start flag           */
99     /* 6   = b'0       : Single-cycle scan                   */
100    /* 5   = b'0       : Automatic clearing of ADDR by its readout
101                        is disabled                           */
102    /* 4   = b'0       : Generation of A/D conversion end interrupt
103                        is disabled                           */
104    /* 3-2 = b'0       : Reserve                               */
105    /* 1   = b'0       : A/D conversion start by the external trigger
106                        or an A/D conversion start trigger from
107                        the MTU2 or MTU2S is disabled         */
108    /* 0   = b'0       : A/D converter is started by the A/D conversion
109                        start trigger from the MTU2 or MTU2S   */
110
111    /* ---- A/D Analog Input Channel Select Register (ADANSR) ---- */
112    ADC0.ADANSR.BYTE = 0x0f; /* AN0-AN3 */
113
114    /* ---- A/D Status Register (ADSR) ---- */
115    if(ADC0.ADSR.BIT.ADF == 0x01){
116        ADC0.ADSR.BIT.ADF = 0x00; /* ADF clear */
117    }
118 }
119
120 /*"FUNC COMMENT"*****
121 * Outline      : A/D conversion
122 *-----
123 * Include      : #include "iodefine.h"
124 *-----
125 * Declaration  : void io_ad_lcyd_scan(unsigned short *ad_buf);
126 *-----
127 * Function     : Clearing of A/D end flag (ADF), and storing of conversion data
128 *-----
129 * Argument     : unsigned short *ad_buf ; Buffer which A/D conversion data are stored
130 *-----
131 * Return Value : none
132 *-----
133 * Notice      :
134 *"FUNC COMMENT END"*****/
135 void io_ad_lcyd_scan(unsigned short *ad_buf)
136 {
137     ADC0.ADCR.BIT.ADST = 1; /* A/D conversion start */
138
139     while(ADC0.ADSR.BIT.ADF == 0){
140         /* A/D conversion completion waiting */
141     }
142
143     ADC0.ADSR.BIT.ADF = 0; /* ADF clear */
144     *ad_buf++ = ADC0.ADDR0; /* AN0 */
145     *ad_buf++ = ADC0.ADDR1; /* AN1 */
146     *ad_buf++ = ADC0.ADDR2; /* AN2 */
147     *ad_buf++ = ADC0.ADDR3; /* AN3 */
148 }
149
150 /* End of File */

```

4. Documents for Reference

- Software Manual
SH-1/SH2/SH-DSP Software Manual
The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
SH7137 Group Hardware Manual
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| Rev. | Date | Description | |
|------|-----------|-------------|------------------------------------|
| | | Page | Summary |
| 1.00 | Jun.18.08 | — | First edition issued |
| 1.01 | Dec.12.08 | 8 to 10 | Listing of Sample Program modified |
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