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# Introduction

Lead acid batteries, once charged, are typically held at a float voltage that is higher than the open-circuit voltage (OCV). The intent of this float charge is to compensate for self-discharge. Not that this is without problems: there is greater water loss due to gas evolution, when compared to being held at OCV. It has also been argued by many that maintaining stationary batteries at float voltage does more harm than good - see, e.g., Nguyen et. al. [1]. Using a reduced float voltage with intermittent charge can be a superior method of battery management in many applications. One specific context of application for such battery management is in on-grid solar applications. In such applications, the battery is only used as a standby, yet it may represent a sizeable chunk of the investment in the solar system. Therefore, the battery life needs to be extended, and its maintenance and watering needs must be reduced also.

### **Enhanced Battery Management**

On initiating a charging cycle for a lead acid battery, it goes through several states.

We summarize the process very briefly; more detailed information is readily available in the public domain, e.g. at websites such as The Battery University [2]. Charging begins in a constant current (CC) regime called the Bulk phase, which ends when the voltage reaches Bulk Voltage (see Table 1). The regime then changes to constant voltage (CV). The battery enters the Absorption state, in which the voltage is held constant at the Bulk Voltage for a specified period of time. Then the voltage is reduced to the Float Voltage which, in the standard case, signals the end of charging. In this application note we are not content with stopping with that. Rather, we want to hold the battery at the Float Voltage for a specified period of time, then reduce the voltage further to what we call the Reduced Float Voltage, which represents the end of the charge cycle.

Typically, the Reduced Voltage will be close to the battery's OCV. However, a battery cannot be held at OCV for too long because it starts to lose capacity and then sulfate. Therefore, the battery must intermittently be taken to a higher voltage (Float or Absorption Voltage) to compensate for this loss of capacity, then brought back to the Reduced Voltage. This may seem like an obvious feature to have in a solar inverter for example, but in the author's experience it is not always available, even in premium inverter brands.



Figure 1. The Battery State Machine



The state diagram in Figure 1 represents those states and their transitions.

# Solution Architecture using GreenPAK<sup>™</sup>

In this section we describe how the various building blocks of **GreenPAK** as well as external elements are brought together to realize the solution. (We will henceforth use programmingstyle variable names such as BulkVoltage, FloatDuration etc.) The IC chosen is SLG46531V. **Asynchronous State Machine (ASM).** GreenPAK was chosen because it offers an ASM that makes it particularly convenient to capture the battery states and transitions. The state and transition definitions are shown in Figure 1.

**ACMPO-2.** For this application note, we take a case where the nominal battery voltage is 12V. The design can easily be extended to other voltages. We can scale the battery voltage with a resistive voltage divider, but we choose an alternate strategy given that we are not interested in voltages less than 12.5V or greater than 14.5V.







We *subtract* 12.5V using shunt references of 10V and 2.5V, as shown in Figure 3, leaving us with a much smaller voltage range of about 2V to contend with, thereby allowing greater accuracy in voltage measurement. This transformed battery voltage of 0-2V is run through a 0.5X gain stage at each analog comparator (ACMP) IN+ input.

$$V_{IN+} = 0.5 * (V_{BAT} - 12.5)$$

Thus each ACMP input IN+ sees a voltage of 0-1V.

For example if we take a 12V Exide SolaTubular battery, the manufacturer-specified values and the transformed values for the respective ACMPs are shown in Table 1.

The above voltage thresholds for the ACMPs are conveniently derived from the internal voltage reference and no external voltage reference is required. The external components used in the design are shown in Fig 3. The component value selection is explained in the section "Example Implementation.'

One of the ACMP's (ACMP0), is referenced to BulkVoltage; when the ASM is in Bulk and the battery reaches BulkVoltage, the AND gate triggers the state change from Bulk to Absorb. The other ACMPs are used to effect the CV regimes by holding the battery voltage at the respective value such as FloatVoltage and ReducedFloatVoltage as we will describe shortly.

Delays/Counters. Once the battery exits the bulk phase, the rest of the state transitions for the remainder of the charge cycle may be conveniently triggered by time duration. For example, the battery moves from Absorb to Float after AbsorbDuration (2 hours) and from Float to ReducedFloat after FloatDuration (1 hour). After spending several days at ReducedFloatVoltage, the battery will be taken up to FloatVoltage again for FloatDuration and the process iterates. These time-based achieved triggers are using delay/counter blocks CNT1/2/3. We wire these as delays rather than counters because a counter outputs a high when it is reset, which disturbs the operation. Instead, we configure these as risingedge delays as shown in Fig.4. For example, DLY3's DLY IN comes from the ASM's Float state output; therefore when Float is entered, the high state is detected by DLY3 and fed to the Float-Reduced float transition after FloatDuration. As soon as the ASM moves from Float to ReducedFloat, DLY\_IN returns to zero, dragging the output also to zero.

Parameter	Value for 12V Battery	Transformed Value at $V_{IN+}$
Bulk voltage	14.5V	1.0V
Float voltage	13.7V	0.6V
Reduced Float voltage	12.6V	0.1V

### Table 1. Typical voltages associated with a lead-acid battery





3-bit LUT6/8-bit CNT3/DLY3 CNT/DLY Type: Ŧ Delay Mode: Ŧ \$ Counter data: 60 (Range: 1 - 255) Delay time N/D Formula (typical): Edge select: Rising Ŧ Output polarity: Non-inverted (OUT -Q mode: Stop and

Figure 3. External Components Used

The clock source for all these delays is CNT0 whose input is the 25kHz clock and output period is set to 60 seconds.

**GPIOs.** A new charge cycle is initiated by driving a HIGH input on Pin3. In an actual application this could be used to initiate a new cycle manually, based on time or based on the battery voltage going too low. The last use case requires an external comparator, and effectively defines NewCycleVoltage as a trigger. Typically its value would be 11.5V for a 12V battery.

In the CC regime, current must typically be limited to C/10 where C is the battery capacity in AH. This is achieved by the output transistors Q1 and Q2 driven into an ON or OFF state by Pin4, wired as a digital output. The current-determining resistor is on the emitter of Q1, and as indicated its value should be 10/C for a battery of capacity C that is rated for a maximum charge current C/10.

Figure 3. DLY Configuration

The battery connects to the collector of Q1 so its voltage does not significantly affect the charge current.

**ACMP1, ACMP2.** Only one state transition is driven by voltage – the BulkVoltage. In contrast to this, the other voltages – e.g. FloatVoltage and ReducedFloatVoltage are not triggers for state transitions. Rather, these are outcomes of the state that the battery is in. Because all these voltages are associated with a CV regime, we may use them as references for ACMP1 and ACMP2 respectively, which allows us to trigger a state change based on the current state and the battery voltage. These comparators are in turn used to drive the charging transistor Q1 as now described.

In the CV regime, there are two ways of charging a battery. One is by the use of a steady current and the other is by using a pulsed current of higher magnitude. For example, pulsed current is used in PWM charging which is popular for lead acid batteries as it supposedly helps reduce sulfation (See The Battery University article [Error! Reference source not found.] and the accompanying comments). We use pulsed charging in the CV regime too, using the same PNP transistor used for CC charging. Based on the state of the battery, we select the appropriate ACMP to also drive the bias to Q1. We use a 25mV hysteresis setting for the ACMPs so that the transistor switches on and off to maintain the average battery voltage at the desired level, equal to the selected ACMP's reference voltage and within the chosen hysteresis band.

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For instance, FloatVoltage is a reference for ACMP2. When the battery enters the Floating phase, we would like to use ACMP2's output to determine when to bias Q1. Since ACMP2's input IN+ pin is reading the actual battery voltage, its output will switch the transistor on and off repeatedly as the actual battery voltage oscillates slightly about FloatVoltage (within ACMP2's hysteresis band). Similar logic holds for CV charging at the other voltages: BulkVoltage and ReducedFloatVoltage. This logic is captured in the truth tables for LUT0/1/2, ORed together by L7.

**Example Implementation.** The design was implemented with the external components in Figure 3 and used to charge an Exide 12V 4.5AH battery. Z1 and Z2 must have a similar operating current range. Here they are LM4040s that operate with a current range of 60 uA to 10mA. Along with R3 = 330R, the current range falls within spec for the desired battery voltage range. C1 is required to avoid forcing the GreenPAK to respond too fast when the comparator is in the hysteresis range, otherwise spurious behavior can result. Q2 is driven to saturation whenever Pin 4 goes high; this drives nearly 10mA through the LED with Vcc = 15V. With a red LED, the voltage drop across R1 is about 1V, so R1 should be set to 10/C ohms to limit charge current to C/10.

The following photographs show the waveform at Pin 4 when the battery is in the Absorb and Float CV regimes. The pulsing nature of the charger is evident; the charge pulse in this test setup was







Figure 6. Pin 4 level, Float

about 5ms with a 300mA charge current.



Note: In the accompanying .GP5 file we have, for testing and evaluation purposes, set CNT0 to output 1s pulses rather than 60s pulses, and the DLY block data have been set so that AbsorbDuration, FloatDuration and ReducedFloatDuration are 1 minute each. The labels attached to the CNT0 and DLY blocks indicate the values that would make more sense in a real implementation.

# Conclusion

In this application note we demonstrated how a mixed-signal platform like the GreenPAK simplifies the design of an extended battery charger with minimal external components. Several extensions to the design are possible and desirable in a robust, field-deployable system. For complete generality we may add a current sensor that triggers a state change in the CV regimes based not on time but on the current dropping below a certain value. Temperature compensation of battery voltages is an important aspect that we have not considered here. We could also do with a load-dependent voltage trigger for a new charge cvcle begin. Parameters to such as AbsorbDuration, FloatDuration, etc. may be made to depend on the frequency of charge/discharge cycles experienced in the application and so on. Ultimately, the objective is to squeeze the maximum life out of a battery and, though lead acid batteries are almost as old as sliced bread and have been analyzed to death, they are temperamental creatures and battery life optimization is easier said than done!

### References

1. "Traditional float charges: are they suited to stationary antimony-free lead acid batteries?" T. M. Phuong Nguyen, Guillaume Dillenseger, Christian Glaize and Jean Alzieu, in *Trends in Telecommunications Technologies*, Christos J. Bouras (ed), INTECH Publishing, 2010. http://www.intechopen.com/books/trends-intelecommunications-technologies;

2. http://www.batteryuniversity.com

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