Application Note

Wake / Sleep Timing Generator

SLG46140

Battery-powered systems require efficient power-management techniques to maximize operating lifetime. In GreenPAK™ devices, analog resources such as comparators (ACMPs) and the ADC often represent a major share of total current consumption.
This application note presents the implementation of a Wake/Sleep timing generator based on the SLG46140. The proposed Wake/Sleep (W/S) function periodically enables and disables analog blocks to reduce average power consumption while maintaining system-state continuity by latching the corresponding outputs. Timing generation is achieved using the internal counter operating in Wake/Sleep ratio control mode and clocked from the low-frequency oscillator.
The described approach provides a practical method for lowering power dissipation without compromising functional behavior, making it well suited for low-power sensing, monitoring, and other battery-operated applications.

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1 Terms and Definitions

ACMP	Analog Comparator
ADC	Analog-to-Digital Converter
CNT	Counter block inside GreenPAK
DCMP	Digital Comparator
IC	Integrated Circuit
LF OSC	Low Frequency Oscillator
LUT	Look-Up Table logic cell
PGA	Programmable Gain Amplifier
PWR UP	Power enable control signal
Sleep Mode	Low-power state in which circuit blocks are powered down while outputs remain latched
Wake Mode	Active state in which circuit blocks are powered and operate normally
Wake/Sleep (W/S)	GreenPAK power management function that periodically powers analog blocks ON and OFF
WS Ctrl	Wake/Sleep Control block derived from CNT0 configured in Wake/Sleep ratio mode

2 References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas

Download our free GreenPAK™ Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Designer Software, Software Download and User Guide, Renesas Electronics
[2] AN-1076.gp, GreenPAK Design File, Renesas Electronics
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics
[5] SLG46140V, Datasheet, Renesas Electronics

Author: Roman Yankevych

3 Introduction

For battery-powered applications, minimizing current consumption is a critical parameter of the design. So, keeping current consumption as low as possible is crucial. This can be achieved by using a WS (Wake/Sleep) timing block for controlling on-chip circuit block powerdown. The most power consuming blocks in GreenPAK IC's are those that work with analog signals (ACMPs, ADC).

4 Wake/Sleep Function Operation Example

The wake/sleep function switches on and off the relevant circuit blocks. In the SLG46140 IC, there are ACMPs and ADC blocks. The block that creates a Wake/Sleep signal is CNT0 switched into 'Wake Sleep ratio control' mode (it morphs into the WS Ctrl block). In this mode this block operates as a counter but supplies ACMPs and ADC with power on and latch signals.

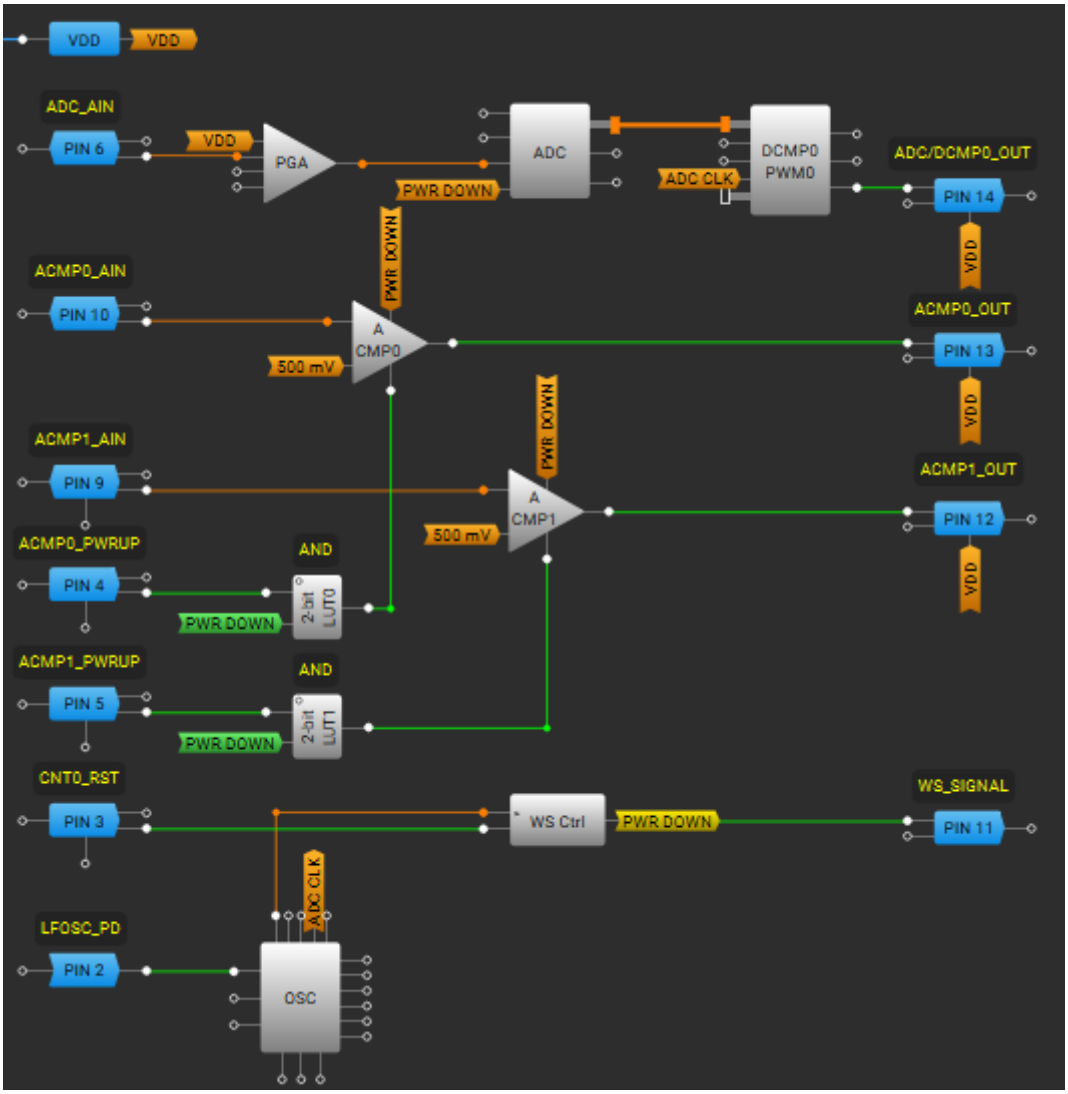

Figure 1: SLG46140 based design with all blocks wake/sleep controlled

To make this function operational just set its type to 'Wake sleep control'. The on time is defined by the clock frequency (LF OSC) and lasts one clock cycle. The ratio is controlled by changing the Counter data value, so the on time is constant, but the overall period could be changed. This design example provides the control of all possible external signals that influence the blocks with wake/sleep function.

NOTE: The on time can be controlled by the clock frequency of LF OSC, and there is a post clock divider behind LF OSC. One can change the LF OSC clock frequency by changing the output divider. The WS Ctrl input clock is from the output of this divider.

5 ACMP Wake and Sleep

To turn on the Wake/Sleep function in ACMP, change the 'ACMPx Wake sleep' option to 'Enable' in the properties of any of the WS Ctrl block. This function is shared between both ACMPs in SLG46140 IC, which means the WS function will be turned on in both ACMPs if any has this option enabled. The operation of WS is the following: the PWR UP input signal of the ACMP should be HIGH to enable block's operation. Setting the PWR UP input (ACMP0_PWRUP or ACMP1_PWRUP) LOW will latch the previous data on the output. After the block is powered up, it will periodically turn on. On the falling edge of the WS signal, the ACMP will latch the output and will not change it until the next WS pulse comes. The ACMP operation can be stopped in several ways: set PWR UP signal LOW, SET or RESET the WS control block, power down the LF OSC. These events have priorities shown in table 1.

NOTE: For correct ACMPs operation the PWR UP input should be sourced from WS Ctrl output. We recommend using LUTs logic cells for full ACMPs operation control.

Table 1: The ACMP operation

Priority	Event	State	Action
1	ACMP Power	Up (W/S[1])	ACMP with W/S
		Down (LOW)	ACMP is OFF
2	LF OSC Power	Up (LOW)	ACMP with W/S
		Down (HIGH)	ACMP is ON or OFF[2]
3	WS Ctrl	SET/ RESET[3]	ACMP always ON or OFF
		none	ACMP with W/S

Operation of the W/S function in ACMP with LF OSC always turned on shown below.

NOTE: Because the W/S function is shared in both ACMPs, there only possible operation cases use 3 control signals (ACMP PWR UP, WS Ctrl RESET/SET IN, LFOSC PWR DOWN). Note that there is no way for one ACMP to be turned on and another ACMP to be in W/S mode:

Table 2: ACMP in W/S mode

ACMP0	ACMP1
ON	ON
OFF	OFF
W/S	W/S
W/S	OFF
OFF	W/S

[1] sourced from WS Ctrl output

[2] depends on 'Wake sleep output state' configuration in WS Ctrl block

[3] depends on WS Ctrl 'Q mode' configuration

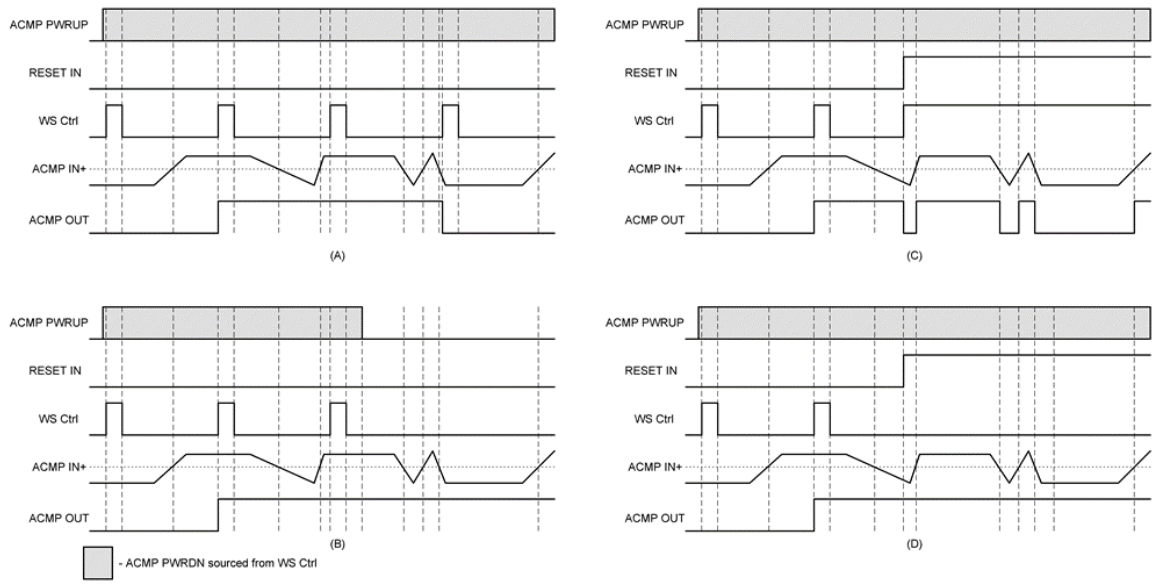

Figure 2: Timing diagrams of the wake/sleep function.

A – ACMP always in W/S mode; B – ACMP forced to power down by ACMP PWRUP in LOW; C – ACMP forced to be always on by WS Ctrl RESET IN in SET mode; D – ACMP forced to power down by WS Ctrl RESET in in RESET mode

6 ADC Wake and Sleep

In this example DCMP0 is used to compare the ADC parallel data with its Register0 value (‘127’, corresponds to 0.5V).

According to the SLG46140 datasheet, the signal to ADC comes from PGA which should be powered down if WS function is used.

Unlike ACMPs ADC power down signal becomes inactive when W/S function is turned on. The rest operates the same as ACMPs with WS function turned on. So the ADC could be turned ON, always OFF or Wake/Sleep depending on WS Ctrl RESET/SET and LF OSC PWR DOWN signals.

7 Conclusion

The W/S function is very useful if analog blocks are used and low power consumption is desired. Wake and sleep itself not only powers up and down ACMPs and ADC dynamically, but also latches the outputs while blocks are in sleep mode. All blocks share the same W/S signal generation source – WS Ctrl/CNT0. It is shared for ACMPs together, while ADC is independent.

Revision History

Revision	Date	Description
1.0	20-May-2015	Initial version
1.01	06-Apr-2026	Updated ADC “Analog part speed”

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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