QUALITY SEMICONDUCTOR, INC.

CMOS Bus Switches Provide Zero Delay Bus Communication

Application Note AN-09

The QS3383 and QS3384 CMOS Bus Switches by Quality Semiconductor are high-speed TTL bus connect devices. When they are enabled, the bus switches directly connect two buses with a connection resistance of less than 5Ω. They are like a 5ns multi-pole relay for TTL signals with an ON resistance of 5Ω. Since these devices directly connect the bus signals they introduce no additional propagation delay, timing skew or noise. They are also inherently bidirectional and dissipate no additional power. They can replace traditional TTL buffers and transceivers to reduce propagation delay, noise, control complexity and power dissipation.

A block diagram of the QS3384 CMOS Bus Switch is shown in Figure 1. This device consists of ten switches arranged as two banks of five. This allows the QS3384 to be used as a 10-bit switch or as a 5-bit, 2-to-1 multiplexer. A block diagram of the QS3383 CMOS Bus Exchange Switch is shown in Figure 2. This device consists of two banks of ten switches arranged to gate through or exchange two banks of five signals. This allows the QS3384 to be used as a 10-bit switch or as a 5-bit, two way bus exchange device. This part is particularly useful for exchange and routing operations such as byte swap, crossbar matrices, and RAM sharing.

Each switch consists of an N channel MOS transistor driven by a CMOS gate. When the switch in enabled, the gate of the N channel transistor is at V_{CC} (+5V) and the device is on. These devices have an ON resistance of less than 5Ω for voltages near ground and will drive in excess of 64mA each. The resistance rises somewhat as the I/O voltage rises from a TTL LOW of 0.0V to a TTL HIGH of 2.4V. In this region the A and B pins are solidly connected, and the bus switch is specified in the same manner as a TTL device over this range. As the I/O voltage rises to approximately 4.0V, the transistor starts to "pinch" off limiting the amount of the current available to drive the load voltage up. This corresponds to a typical TTL HIGH of 3.5 to 4.0V.

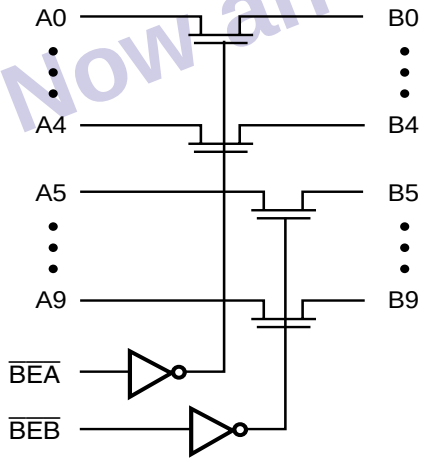

Figure 1. QS3384 CMOS Bus Switch Block Diagram

Table 1. Pin Description

Name	I/O	Function
A9-A0	I/O	Bus A
B9-B0	I/O	Bus B
$\overline{BEA}$, $\overline{BEB}$	I	Bus Switch Enable

Table 2. Function Table

$\overline{BEA}$	$\overline{BEB}$	B4-B0	B9-B5	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A4-A0	Hi-Z	Connect
H	L	Hi-Z	A9-A5	Connect
L	L	A4-A0	A9-A5	Connect

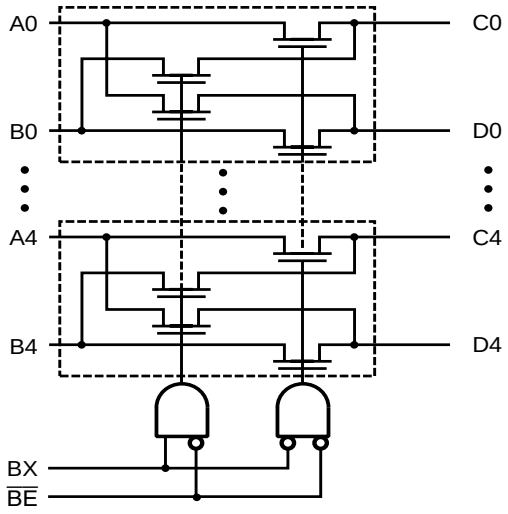

Figure 2. QS3383 CMOS Bus Exchange Switch Block Diagram

Table 3. Pin Description

Name	I/O	Function
A4-A0, B4-B0	I/O	Buses A, B
C4-C0, D4-D0	I/O	Buses C, D
$\overline{BE}$	I	Bus Switch Enable
BX	I	Bus Exchange

Table 4. Function Table

$\overline{BE}$	BX	A4-A0	B4-B0	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C4-C0	D4-D0	Connect
L	H	D4-D0	C4-C0	Exchange

The bus switch provides a low resistance connection between inputs and outputs for voltages below 3.0V. As the I/O voltage rises above 3V, the resistance increases until the switch turns off, at approximately 4.0V. This is shown in Figure 3, a V_{IN} versus V_{OUT} chart. The switch on resistance is determined by the lower of the voltages on the two I/O pins. The resistance rises as the I/O voltage rises, as shown in Figure 4.

V_{OUT} vs. V_{IN} for Various Loads, Typical

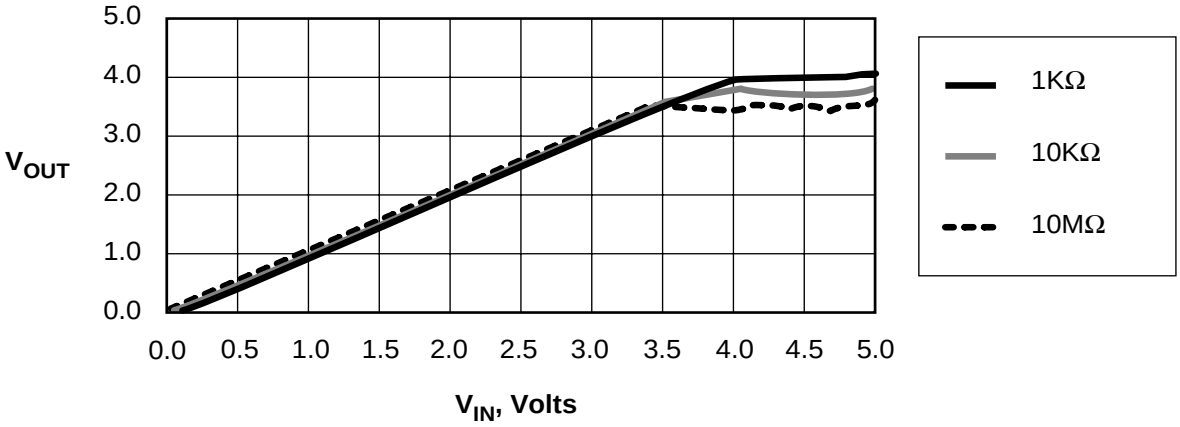

Figure 3. V_{OUT} vs. V_{IN}

The bus switch provides a path for a driving device to drive capacitance to ground and to drive capacitance up from ground. This is shown in Figure 5. When the A (or B) input is driven to a TTL LOW of 0.0V, the N channel transistor is fully ON and the B (or A) output will follow it. Likewise, when the A (or B) input is driven from a TTL LOW of 0.0V to a TTL HIGH, the capacitor side of the N channel switch is at 0.0V, the switch is fully ON and the B (or A) output will follow it through threshold and beyond. This means that the rise and fall time characteristics and waveforms of the B (or A) output will be determined by the TTL driver, not the bus switch. The switch introduces no propagation delay, to a first approximation.

When the bus switch is disabled, the N channel transistor gate is at 0.0V, and the transistor is OFF. By the nature of the N Channel transistor design, the A and B pins are fully isolated when the transistor is OFF. Leakage and capacitance is to the chip substrate (i.e., ground) rather than between input and output. This minimizes feedthrough in the OFF state. Because only an N channel transistor is used, either A or B pin(s) can be taken to V_{CC} and above, and the device can be powered down without loading either bus.

The bus switch can replace drivers and transceivers in systems if bus repowering is not required. Since the bus switch directly connects two buses, it provides no drive of its own but relies on the device that is driving data onto the connected buses. If the additional loading of the connected bus is small enough, there is a net gain in speed. For example, the sensitivity to loading of a driver such as the 74FCT244 is typically 2ns/100pF. If the connected bus adds 50pF of loading the added delay will be 1ns. This is much less than the 4 to 10ns delay of the buffer or transceiver the bus switch replaces.

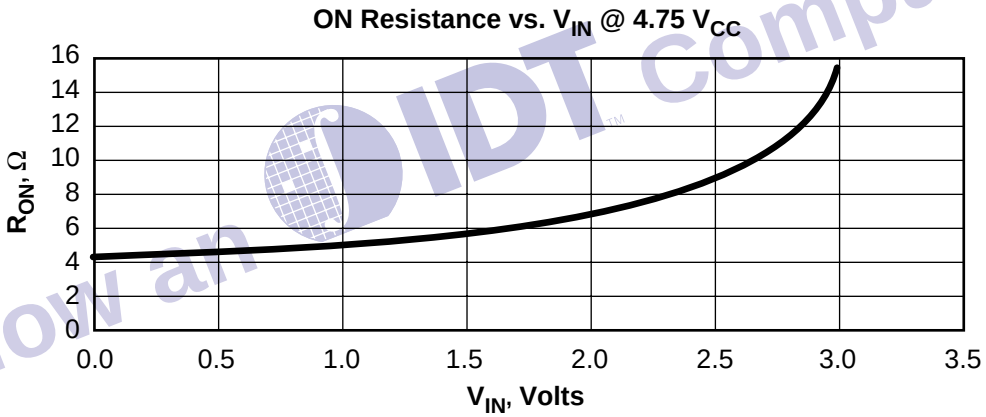

Figure 4. Switch ON Resistance vs. V_{IN}

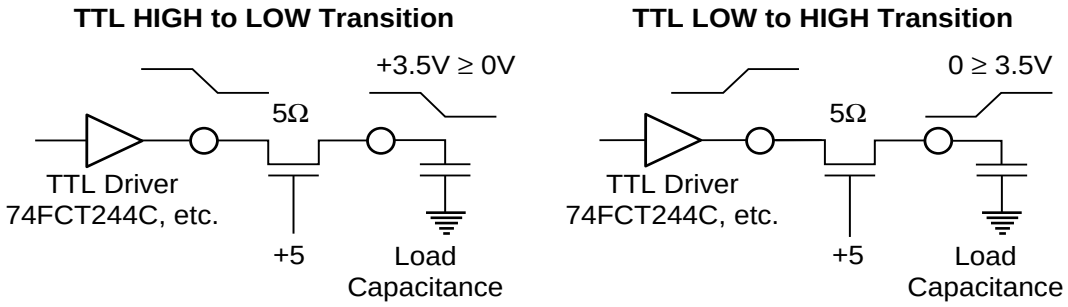

Figure 5. CMOS Bus Switch Operation

Microprocessor Shared Memory Connect for Slave Processor

Figure 6 shows the QS3384 bus switch used to allow the memory for a DSP slave processor to be accessed by the host processor. A 33MHz TMS320C30 system is shown with a 16K x 32 SRAM as its program and data storage memory. The SRAM is connected to the DSP CPU by a QS3384, allowing full-speed operation while the CPU is running. This saves 10ns over using conventional fast buffers and transceivers, i.e., 5ns for a 244 address buffer to the SRAM and 5ns for an 245 address transceiver from the SRAM, as shown in the timing diagrams. This allows using SRAMs with 35ns T_{AA} instead of 25ns. Between calculations, the QS3384's disconnect the SRAM from the DSP CPU and connect it to the host CPU, allowing the host to write data in before the DSP calculation and read data out after.

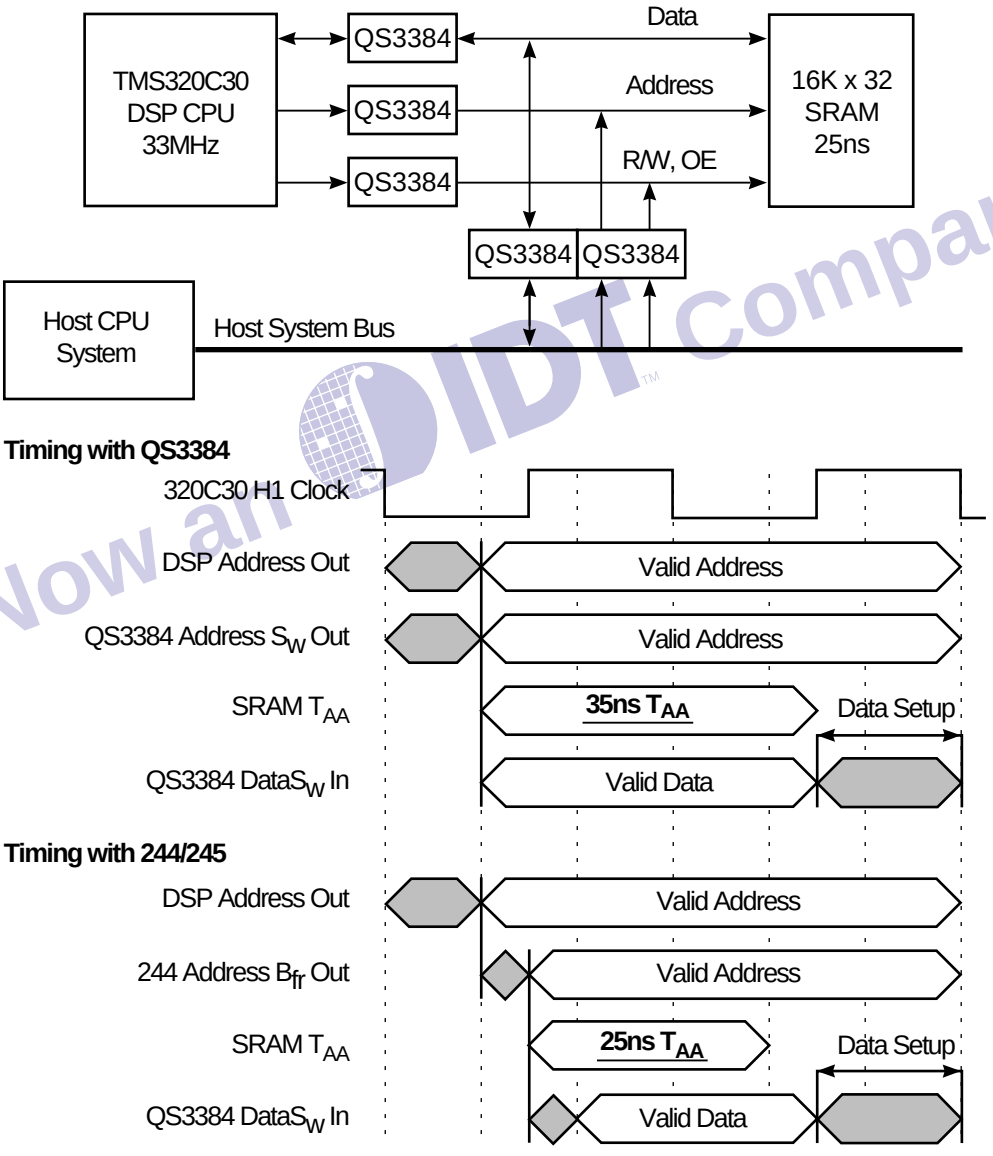

Figure 6. QS3384 as DSP Shared Memory Connect

Multiprocessor System Fast Bus Connect

Figure 7 shows the QS3384 bus switch used as a fast bus connect in a high-performance multiprocessor system. Four 32-bit processors are shown, each with its own cache or other local memory. Each processor is connected by a QS3384 bus switch to a 1 meg x 32, 25ns cycle time fast SRAM main memory. The 3384 is used to connect the address, data, and control lines of the SRAM directly to each processor. When one of the QS3384's is active, the main memory appears as a simple SRAM to the connected CPU. This provides a simple, very fast interface with no additional delays for buffers or data direction logic and no timing skew in the control signals.

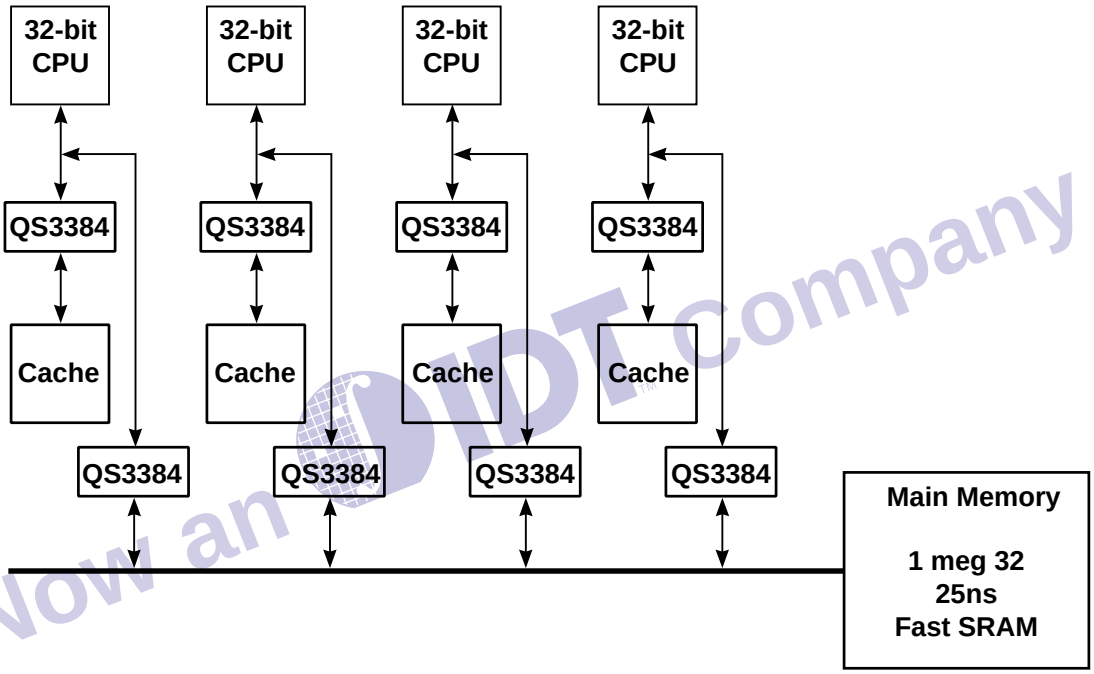

Figure 7. QS3384 as Multiprocessor System Bus Connect

Bus Exchange Switch for Ping Pong Memory Connect

Figure 8 shows the QS3383 bus exchange switch used to connect two memories to a DSP processor and a host CPU bus. The QS3383 connects Memory A to either the DSP or host CPU, and Memory B to the host CPU or DSP CPU, respectively, depending on the state of the bus exchange control. This configuration allows the host CPU to be accessing one memory for loading program and data or retrieving results while the DSP CPU is running out of the other memory. When the calculation is complete, the memories are exchanged, and the DSP CPU can continue with another calculation while the results of the last one are accessed. This configuration allows both high-speed and HIGH throughput.

The Ping Pong memory configuration can also be used to pipeline results between processors, as shown in Figure 9. All processors transfer data from their input memories to their output memories. When one pass is complete, the memories are exchanged and the output of one processor becomes the input of the next.

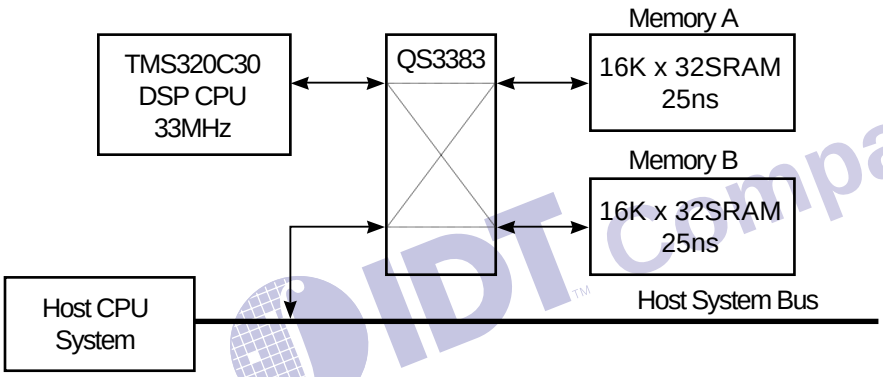

Figure 8. QS3383 for Ping Pong Memory Connect

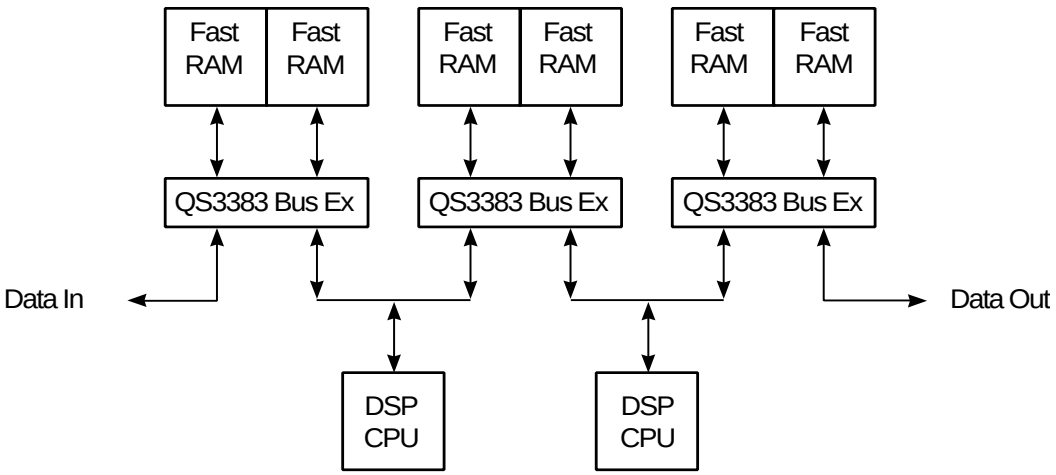

Figure 9. QS3383 for Ping Pong Pipeline Memory

Bus Exchange Switch for Crossbar Systems

Figure 10 shows the QS3383 bus exchange switch used to connect four CPUs and four memories in a crossbar configuration. In this configuration, any CPU can be connected to any memory. If there is no conflict by two CPUs for the same memory, any valid combinations of CPU and memory can be made by appropriate selection of the QS3383 controls. Two layers of QS3383 bus exchange switches are required for this four-way crossbar. Three layers will be required for an 8-way crossbar, etc.

The QS3383 bus exchange switch is ideal for crossbar work because it introduces no delay of its own. A 16-way crossbar with four layers of switches adds little or no delay over direct connection of the RAM to the CPU. Also, the CPU sees a simple RAM interface without the complicated timing skew requirements which might be imposed by using bus transceivers instead of QS3383 switches.

Bus Exchange Switch for Bus Byte Swap and Barrel Shift

A scheme similar to the one shown in the diagram of Figure 10 can also be used to provide byte swap capability between a CPU and memory. This is useful in systems where big-endian and little-endian byte orders are mixed within the same system. If the CPU and RAM blocks of Figure 10 are interpreted as bytes of a CPU and memory bus respectively, the crossbar switch scheme shown allows any combination of byte swapping or shifting desired without introducing any additional propagation delay or control considerations. If this concept is extended to the bit level, a barrel shifter results.

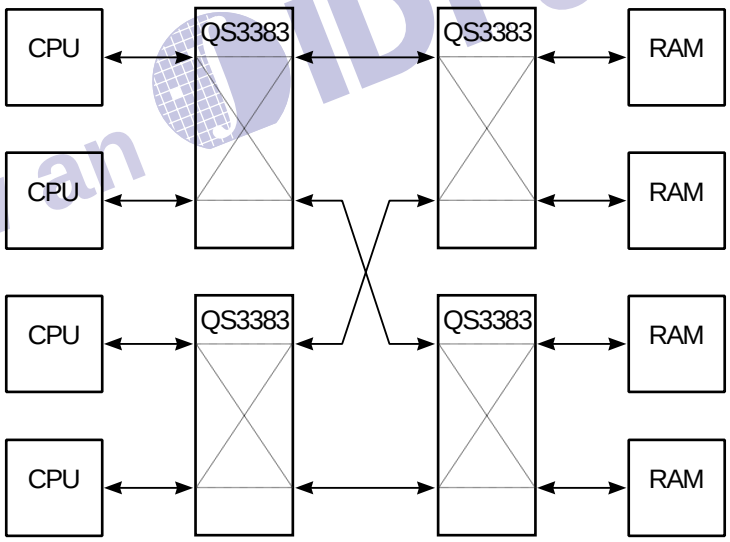

Figure 10. QS3383 Crossbar Switch

Fast Address Latch

Figure 11 shows the QS3384 bus switch used as a fast address latch in an SRAM memory subsystem. In this system, the QS3384 connects the SRAM to the address bus, which drives the stray capacitance of the SRAM array. When the QS3384 turns OFF, the stray capacitance holds the TTL level. The advantage of using the QS3384 instead of a fast latch such as the 74FCT373 is that the effective throughput delay is much less. The delay caused by the additional 50pF load on the address bus may be 1ns as compared to 4ns for the fastest latch. Also, the QS3384 does not introduce additional noise.

The hold time for typical capacitances and leakages can be quite long compared to the clock cycle times of fast systems. For the 16K x 32 configuration of eight 16K x 4 SRAMs shown, the stray capacitance is of the order of 50pF. The turn OFF transient of the QS3384 will typically be less than 50mV. Assuming a 1V change in level and a typical total leakage at operating temperature of less than 50nA, (SRAMs + 3384), the hold time is of the order of (50 x 10E-12/50 x 10E-9) = 1ms. If an indefinite hold is desired, an active terminator such as QS3389 can be used as shown in Figure 11.

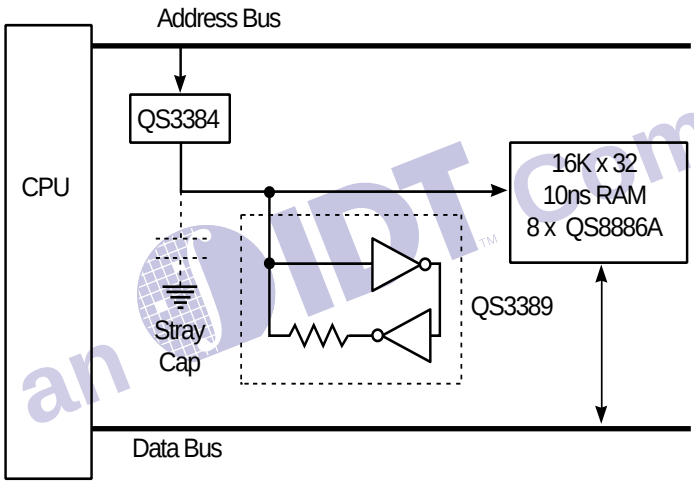

Figure 11. QS3384 Fast Address Latch

ATE Load Switch

Figure 12 shows the QS3384 bus switch used as a load switch for an automated test equipment (ATE) load board. ATE equipment requires custom design of the load board (i.e. electrical test fixture) for a given device to be tested. A common problem to be solved is the connection and disconnection of load resistor network to each pin of the device under test (DUT). The load must be connected during parts of the test and disconnected during other parts. This connection is typically done with small relays because of their LOW ON resistance. However, relays are large and slow. The QS3384 bus switch can replace up to 10 relays in this application, in a smaller package, and with an actuation time of 6ns rather than 5ms. This can significantly speed up test time.

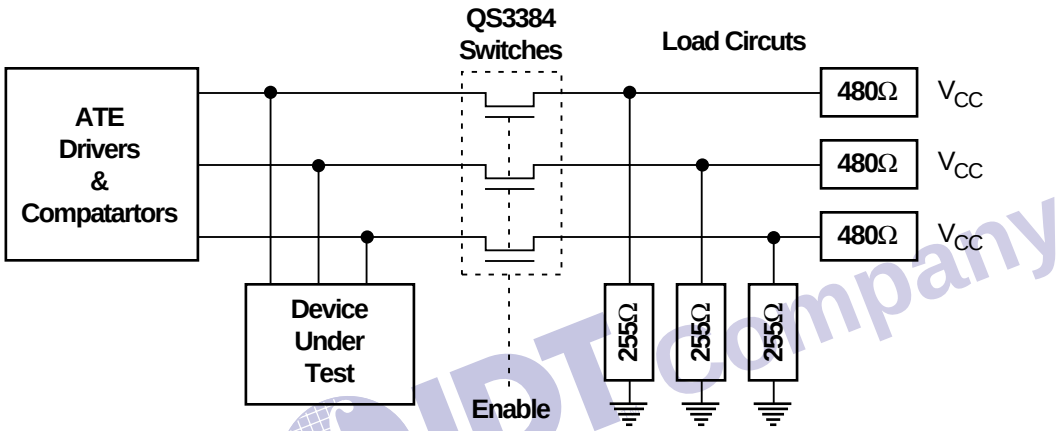

Figure 12 QS3384 ATE Load Switch

Conclusion

The QS3383 and QS3384 bus switches are new tools for the system designer. They can be used to reduce propagation delay and to create high-speed systems with simplified interfaces, improved timing margins and reduced noise.