



Programmable Timing Control Hub™ for Next Gen P4™ processor

Recommended Application:

CK409 Compliant clock for Next Gen P4 Processor

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 1 - 0.7V current-mode differential SRC pair
- 9 - PCI, 3 free running, 33MHz
- 3 - REF, 14.318MHz
- 3 - 3V66, 66.66MHz
- 1 - VCH/3V66, selectable 48MHz or 66MHz
- 2 - 48MHz
- 1 - 24/48MHz

Key Specifications:

- CPU/SRC outputs cycle-cycle jitter < 125ps
- 3V66 outputs cycle-cycle jitter < 250ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 300ppm frequency accuracy on CPU & SRC clocks

Features/Benefits:

- QuadRom™ frequency selection.
- Programmable output frequency.
- Programmable asynchronous 3V66&PCI frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Uses external 14.318MHz reference input.
- Supports tight ppm accuracy clocks for Serial-ATA
- Supports spread spectrum modulation, 0 to -0.5% down spread and +/- 0.25% center spread
- Supports CPU clks up to 400MHz

Functionality

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz
0	0	0	0	0	100.00	66.66	33.33
0	0	0	0	1	200.00	66.66	33.33
0	0	0	1	0	133.33	66.66	33.33
0	0	0	1	1	166.67	66.66	33.33
0	0	1	0	0	200.00	66.66	33.33
0	0	1	0	1	400.00	66.66	33.33
0	0	1	1	0	266.67	66.66	33.33
0	0	1	1	1	333.33	66.66	33.33
0	1	0	0	0	100.99	67.33	33.66
0	1	0	0	1	201.98	67.33	33.66
0	1	0	1	0	134.65	67.33	33.66
0	1	0	1	1	168.31	67.32	33.66
0	1	1	0	0	115.00	76.66	38.33
0	1	1	0	1	230.00	76.66	38.33
0	1	1	1	0	153.33	76.66	38.33
0	1	1	1	1	191.67	76.66	38.33
1	0	0	0	0	100.00	66.66	33.33
1	0	0	0	1	200.00	66.66	33.33
1	0	0	1	0	133.33	66.66	33.33
1	0	0	1	1	166.67	71.43	35.71
1	0	1	0	0	200.00	66.66	33.33
1	0	1	0	1	400.00	66.66	33.33
1	0	1	1	0	266.67	66.66	33.33
1	0	1	1	1	333.33	66.66	33.33
1	1	0	0	0	105.00	69.99	35.00
1	1	0	0	1	210.00	69.99	35.00
1	1	0	1	0	140.00	69.99	35.00
1	1	0	1	1	175.00	69.99	35.00
1	1	1	0	0	110.00	73.33	36.66
1	1	1	0	1	220.00	73.33	36.66
1	1	1	1	0	146.66	73.33	36.66
1	1	1	1	1	183.34	73.33	36.66

Pin Configuration

*FS1/REF0	1	48	VDDA
*FS0/REF1	2	47	GND
REF2	3	46	IREF
VDDREF	4	45	Reset#
X1	5	44	GND
X2	6	43	CPUCLKT1
GND	7	42	CPUCLKC1
**FS2/PCICLK_F0	8	41	VDDCPU
**FS4/PCICLK_F1	9	40	CPUCLKT0
PCICLK_F2	10	39	CPUCLKC0
VDDPCI	11	38	GND
GND	12	37	SRCCLKT
^PCICLK0	13	36	SRCCLKC
PCICLK1	14	35	VDD
PCICLK2	15	34	VttPWR_GD/PD#
PCICLK3	16	33	SDATA
VDDPCI	17	32	SCLK
GND	18	31	3V66_0
PCICLK4	19	30	3V66_1
PCICLK5	20	29	GND
**Sel24_48#/24_48MHz	21	28	VDD3V66
**FS3/48MHz_0	22	27	3V66_2
48MHz_1	23	26	3V66_3/VCH
GND	24	25	VDD48

* This pin have 120K pull-up to VDD

** This pin have 120K pull-down to GND

^^ An external 2.2K pull-down resistor is needed on this pin

48-pin SSOP

Note: FS1 and FS0 are equal to Intel CK409-defined FSA and FSB, respectively.

Pin Description

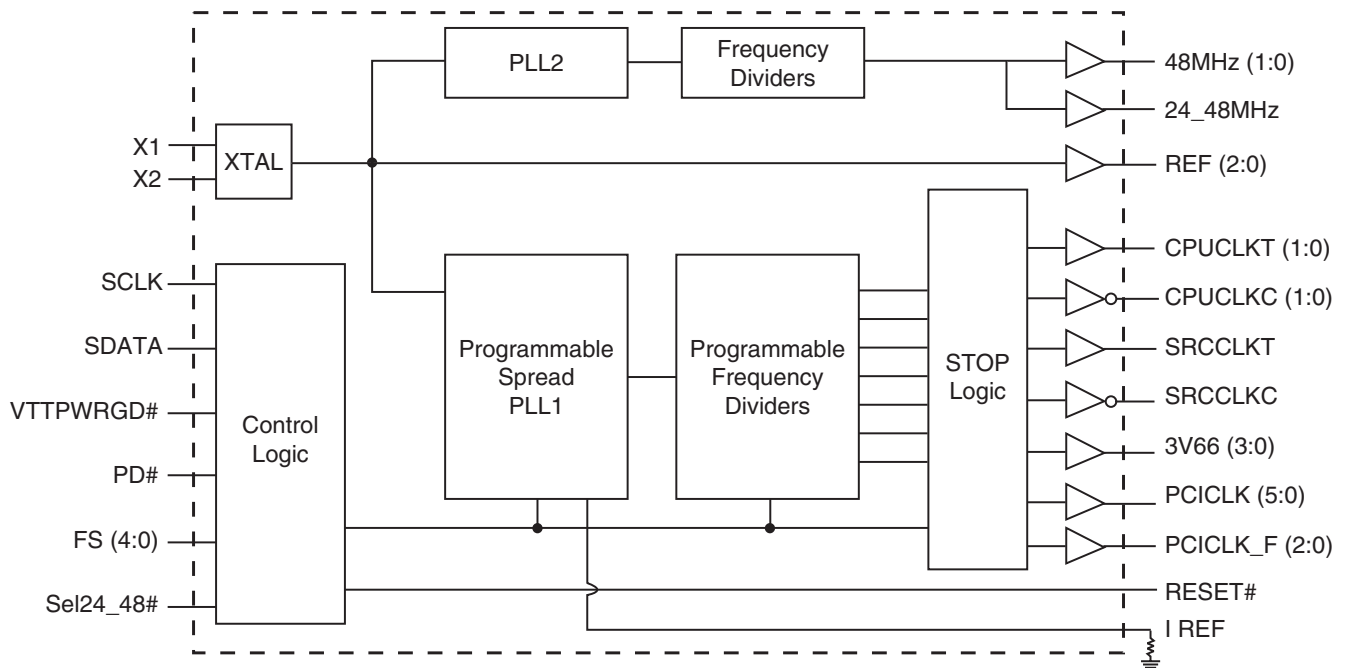
PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	*FS1/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
2	*FS0/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
3	REF2	OUT	14.318 MHz reference clock.
4	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
5	X1	IN	Crystal input, nominally 14.318MHz.
6	X2	OUT	Crystal output, Nominally 14.318MHz
7	GND	PWR	Ground pin.
8	**FS2/PCICLK_F0	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
9	**FS4/PCICLK_F1	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
10	PCICLK_F2	OUT	Free running PCI clock not affected by PCI_STOP#.
11	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
12	GND	PWR	Ground pin.
13	^PCICLK0	OUT	PCI clock output.
14	PCICLK1	OUT	PCI clock output.
15	PCICLK2	OUT	PCI clock output.
16	PCICLK3	OUT	PCI clock output.
17	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
18	GND	PWR	Ground pin.
19	PCICLK4	OUT	PCI clock output.
20	PCICLK5	OUT	PCI clock output.
21	**Sel24_48#/24_48MHz	I/O	Latched select input for 24/48MHz output / 24/48MHz clock output. 1=24mHz, 0 = 48MHz.
22	**FS3/48MHz_0	I/O	Frequency select latch input pin / Fixed 48MHz clock output. 3.3V
23	48MHz_1	OUT	48MHz clock output.
24	GND	PWR	Ground pin.
25	VDD48	PWR	Power for 24 & 48MHz output buffers and fixed PLL core.
26	3V66_3/VCH	OUT	3.3V 66.66MHz clock output / 48MHz VCH clock output.
27	3V66_2	OUT	3.3V 66.66MHz clock output
28	VDD3V66	PWR	Power pin for the 3V66 clocks.
29	GND	PWR	Ground pin.
30	3V66_1	OUT	3.3V 66.66MHz clock output
31	3V66_0	OUT	3.3V 66.66MHz clock output
32	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
33	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
34	VttPWR_GD/PD#	IN	This 3.3V LVTTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. / Asynchronous active low input pin used to power down the device into a low power state.
35	VDD	PWR	Power supply, nominal 3.3V
36	SRCCLKC	OUT	Complement clock of differential pair for S-ATA support. +/- 300ppm accuracy required.
37	SRCCLKT	OUT	True clock of differential pair for S-ATA support. +/- 300ppm accuracy required.
38	GND	PWR	Ground pin.
39	CPUCLKC0	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
40	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
41	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
42	CPUCLKC1	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
43	CPUCLKT1	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
44	GND	PWR	Ground pin.
45	Reset#	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
46	IREF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
47	GND	PWR	Ground pin.
48	VDDA	PWR	3.3V power for the PLL core.

General Description

ICS952607 is a 48 pin clock chip following Intel CK409 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS952607** is driven with a 14.318MHz crystal. It generates CPU outputs up to 200MHz. It also provides a tight ppm accuracy output for Serial ATA support.

The **ICS952607** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I²C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment. This part also provides 128 frequency selections via ICS QuadROM™ technology as an alternate to M/N programming.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
4	7	Xtal, Ref
28	29	3V66
11,17	12,18	PCICLK outputs
35	38	SRCCLK outputs
41	44	CPU outputs
48	47	MCLK, CPU Analog, CPU digital
25	24	48MHz Fix, Fix Digital, Fix analog

Table1: QuadRom Frequency Selection Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI	Spread
		FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	%
0	0	0	0	0	0	0	100.00	66.66	33.33	0 to -0.5% Down
0	0	0	0	0	0	1	200.00	66.66	33.33	0 to -0.5% Down
0	0	0	0	0	1	0	133.33	66.66	33.33	0 to -0.5% Down
0	0	0	0	0	1	1	166.67	66.66	33.33	0 to -0.5% Down
0	0	0	0	1	0	0	200.00	66.66	33.33	0 to -0.5% Down
0	0	0	0	1	0	1	400.00	66.66	33.33	0 to -0.5% Down
0	0	0	0	1	1	0	266.67	66.66	33.33	0 to -0.5% Down
0	0	0	0	1	1	1	333.33	66.66	33.33	0 to -0.5% Down
0	0	0	1	0	0	0	100.99	67.33	33.66	0.35% Center
0	0	0	1	0	0	1	201.98	67.33	33.66	0.35% Center
0	0	0	1	0	1	0	134.65	67.33	33.66	0.35% Center
0	0	0	1	0	1	1	168.31	67.32	33.66	0.35% Center
0	0	0	1	1	0	0	115.00	76.66	38.33	No Spread
0	0	0	1	1	0	1	230.00	76.66	38.33	No Spread
0	0	0	1	1	1	0	153.33	76.66	38.33	No Spread
0	0	0	1	1	1	1	191.67	76.66	38.33	No Spread
0	0	1	0	0	0	0	100.00	66.66	33.33	0.35% Center
0	0	1	0	0	0	1	200.00	66.66	33.33	0.35% Center
0	0	1	0	0	1	0	133.33	66.66	33.33	0.35% Center
0	0	1	0	0	1	1	166.67	71.43	35.71	0.35% Center
0	0	1	0	1	0	0	200.00	66.66	33.33	0.35% Center
0	0	1	0	1	0	1	400.00	66.66	33.33	0.35% Center
0	0	1	0	1	1	0	266.67	66.66	33.33	0.35% Center
0	0	1	0	1	1	1	333.33	66.66	33.33	0.35% Center
0	0	1	1	0	0	0	105.00	69.99	35.00	No Spread
0	0	1	1	0	0	1	210.00	69.99	35.00	No Spread
0	0	1	1	0	1	0	140.00	69.99	35.00	No Spread
0	0	1	1	0	1	1	175.00	69.99	35.00	No Spread
0	0	1	1	1	0	0	110.00	73.33	36.66	No Spread
0	0	1	1	1	0	1	220.00	73.33	36.66	No Spread
0	0	1	1	1	1	0	146.66	73.33	36.66	No Spread
0	0	1	1	1	1	1	183.34	73.33	36.66	No Spread

Table continued on next page.

Table1: QuadRom Frequency Selection Table (Continued)

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI	Spread
		FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	%
0	1	0	0	0	0	0	103.00	68.66	34.33	No Spread
0	1	0	0	0	0	1	206.00	68.66	34.33	No Spread
0	1	0	0	0	1	0	137.33	68.66	34.33	No Spread
0	1	0	0	0	1	1	171.67	68.66	34.33	No Spread
0	1	0	0	1	0	0	228.89	68.66	34.33	No Spread
0	1	0	0	1	0	1	412.00	68.66	34.33	No Spread
0	1	0	0	1	1	0	274.67	68.66	34.33	No Spread
0	1	0	0	1	1	1	343.33	68.66	34.33	No Spread
0	1	0	1	0	0	0	105.00	69.99	35.00	No Spread
0	1	0	1	0	0	1	210.00	69.99	35.00	No Spread
0	1	0	1	0	1	0	140.00	69.99	35.00	No Spread
0	1	0	1	0	1	1	175.00	69.99	35.00	No Spread
0	1	0	1	1	0	0	233.33	69.99	35.00	No Spread
0	1	0	1	1	0	1	420.00	69.99	35.00	No Spread
0	1	0	1	1	1	0	280.00	69.99	35.00	No Spread
0	1	0	1	1	1	1	350.00	69.99	35.00	No Spread
0	1	1	0	0	0	0	107.00	71.33	35.66	No Spread
0	1	1	0	0	0	1	214.00	71.33	35.66	No Spread
0	1	1	0	0	1	0	142.66	71.33	35.66	No Spread
0	1	1	0	0	1	1	178.34	71.33	35.66	No Spread
0	1	1	0	1	0	0	237.78	71.33	35.66	No Spread
0	1	1	0	1	0	1	428.00	71.33	35.66	No Spread
0	1	1	0	1	1	0	285.34	71.33	35.66	No Spread
0	1	1	0	1	1	1	356.66	71.33	35.66	No Spread
0	1	1	1	0	0	0	110.00	73.33	36.66	No Spread
0	1	1	1	0	0	1	220.00	73.33	36.66	No Spread
0	1	1	1	0	1	0	146.66	73.33	36.66	No Spread
0	1	1	1	0	1	1	183.34	73.33	36.66	No Spread
0	1	1	1	1	0	0	244.44	73.33	36.66	No Spread
0	1	1	1	1	0	1	440.00	73.33	36.66	No Spread
0	1	1	1	1	1	0	293.34	73.33	36.66	No Spread
0	1	1	1	1	1	1	366.66	73.33	36.66	No Spread

Table continued on next page.

Table1: QuadRom Frequency Selection Table 3 (Continued)

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI	Spread
		FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	%
1	0	0	0	0	0	0	95.00	63.33	31.66	No Spread
1	0	0	0	0	0	1	190.00	63.33	31.66	No Spread
1	0	0	0	0	1	0	126.66	63.33	31.66	No Spread
1	0	0	0	0	1	1	158.34	63.33	31.66	No Spread
1	0	0	0	1	0	0	211.11	63.33	31.66	No Spread
1	0	0	0	1	0	1	380.00	63.33	31.66	No Spread
1	0	0	0	1	1	0	253.34	63.33	31.66	No Spread
1	0	0	0	1	1	1	316.66	63.33	31.66	No Spread
1	0	0	1	0	0	0	90.00	59.99	30.00	No Spread
1	0	0	1	0	0	1	180.00	59.99	30.00	No Spread
1	0	0	1	0	1	0	120.00	59.99	30.00	No Spread
1	0	0	1	0	1	1	150.00	59.99	30.00	No Spread
1	0	0	1	1	0	0	200.00	59.99	30.00	No Spread
1	0	0	1	1	0	1	360.00	59.99	30.00	No Spread
1	0	0	1	1	1	0	240.00	59.99	30.00	No Spread
1	0	0	1	1	1	1	300.00	59.99	30.00	No Spread
1	0	1	0	0	0	0	85.00	56.66	28.33	No Spread
1	0	1	0	0	0	1	170.00	56.66	28.33	No Spread
1	0	1	0	0	1	0	113.33	56.66	28.33	No Spread
1	0	1	0	0	1	1	141.67	56.66	28.33	No Spread
1	0	1	0	1	0	0	188.89	56.66	28.33	No Spread
1	0	1	0	1	0	1	340.00	56.66	28.33	No Spread
1	0	1	0	1	1	0	226.67	56.66	28.33	No Spread
1	0	1	0	1	1	1	283.33	56.66	28.33	No Spread
1	0	1	1	0	0	0	80.00	53.33	26.66	No Spread
1	0	1	1	0	0	1	160.00	53.33	26.66	No Spread
1	0	1	1	0	1	0	106.66	53.33	26.66	No Spread
1	0	1	1	0	1	1	133.34	53.33	26.66	No Spread
1	0	1	1	1	0	0	177.78	53.33	26.66	No Spread
1	0	1	1	1	0	1	320.00	53.33	26.66	No Spread
1	0	1	1	1	1	0	213.34	53.33	26.66	No Spread
1	0	1	1	1	1	1	266.66	53.33	26.66	No Spread

Table continued on next page.

Table1: QuadRom Frequency Selection Table 4 (Continued)

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI	Spread
		FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	%
1	1	0	0	0	0	0	115.00	76.66	38.33	No Spread
1	1	0	0	0	0	1	230.00	76.66	38.33	No Spread
1	1	0	0	0	1	0	153.33	76.66	38.33	No Spread
1	1	0	0	0	1	1	191.67	76.66	38.33	No Spread
1	1	0	0	1	0	0	255.55	76.66	38.33	No Spread
1	1	0	0	1	0	1	460.00	76.66	38.33	No Spread
1	1	0	0	1	1	0	306.67	76.66	38.33	No Spread
1	1	0	0	1	1	1	383.33	76.66	38.33	No Spread
1	1	0	1	0	0	0	115.00	79.99	40.00	No Spread
1	1	0	1	0	0	1	230.00	79.99	40.00	No Spread
1	1	0	1	0	1	0	153.33	79.99	40.00	No Spread
1	1	0	1	0	1	1	191.67	79.99	40.00	No Spread
1	1	0	1	1	0	0	255.55	79.99	40.00	No Spread
1	1	0	1	1	0	1	460.00	79.99	40.00	No Spread
1	1	0	1	1	1	0	306.67	79.99	40.00	No Spread
1	1	0	1	1	1	1	383.33	79.99	40.00	No Spread
1	1	1	0	0	0	0	78.00	51.99	26.00	No Spread
1	1	1	0	0	0	1	156.00	51.99	26.00	No Spread
1	1	1	0	0	1	0	104.00	51.99	26.00	No Spread
1	1	1	0	0	1	1	130.00	51.99	26.00	No Spread
1	1	1	0	1	0	0	173.33	51.99	26.00	No Spread
1	1	1	0	1	0	1	312.00	51.99	26.00	No Spread
1	1	1	0	1	1	0	208.00	51.99	26.00	No Spread
1	1	1	0	1	1	1	260.00	51.99	26.00	No Spread
1	1	1	1	0	0	0	75.00	50.00	25.00	No Spread
1	1	1	1	0	0	1	150.00	50.00	25.00	No Spread
1	1	1	1	0	1	0	100.00	50.00	25.00	No Spread
1	1	1	1	0	1	1	125.00	50.00	25.00	No Spread
1	1	1	1	1	0	0	166.67	50.00	25.00	No Spread
1	1	1	1	1	0	1	300.00	50.00	25.00	No Spread
1	1	1	1	1	1	0	200.00	50.00	25.00	No Spread
1	1	1	1	1	1	1	250.00	50.00	25.00	No Spread

General I²C serial interface information for the ICS952607

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2 _(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N		
		ACK
○		
○		○
○		○
		○
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2 _(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address D3 _(H)		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
ACK		
○		
○		
○		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

I²C Table: Frequency Select Register

Byte 0		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-		FS6	Freq Select Bit 6	RW	See Table 1: QuadRom Frequency Selection Table		0
Bit 5	-		FS5	Freq Select Bit 5	RW			0
Bit 4	-		FS4	Freq Select Bit 4	RW			0
Bit 3	-		FS3	Freq Select Bit 3	RW			0
Bit 2	-		FS2	Freq Select Bit 2	RW			0
Bit 1	-		FSA	Freq Select Bit 1	RW			0
Bit 0	-		FSB	Freq Select Bit 0	RW			0

I²C Table: Spreading and Device Behavior Control Register

Byte 1		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		SS1	Spread Select 1	RW	00 = 0.35%	10 = 0.75%	0
Bit 6	-		SS0	Spread Select 0	RW	01 = 0.50%	11 = No Spread	0
Bit 5	-		SS_EN	Spread Enable Control	RW	ON	OFF	1
Bit 4	-		WDS_EN	WD Soft Reset Enable	RW	ON	OFF	0
Bit 3	37,36		SRC/SRC#	Output Control	RW	Disable	Enable	1
Bit 2	-		Reserved	Reserved	RW	-	-	1
Bit 1	43,42		CPUCLKT/C_1	Output Control	RW	Disable	Enable	1
Bit 0	40,39		CPUCLKT/C_0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 2		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		SRC Stop Mode	0: SRCT Driven during PD#; 1: Tri-stated	RW	Driven	Hi-Z	0
Bit 6	-		Reserved	Reserved	RW	-	-	0
Bit 5	-		CPUT Stop Mode	0: CPUT Driven during PD#; 1: Tri-stated	RW	Driven	Hi-Z	0
Bit 4	-		Reserved	Reserved	RW	-	-	0
Bit 3	27		3V66_2	Output Control	RW	Disable	Enable	1
Bit 2	-		Reserved	Reserved	RW	-	-	1
Bit 1	-		Reserved	Reserved	RW	-	-	1
Bit 0	-		Reserved	Reserved	RW	-	-	1

I²C Table: Output Control Register

Byte 3		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		ASEL1	3V66/PCI Freq Select	RW	See Table 5: Async AGP/PCI Freq Table		0
Bit 6	-		Reserved	Reserved	RW	-	-	0
Bit 5	20		PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	19		PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	16		PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	15		PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	14		PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	13		PCICLK0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 4		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7			48MHz_0 2x output drive	0=2x drive	RW	2x drive	normal	0
Bit 6			SRCFS	SRC Frequency Select	-	100MHz	200MHz	0
Bit 5			Reserved	Reserved	RW	-	-	0
Bit 4	30		3V66_1	Output Control	RW	Disable	Enable	1
Bit 3	31		3V66_0	Output Control	RW	Disable	Enable	1
Bit 2	10		PCICLK_F2	Output Control	RW	Disable	Enable	1
Bit 1	9		PCICLK_F1	Output Control	RW	Disable	Enable	1
Bit 0	8		PCICLK_F0	Output Control	RW	Disable	Enable	1

I²C Table: Reserved Register

Byte 5		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		3V66_3/VCH Select	Output Select	RW	3V66	VCH	0
Bit 6	-		Mode Sel1	PLL Mode Selection Bits	RW	See Table 4: Mode Selection Table		0
Bit 5	-		Mode Sel0		RW			0
Bit 4	26		3V66_3/VCH	Output Control	RW	Disable	Enable	1
Bit 3	-		M PLL2 Div3	M Divider Programming bits for Async mode 2&3	RW	The decimal representation of M PLL2 Div (3:0) + 2 is equal to REF divider value for PLL2		X
Bit 2	-		M PLL2 Div2		RW			X
Bit 1	-		M PLL2 Div1		RW			X
Bit 0	-		M PLL2 Div0		RW			X

Table 3: Linear M/N AGP/PCI Programmable Frequency Example

Hex B5b3:0	Hex B6b6:0	AGP Freq	PCI Freq	Hex B5b3:0	Hex B6b6:0	AGP Freq	PCI Freq
C	31	65.15	32.58	C	33	67.44	33.72
B	2D	65.24	32.62	7	1E	67.57	33.78
A	29	65.34	32.67	B	2F	67.70	33.85
7	1D	65.79	32.89	A	2B	68.01	34.01
6	19	66.01	33.01	C	34	68.58	34.29
D	36	66.14	33.07	B	30	68.93	34.47
C	32	66.30	33.15	A	2C	69.34	34.67
B	2E	66.47	33.24	C	35	69.73	34.86
A	2A	66.68	33.34	9	28	69.83	34.91
D	37	67.21	33.61	6	1B	70.01	35.01

Table 4: Mode Selection Table

Mode	Standard Overclock Mode	CPU Overclock Mode	Graphic Overclock Mode
IIC Control	Byte 5 bit(6:5) = 00	Byte 5 bit(6:5) = 01	Byte 5 bit(6:5) = 10
CPU M/N Overclocking	Byte 11 & 12	Byte 11 & 12	Byte 11 & 12
SRC M/N Overclocking	Byte 11 & 12	Byte 5 & 6 (asynchronous)	Byte 11 & 12
AGP/PCI M/N Overclocking	Byte 11 & 12	Byte 5 & 6 (asynchronous)	Byte 5 & 6 (asynchronous)
Spreading	All clocks have spread.	Only CPU clocks have spread.	Latch input should be set as FS(4:0) = 10xxx. CPU & SRC have spread.
Remark	All clocks overlock together by Byte 11&12 M/N programming.	CPU overlock by Byte 11&12 SRC/AGP/PCI overlock by Byte 5&6 asynchronously.	CPU/SRC overlock by Byte 11&12 AGP/PCI overlock by Byte 5&6 asynchronously.
Mode B (B6&B3 bit 7) AGP/PCI can be selected to be overlock from 66/33, 72/36 or 80/40.	Simple async AGP/PCI overlocking w/o using M/N programming.	SRC can be kept at 100 w/o spread yet AGP/PCI can be overlocked.	Simple async AGP/PCI overlocking w/o using M/N programming.

Table 5: Asynchronous 3V66/PCI Frequency Table

Byte6 Bit7	Byte3 Bit7	3V66/PCI Frequency
0	0	66.66/33.33
0	1	80.00/40.00
1	0	72.73/36.36

I²C Table: Vendor & Revision ID Register

Byte 6		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	-	ASEL0	3V66/PCI Freq Select	RW	See Table 4: Async AGP/PCI Freq Table		0
Bit 6	-	-	N PLL2 Div6	N Divider Programming bits for Async mode 2&3	RW	The decimal representation of N PLL2 Div (6:0) + 8 is equal to VCO divider value for PLL2.		X
Bit 5	-	-	N PLL2 Div5		RW			X
Bit 4	-	-	N PLL2 Div4		RW			X
Bit 3	-	-	N PLL2 Div3		RW			X
Bit 2	-	-	N PLL2 Div2		RW			X
Bit 1	-	-	N PLL2 Div1		RW			X
Bit 0	-	-	N PLL2 Div0		RW			X

I²C Table: Vendor & Revision ID Register

Byte 7		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	-	RID2		R	-	-	X
Bit 5	-	-	RID1		R	-	-	X
Bit 4	-	-	RID0		R	-	-	X
Bit 3	-	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	-	VID2		R	-	-	0
Bit 1	-	-	VID1		R	-	-	0
Bit 0	-	-	VID0		R	-	-	1

I²C Table: Byte Count Register

Byte 8		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	-	-	BC6		RW			0
Bit 5	-	-	BC5		RW			0
Bit 4	-	-	BC4		RW			0
Bit 3	-	-	BC3		RW			1
Bit 2	-	-	BC2		RW			1
Bit 1	-	-	BC1		RW			1
Bit 0	-	-	BC0		RW			1

I²C Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WD7	WD Timer Bit 7	RW	These bits represent X*290ms the watchdog timer waits before it goes to alarm mode. Default is 11 x 293ms = 3.2s.		0
Bit 6	-	WD6	WD Timer Bit 6	RW			0
Bit 5	-	WD5	WD Timer Bit 5	RW			0
Bit 4	-	WD4	WD Timer Bit 4	RW			0
Bit 3	-	WD3	WD Timer Bit 3	RW			1
Bit 2	-	WD2	WD Timer Bit 2	RW			0
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	WDEN	Watchdog Enable	R	Disable	Enable	1
Bit 5	-	WDFSEN	WD Safe Frequency Mode	RW	Latched FS/Byte0	WD B10 b(4:0)	0
Bit 4	-	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte0 bit (4:0).		0
Bit 3	-	WD SF3		RW			0
Bit 2	-	WD SF2		RW			0
Bit 1	-	WD SF1		RW			0
Bit 0	-	WD SF0		RW			0

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(8:0)+8] / [MDiv(6:0)+2]		X
Bit 6	-	M Div6	M Divider Programming bits	RW			X
Bit 5	-	M Div5		RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(8:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(8:0)+8] / [MDiv(6:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 14		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Reserved	Reserved	R	-	-	0
Bit 6	-		Reserved	Reserved	R	-	-	0
Bit 5	-		SSP13	Spread Spectrum Programming b(13:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 4	-		SSP12		RW			X
Bit 3	-		SSP11		RW			X
Bit 2	-		SSP10		RW			X
Bit 1	-		SSP9		RW			X
Bit 0	-		SSP8		RW			X

I²C Table: Output Divider Control Register

Byte 15		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		SRC Div3	SRC Divider Ratio Programmaing Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-		SRC Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-		SRC Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-		SRC Div0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X
Bit 3	-		CPU Div3	CPUDivider Ratio Programmaing Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-		CPU Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-		CPU Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-		CPU Div0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I²C Table: Output Divider Control Register

Byte 16		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		Reserved	Reserved	RW	-		-		X
Bit 6	-		Reserved	Reserved	RW	-		-		X
Bit 5	-		Reserved	Reserved	RW	-		-		X
Bit 4	-		Reserved	Reserved	RW	-		-		X
Bit 3	-		3V66Div3	3V66 Divider Ratio Programmaing Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-		3V66Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-		3V66Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-		3V66Div0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I²C Table: Output Divider Control Register

Byte 17		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Reserved	Reserved	RW	-	-	X
Bit 6	-		3V66INV	3V66 Phase Invert	RW	Default	Inverse	X
Bit 5	-		SRCINV	SRC Phase Invert	RW	Default	Inverse	X
Bit 4	-		CPUINV	CPU Phase Invert	RW	Default	Inverse	X
Bit 3	-		Reserved	Reserved	RW	-	-	0
Bit 2	-		Reserved	Reserved	RW	-	-	0
Bit 1	-		Reserved	Reserved	RW	-	-	0
Bit 0	-		Reserved	Reserved	RW	-	-	0

I²C Table: Group Skew Control Register

Byte 18		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Reserved	Reserved	RW	-	-	0
Bit 6	-		Reserved	Reserved	RW	-	-	0
Bit 5	-		Reserved	Reserved	RW	-	-	0
Bit 4	-		Reserved	Reserved	RW	-	-	0
Bit 3	-		Reserved	Reserved	RW	-	-	0
Bit 2	-		Reserved	Reserved	RW	-	-	0
Bit 1	-		Reserved	Reserved	RW	-	-	0
Bit 0	-		Reserved	Reserved	RW	-	-	0

I²C Table: Group Skew Control Register

Byte 19		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		3V66Skw3	CPU-3V66 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	0
Bit 6	-		3V66Skw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	0
Bit 5	-		3V66Skw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 4	-		3V66Skw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0
Bit 3	-		PCISkw3	CPU-PCI 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	1
Bit 2	-		PCISkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	1
Bit 1	-		PCISkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 0	-		PCISkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0

I²C Table: Group Skew Control Register

Byte 20		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		PCISkw3	CPU-PCI F(2:0) 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	1
Bit 6	-		PCISkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	1
Bit 5	-		PCISkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 4	-		PCISkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0
Bit 3	-		Reserved	Reserved	RW	-	-	-	-	0
Bit 2	-		Reserved	Reserved	RW	-	-	-	-	0
Bit 1	-		Reserved	Reserved	RW	-	-	-	-	0
Bit 0	-		Reserved	Reserved	RW	-	-	-	-	0

I²C Table: Slew Rate Control Register

Byte 21		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		PCIFStr1	PCICLK (2:0) Strength Control	RW	00 = 0.63X		10 = 0.88X		1
Bit 6	-		PCIFStr0			01 = 0.75X		11 = 1.00X		1
Bit 5	-		Reserved	Reserved	RW	-		-		1
Bit 4	-		Reserved	Reserved	RW	-		-		1
Bit 3	-		Reserved	Reserved	RW	-		-		1
Bit 2	-		Reserved	Reserved	RW	-		-		1
Bit 1	-		AGPStr1	AGPCLK Strength Control	RW	00 = 0.70X		10 = 0.90X		1
Bit 0	-		AGPStr0			01 = 0.80X		11 = 1.00X		1

I²C Table: Slew Rate Control Register

Byte 22		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		REF_Slw	REF Slew Rate Control	RW	00 = Medium		10 = Strong		1
Bit 6	-				RW	01 = Weak		11 = N/A		0
Bit 5	-		PCIFStr1	PCICLK (5) Strength Control	RW	00 = 0.63X		10 = 0.88X		1
Bit 4	-		PCIFStr0			01 = 0.75X		11 = 1.00X		1
Bit 3	-		PCIFStr1	PCICLK (4:2) Strength Control	RW	00 = 0.63X		10 = 0.88X		1
Bit 2	-		PCIFStr0			01 = 0.75X		11 = 1.00X		1
Bit 1	-		PCIFStr1	PCICLK (1:0) Strength Control	RW	00 = 0.63X		10 = 0.88X		1
Bit 0	-		PCIFStr0			01 = 0.75X		11 = 1.00X		1

I²C Table: Output Control Register

Byte 23		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	22		48MHz_0	Output Control	RW	Disable		Enable		1
Bit 6	21		24_48MHz	Output Control	RW	Disable		Enable		1
Bit 5	2		REF1	Output Control	RW	Disable		Enable		1
Bit 4	1		REF0	Output Control	RW	Disable		Enable		1
Bit 3	3		REF2	Output Control	RW	Disable		Enable		1
Bit 2	23		48MHz_1	Output Control	RW	Disable		Enable		1
Bit 1	-		Reserved	Reserved	RW	-		-		0
Bit 0	-		Reserved	Reserved	RW	-		-		0

I²C Table: Read Back Register

Byte 24		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		WDHRB	WD Hard Alarm Status Read back	R	-	-	X
Bit 6	-		WDSRB	WD Soft Alarm Status Read back	R	-	-	X
Bit 5	-		Reserved	Reserved	R	-	-	0
Bit 4	-		FS4RB	FS4 Read back	R	-	-	X
Bit 3	-		FS3RB	FS3 Read back	R	-	-	X
Bit 2	-		FS2RB	FS2 Read back	R	-	-	X
Bit 1	-		FSARB	FSA Read back	R	-	-	X
Bit 0	-		FSBRB	FSB Read back	R	-	-	X

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

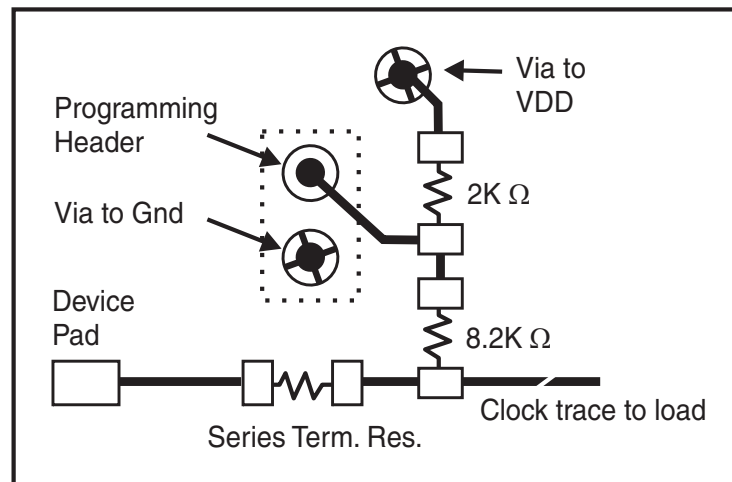


Fig. 1

Absolute Maximum Ratings

Core Supply Voltage	4.6 V
I/O Supply Voltage	3.6V
Logic Inputs	GND –0.5 V to $V_{DD} + 0.5$ V
Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Case Temperature	115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = 3.3$ V $\pm 5\%$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3V $\pm 5\%$	2		$V_{DD} + 0.3$	V	
Input MID Voltage	V_{MID}	3.3V $\pm 5\%$	1		1.8	V	
Input Low Voltage	V_{IL}	3.3V $\pm 5\%$	$V_{SS} - 0.3$		0.8	V	
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	μA	
Input Low Current	I_{IL1}	$V_{IN} = 0$ V; Inputs with no pull-up resistors	-5			μA	
	I_{IL2}	$V_{IN} = 0$ V; Inputs with pull-up resistors	-200			μA	
Operating Supply Current	$I_{DD3.3OP}$	Full Active, $C_L = \text{Full load}$;			350	mA	
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			35	mA	
		all differential pairs tri-stated			12	mA	
Input Frequency ³	F_i	$V_{DD} = 3.3$ V		14.31818		MHz	3
Pin Inductance ¹	L_{pin}				7	nH	1
Input Capacitance ¹	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX} ⁴	X1 & X2 pins			5	pF	1
Clk Stabilization ^{1,2}	T_{STAB}	From VDD Power-Up or de-assertion of PD# to 1st clock.			1.8	ms	1,2
Modulation Frequency		Triangular Modulation	30		33	kHz	1

¹Guaranteed by design, not 100% tested in production.

²See timing diagrams for timing requirements.

³Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

⁴Crystal recommendations: $C_L = 20\text{pF}$ and Shunt cap. Max = 5pF.

Electrical Characteristics - CPU & SRC 0.7V Current Mode Differential Pair

$T_A = 0 - 70^{\circ}\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 2\text{pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Z_o^1	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1
Voltage Low	VLow		-150		150		1
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Rise Time	t_r	$V_{OL} = 0.175\text{V}$, $V_{OH} = 0.525\text{V}$	175		700	ps	1
Fall Time	t_f	$V_{OH} = 0.525\text{V}$, $V_{OL} = 0.175\text{V}$	175		700	ps	1
Rise Time Variation	d- t_r				125	ps	1
Fall Time Variation	d- t_f				125	ps	1
Duty Cycle	d_{i3}	Measurement from differential waveform	45		55	%	1
Skew	t_{sk3}	$V_T = 50\%$			100	ps	1
Jitter, Cycle to cycle	$t_{jcy-cyc}$	Measurement from differential waveform			125	ps	1

¹Guaranteed by design, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

SRC clock outputs run at only 100MHz or 200MHz, specs for 133.33 and 166.66 do not apply to SRC clock pair.

Electrical Characteristics - 3V66

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10\text{-}30\text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Output High Voltage	V_{OH}	$I_{OH} = -1\text{ mA}$	2.4			V	
Output Low Voltage	V_{OL}	$I_{OL} = 1\text{ mA}$			0.55	V	
Output High Current	I_{OH}	$V_{OH@MIN} = 1.0\text{ V}$	-33			mA	
		$V_{OH@MAX} = 3.135\text{ V}$			-33	mA	
Output Low Current	I_{OL}	$V_{OL@MIN} = 1.95\text{ V}$	30			mA	
		$V_{OL@MAX} = 0.4\text{ V}$			38	mA	
Edge Rate		Rising edge rate	1		4	V/ns	1
Edge Rate		Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$	0.5		2	ns	1
Fall Time	t_{f1}	$V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$	0.5		2	ns	1
Duty Cycle	d_{t1}	$V_T = 1.5\text{ V}$	45		55	%	1
Skew	t_{sk1}	$V_T = 1.5\text{ V}$			250	ps	1
Jitter	$t_{jcy-cyc}$	$V_T = 1.5\text{ V}$ 3V66			250	ps	1

¹Guaranteed by design, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

Electrical Characteristics - PCICLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10\text{-}30\text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Output High Voltage	V_{OH}	$I_{OH} = -1\text{ mA}$	2.4			V	
Output Low Voltage	V_{OL}	$I_{OL} = 1\text{ mA}$			0.55	V	
Output High Current	I_{OH}	$V_{OH@MIN} = 1.0\text{ V}$	-33			mA	
		$V_{OH@MAX} = 3.135\text{ V}$			-33	mA	
Output Low Current	I_{OL}	$V_{OL@MIN} = 1.95\text{ V}$	30			mA	
		$V_{OL@MAX} = 0.4\text{ V}$			38	mA	
Edge Rate		Rising edge rate	1		4	V/ns	1
Edge Rate		Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$	0.5		2	ns	1
Fall Time	t_{f1}	$V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$	0.5		2	ns	1
Duty Cycle	d_{t1}	$V_T = 1.5\text{ V}$	45		55	%	1
Skew	t_{sk1}	$V_T = 1.5\text{ V}$			500	ps	1
Jitter	$t_{jcy-cyc}$	$V_T = 1.5\text{ V}$ 3V66			250	ps	1

¹Guaranteed by design, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

Electrical Characteristics - VCH, 48MHz, 24MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10\text{-}20\text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-200		200	ppm	1,2
Output High Voltage	V_{OH}	$I_{OH} = -1\text{ mA}$	2.4			V	
Output Low Voltage	V_{OL}	$I_{OL} = 1\text{ mA}$			0.55	V	
Output High Current	I_{OH}	$V_{OH@MIN} = 1.0\text{ V}$	-33			mA	
		$V_{OH@MAX} = 3.135\text{ V}$			-33	mA	
Output Low Current	I_{OL}	$V_{OL@MIN} = 1.95\text{ V}$	30			mA	
		$V_{OL@MAX} = 0.4\text{ V}$			38	mA	
Edge Rate		Rising edge rate	1		2	V/ns	1
Edge Rate		Falling edge rate	1		2	V/ns	1
Rise Time	t_{r1}	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$	1		2	ns	1
Fall Time	t_{f1}	$V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$	1		2	ns	1
Duty Cycle	d_{t1}	$V_T = 1.5\text{ V}$	45		55	%	1
Skew	t_{sk1}	$V_T = 1.5\text{ V}$			1	ns	1
Long Term Jitter		125us period jitter (8kHz frequency modulation amplitude)			6	ns	1

¹Guaranteed by design, not 100% tested in production.

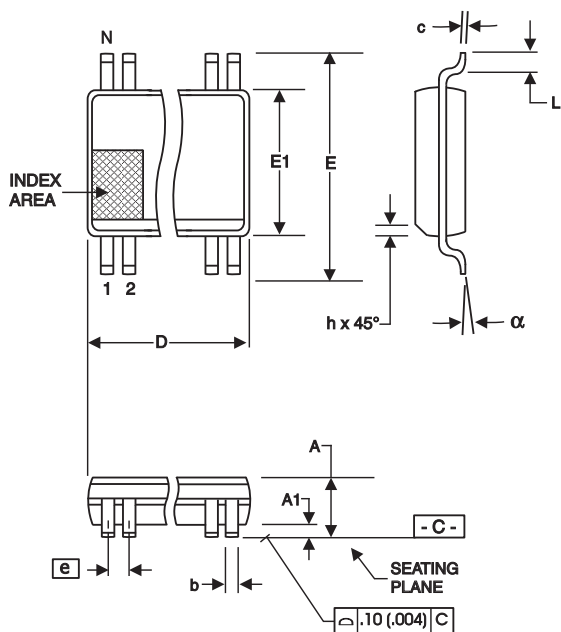
²All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

Electrical Characteristics - REF-14.318MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10\text{-}20\text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1
Output High Voltage	V_{OH}^1	$I_{OH} = -1\text{ mA}$	2.4			V	
Output Low Voltage	V_{OL}^1	$I_{OL} = 1\text{ mA}$			0.4	V	
Output High Current	I_{OH}^1	$V_{OH@MIN} = 1.0\text{ V}$, $V_{OH@MAX} = 3.135\text{ V}$	-29		-23	mA	
Output Low Current	I_{OL}^1	$V_{OL@MIN} = 1.95\text{ V}$, $V_{OL@MAX} = 0.4\text{ V}$	29		27	mA	
Rise Time	t_{r1}^1	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$	1		2	ns	1
Fall Time	t_{f1}^1	$V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$	1		2	ns	1
Skew	t_{sk1}^1	$V_T = 1.5\text{ V}$			500	ps	1
Duty Cycle	d_{t1}^1	$V_T = 1.5\text{ V}$	45		55	%	1
Jitter	$t_{jvc-cvc}^1$	$V_T = 1.5\text{ V}$			1000	ps	1

¹Guaranteed by design, not 100% tested in production.



SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS		COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS952607yFLF-T

Example:

ICS XXXX y F LF-T

Designation for tape and reel packaging

RoHS Compliant (Optional)

Package Type

F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix

ICS = Standard Device

Revision History

Rev.	Issue Date	Description	Page #
A	7/26/2005	1. Added SMBus Slave Address page. 2. Updated LF Ordering Information to RoHS Compliant.	8, 21

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