Single Channel Type-2 M-LVDS to LVTTL Transceiver IDT5V5206

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Single Channel Type-2 M-LVDS to LVTTL Transceiver

IDT5V5206

FEATURES

- **Main Features**
  - –
  - *Type-2 M-LVDS receiver supports 100 mV offset threshold*
  - *Up to 166 MHz LVTTL input/output signal*
  - *M-LVDS interface allows common-mode voltage: -1 V to 3.4 V*
  - *Power up and power down glitch free*
  - *M-LVDS interface pins in high impedance state when the device is powered down or VDD < 1.5 V*
  - *Capable of driving bus load from 30 Ω to 55 Ω*
- **Other Features**
  - *Low power consumption < 120 mW*
  - *Hot swappable*
  - *8-pin SOIC package*

APPLICATIONS

- *Backplane transmission*
- *Telecommunication system*
- *Data communications*
- *ATCA clock distribution*

DESCRIPTION

The IDT5V5206 is a transceiver which can interchange data across multipoint data bus structures.

The device has a LVTTL driver and receiver, a selectable Type-2 M-LVDS receiver and M-LVDS driver. It translates between LVTTL signals and M-LVDS signals. The drivers and the receivers can be enabled or disabled by external pins. The M-LVDS driver is capable of driving bus load from 30 Ω to 55 Ω. The M-LVDS interface allows common-mode voltage range of -1 V to 3.4 V.

FUNCTIONAL BLOCK DIAGRAM

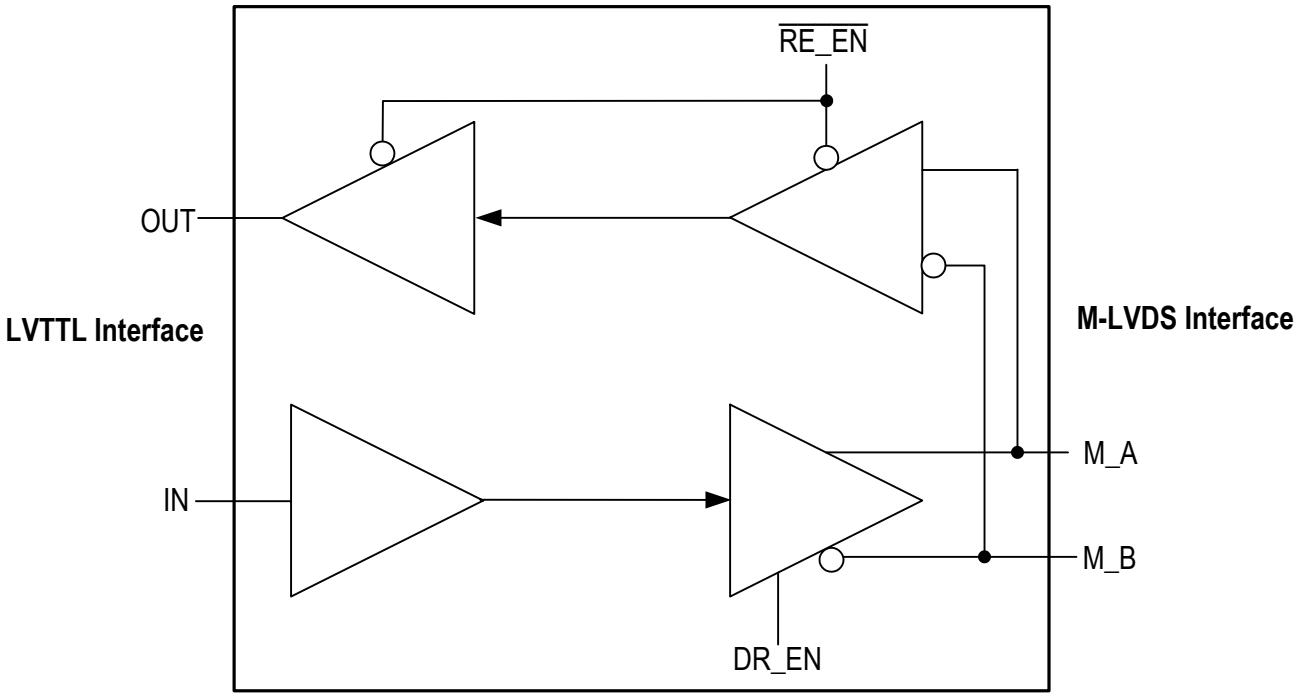


Figure-1 Functional Block Diagram

1 PIN ASSIGNMENT

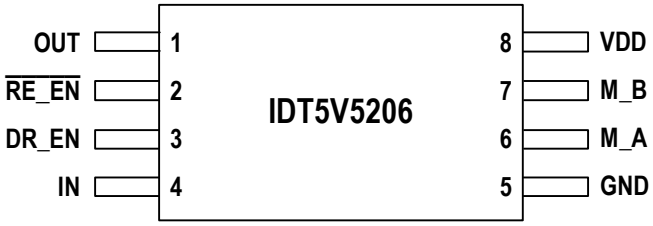


Figure-2 IDT5V5206 SOIC8 Package Pin Assignment

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Pin No.	I/O	Type	Description
Global Signal				
DR_EN	3	I Pull-down	LVTTL	**DR_EN: M-LVDS Driver Enable** This pin controls the M-LVDS driver: high for enable and low for disable.
$\overline{\text{RE\_EN}}$	2	I Pull-up	LVTTL	**$\overline{\text{RE\_EN}}$: Type-2 M-LVDS Receiver and LVTTL Driver Enable** This pin controls the Type-2 M-LVDS receiver and LVTTL driver: high for disable and low for enable. Note that the LVTTL driver is in high impedance state when disabled.
LVTTL Interface				
IN	4	I	LVTTL	**IN: LVTTL Input** An up to 166 MHz LVTTL signal is input on this pin.
OUT	1	O	LVTTL	**OUT: LVTTL Output** This pin outputs an up to 166 MHz signal.
M-LVDS Interface				
M_A M_B	6 7	I/O	M-LVDS	**M_A/M_B: Positive/Negative M-LVDS Data Bus Interface** This pair of pins are connected to the M-LVDS data bus.
Power Supply and Ground				
VDD	8	Power	-	**3.3 V Power Supply**
GND	5	Ground	-	**Ground**

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATING AND RECOMMENDED OPERATION CONDITIONS

Table-2 Absolute Maximum Rating

Symbol	Parameter		Range
V_{DD}	Supply Voltage		-0.5 V to 4.1 V
V_{IN}	Input Voltage	$\overline{RE\_EN}$, DR_EN, IN_A, IN_B	-0.5 V to 4.1 V
		M_A, M_B	-1.8 V to 4 V
V_{OUT}	Output Voltage	OUT_A, OUT_B	-0.3 V to 4 V
		M_A, M_B	-1.8 V to 4 V
	Electrostatic Discharge	Human Body Model M_A, M_B	±8 kV
		All pins	±2 kV
T_J	Junction Temperature	150°C	
T_S	Storage Temperature	-65°C to 165°C	

Table-3 Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power Supply	3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	2		3.0	V
V_{IL}	Low Level Input Voltage	0		0.8	V
	Voltage at any Bus Terminal	-1.4		3.8	V
	Magnitude of Differential Input Voltage	0.05		3.0	V
T_A	Ambient Operating Temperature	-40		85	°C

3.2 LVTTL DRIVER/RECEIVER CHARACTERISTICS

3.2.1 M-LVDS TO LVTTL

Table-4 LVTTL DC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IHL}	Input High Level		2.0		V_{DD} + 0.3	V
V_{ILL}	Input Low Level		-0.3		0.8	V
I_{ILL}	Input Leakage Current		-1.0		1.0	µA
V_{OHL}	Output High Voltage	Output Current = 17 mA, V_{DD} = 3 V	2.4			V
V_{OLL}	Output Low Voltage	Output Current = 12 mA, V_{DD} = 3 V			0.4	V

Table-5 LVTTL AC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_r	Rise Time	C_{load} = 15 pF, 10% - 90%			1.2	ns
t_f	Fall Time	C_{load} = 15 pF, 10% - 90%			1.2	ns
f_{ML}	Frequency				166	MHz

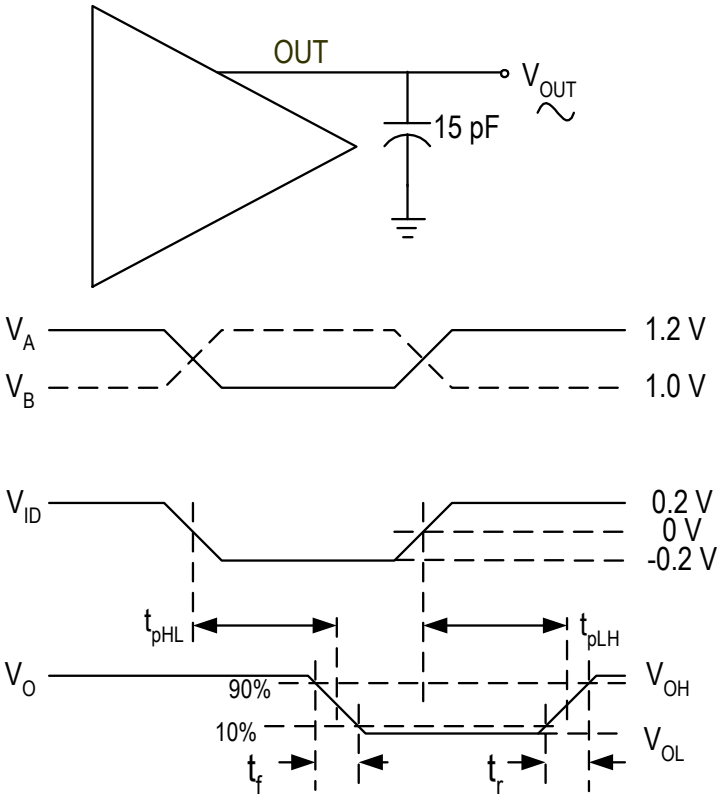


Figure-3 LVTTL Output Test Circuit and Waveforms

3.3 M-LVDS DRIVER TYPE-2 RECEIVER CHARACTERISTICS

Table-6 M-LVDS Type-2 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-mode Input Voltage	Receiver Output[1]
V_A	V_B			
2.400	0.000	2.400	1.200	High
0.000	2.400	-2.400	1.200	Low
3.475	3.325	0.150	3.4	High
3.425	3.375	0.050	3.4	Low
-0.925	-1.075	0.150	-1	High
-0.975	-1.025	0.050	-1	Low

1. The receiver is enabled (The $\overline{RE\_EN}$ pin is pulled low).

Table-7 M-LVDS DC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{ODM}	Differential Output Voltage		480		650	mV
ΔV_{ODM}	Change in V_{ODM} for Complimentary Output States, $\Delta V_{ODM} = \lvert V_{ODM1} - V_{ODM0} \rvert$		-50		50	mV
V_{OSM}	Offset Voltage		0.8		1.2	V
ΔV_{OSM}	Change in V_{OSM} for Complimentary Output States		-50		50	mV
$V_{OSM(p-p)}$	Peak-to-peak Common-mode Output Voltage				150	mV
I_{OM}	Output Short Circuit Current				20	mA
I_{IZM}	High Impedance Input Current		-10		10	µA
V_{THM}	Differential Input High Threshold	Type-2	150			mV
V_{TLM}	Differential Input Low Threshold	Type-2			+50	mV
V_{CMM}	Input Common-mode Range	$V_{INA} - V_{INB}$ = 200 mV	-1		3.4	V
I_{INM}	Input Current	Input Voltage = 0 V to 2.4 V	-20		20	µA

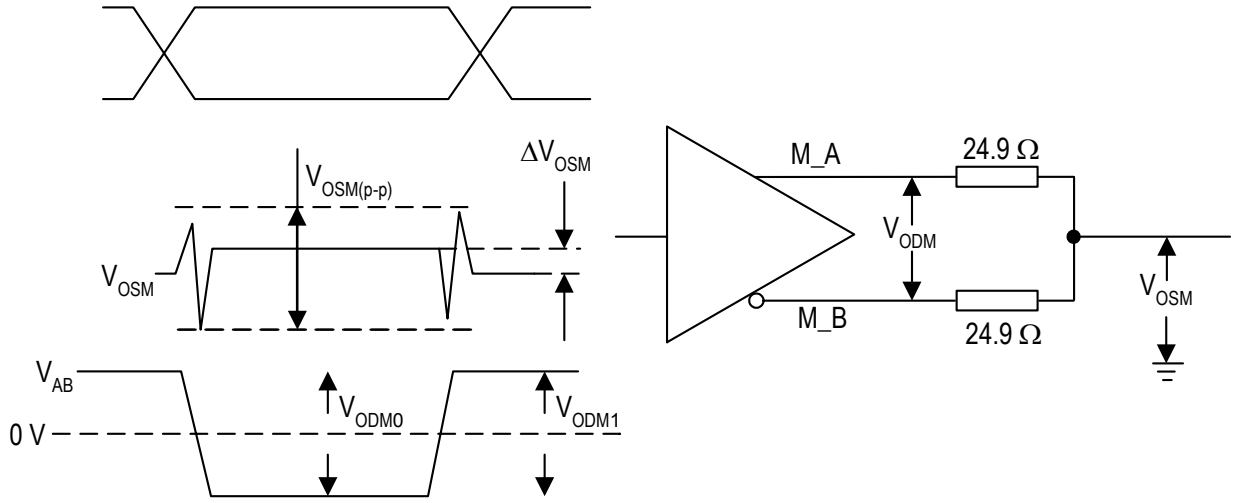


Figure-4 M-LVDS Driver Output Voltage Test Circuit

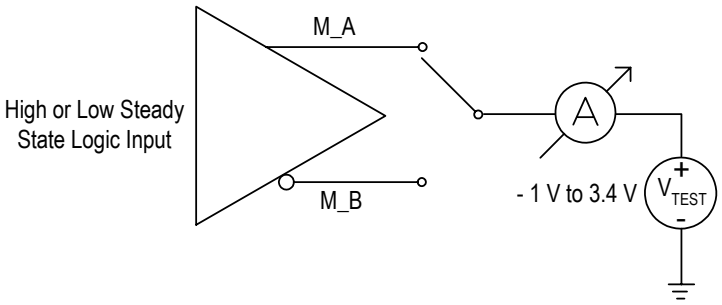


Figure-5 M-LVDS Driver Short-Circuit Test Circuit

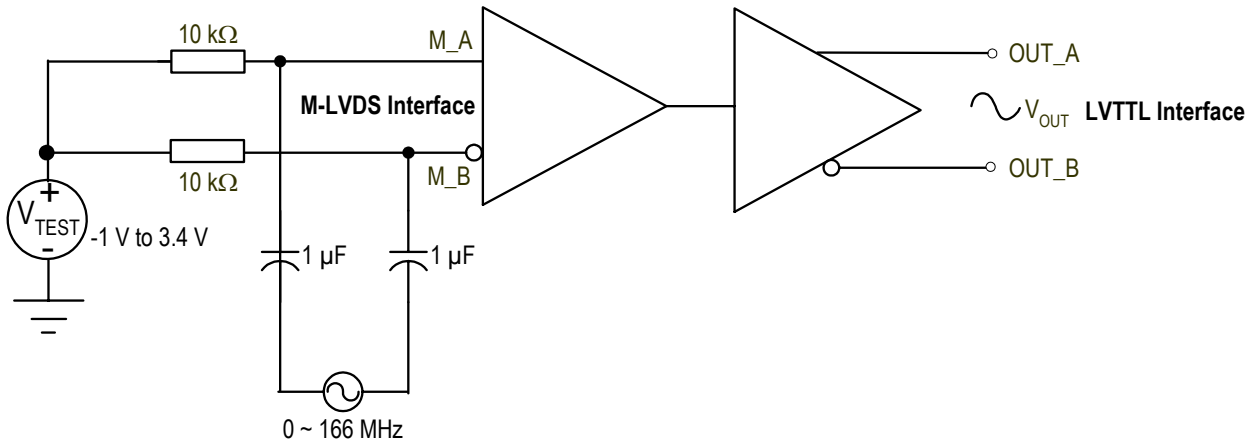


Figure-6 M-LVDS Type-2 Receiver Input Common-mode Range Test Circuit

Table-8 M-LVDS Input Current Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_A	Receiver or Transceiver with Driver Disabled Input Current	V_A = 3.8 V, V_B = 1.2 V	0		32	µA
		V_A = 0 V or 2.4 V, V_B = 1.2 V	-20		20	
		V_A = - 1.4 V, V_B = 1.2 V	-32		0	
I_B	Receiver or Transceiver with Driver Disabled Input Current	V_B = 3.8 V, V_A = 1.2 V	0		32	µA
		V_B = 0 V or 2.4 V, V_A = 1.2 V	-20		20	
		V_B = -1.4 V, V_A = 1.2 V	-32		0	
I_{AB}	Receiver or Transceiver with Driver Differential Current (I_A - I_B)	V_A = V_B, -1.4 V < V_A < 3.8 V	-4		4	µA
$I_{A(OFF)}$	Receiver or Transceiver Power-off Input Current	V_A = 3.8 V, V_B = 1.2 V, 0 V < V_{DD} < 1.5 V	0		32	µA
		V_A = 0 or 2.4 V, V_B = 1.2 V, 0 V < V_{DD} < 1.5 V	-20		20	
		V_A = -1.4 V, V_B = 1.2 V, 0 V < V_{DD} < 1.5 V	-32		0	
$I_{B(OFF)}$	Receiver or Transceiver Power-off Input Current	V_B = 3.8 V, V_A = 1.2 V, 0 V < V_{DD} < 1.5 V	0		32	µA
		V_B = 0 or 2.4 V, V_A = 1.2 V, 0 V < V_{DD} < 1.5 V	-20		20	
		V_B = -1.4 V, V_A = 1.2 V, 0 V < V_{DD} < 1.5 V	-32		0	
$I_{AB(OFF)}$	Receiver or Transceiver Power-off Differential Input Current (I_A - I_B)	V_A = V_B, 0 V < V_{DD}< 1.5 V, -1.4 V < V_A < 3.8 V	-4		4	µA
C_{AB}	Transceiver with driver disabled differential input capacitance	V_{AB} = 0.4 sin (30E6πt) V			4	pF

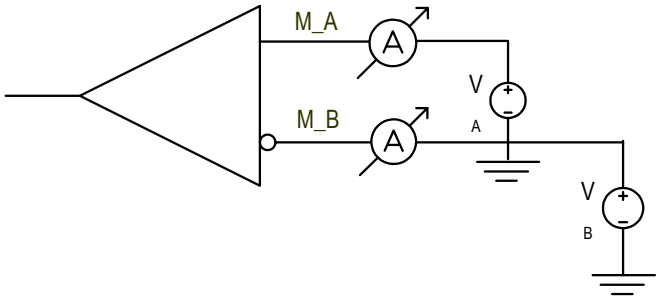


Figure-7 Various Input Currents Test Circuit

Table-9 M-LVDS AC Parameters

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
t_r	Rise Time	10% - 90%	0.8		1.5	ns
t_f	Fall Time	10% - 90%	0.8		1.5	ns
t_{TSL}	Differential Skew, $t_{TSL} = \{t_{TSL1}, t_{TSL2}\}$		-100		100	ps
f_{ML}	Frequency				166	MHz

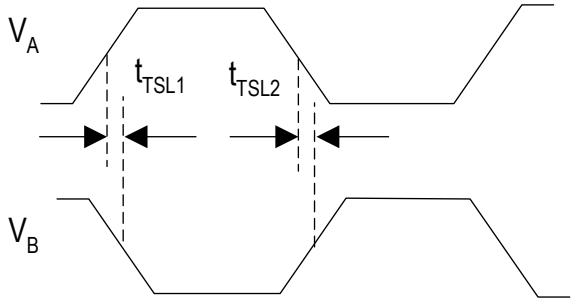


Figure-8 Differential Skew

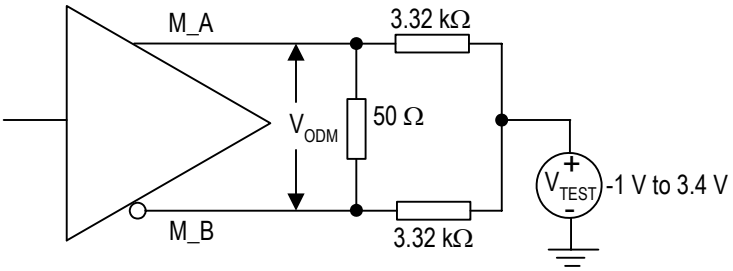


Figure-9 M-LVDS Output Voltage Test Circuit

Table-10 M-LVDS Type-2 Receiver AC Parameters

Output mode	Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
LVTTL	t_{pLH}	Delay, Low to High Level	Input clock: freq = 50 MHz, Impedance = 150 Ω, Voltage = -200 mV - 200 mV. See Figure-3	2.5	5.5	6.5	ns
	t_{pHL}	Delay, High to Low Level		2.5	5.5	6.5	ns
	t_{sk} Type-2	Pulse Skew, $t_{sk} = \|t_{pLH} - t_{pHL}\|$			300	500	ps
	T_r (10% - 90%)	Rise Time		1		2.4	ns
	T_f (10% - 90%)	Fall Time		1		2.4	ns
	$T_{jit(per)}$	Period jitter, rms (1 standard deviation)			4	7	ps
		Output to Output Skew				200	ps

Table-11 M-LVDS Driver AC Parameter

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
t_{pLH}	Delay, Low to High Level	Input clock: freq = 15 MHz, $T_r = T_f = 1.2$ ns, Impedance = 300 Ω, Voltage = 0 V - 3.3 V. See Figure-4	2.5	3.7	5.5	ns
t_{pHL}	Delay, High to Low Level		2.5	3.7	5.5	ns
Tsk LVTTL input	Pulse Skew, $t_{sk} = \|t_{pLH} - t_{pHL}\|$			40	100	ps
T_r (10% - 90%)	Rise Time		0.7	1.1	1.5	ns
T_f (10% - 90%)	Fall Time		0.7	1.1	1.5	ns
$T_{jit(per)}$	Period jitter, rms(1 standard deviation)			2	3	ps
	Output to Output Skew				100	ps

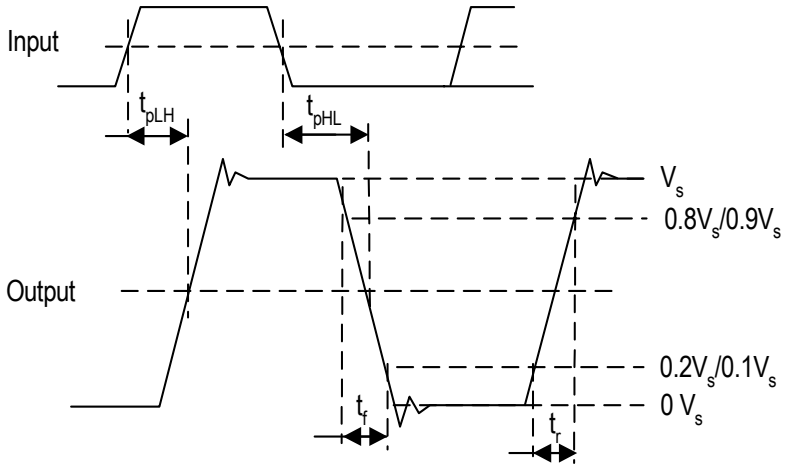
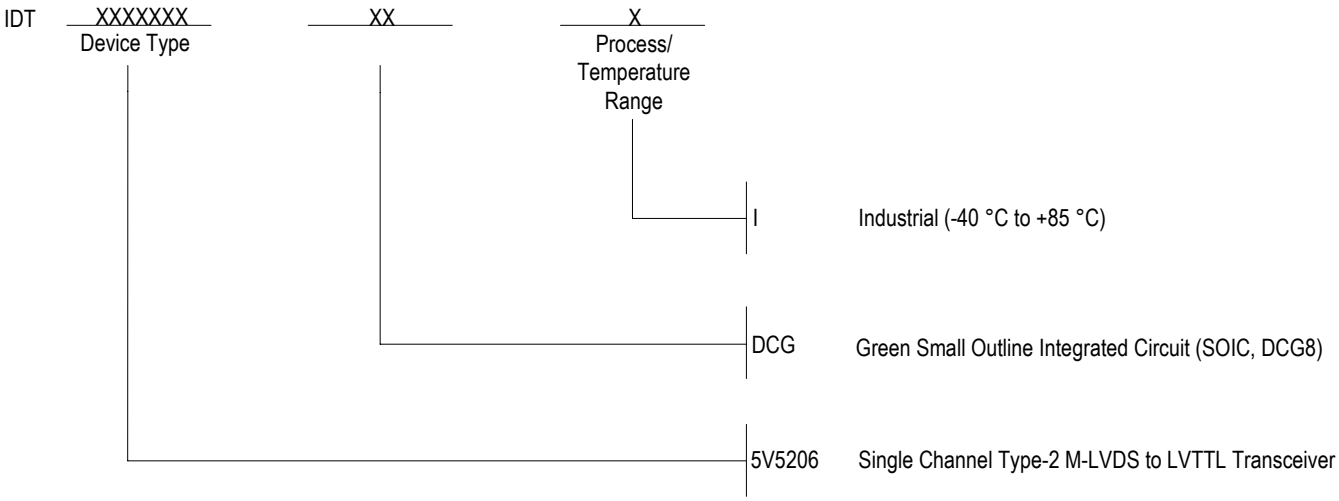


Figure-10 Timing and Voltage Definitions for the Output Signal

ORDERING INFORMATION



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