FAQs ABOUT THE IDT82V3001A, IDT82V3002A, IDT82V3011, AND IDT82V3012

APPLICATION NOTE AN-406

INTRODUCTION:

Digital Phase Lock Loops, DPLLs, often referred to as a WAN PLL, can be difficult to understand as they incorporate traditional PLLs as well as complex logic. This application note is designed to set in place some basic terminology, demystify WAN PLL and clarify commonly asked questions about the functionality of WAN PLL.

In basic terms, the WAN PLL contains an internal Analog Phase Lock Loop (APLL), digital logic and internal memory to track the external input clock relative to the internal APLL. From the WAN PLL's perspective, the internal APLL is considered the "ideal" clock source. The internal APLL is a very narrow band PLL so that can produce a very precise internal clock with which to characterize the external clock. To do this, the APLL requires and external clock oscillator (20MHz).

TERMINOLOGY:

Before getting into the details of the WAN PLL, here are some definitions of terms that often come up when discussing WAN PLLs.

JITTER:

SONET specifications ITU-T-G.701 "Jitter is defined as that short-term non-cumulative variations of the significant instants of a digital signal from their ideal positions in time".

WANDER:

ITU defines wander as jitter<10Hz or long term variations in the significant instants. Other definitions of wander do exist, though this is the most widely accepted definition.

UNIT INTERVAL (UI):

Jitter Amplitude is measured in Unit Intervals (UI), where 1 UI would be the phase deviation of one clock period.

UIPP (UNIT INTERVAL PEAK-TO-PEAK):

Peak-to-peak UI is often referred to as jitter amplitude. Since jitter amplitude is normalized to the associated frequency (a percentage), it is easy to compare jitter amplitude among different frequencies.

Example:

Maximum Intrinsic Jitter of F8o (8KHz) is 0.0001UIpp (per Data Sheet)
8KHz = 125µS for 1 UI
0.0001UIpp x 125µS = 12.5ns
This means that the maximum amount of intrinsic jitter you would expect to see on the F8o pin is 12.5ns peak-to-peak.

PARTS PER MILLION (PPM):

Example:

The 20MHz clock oscillator has a frequency accuracy of +/-32ppm.
20MHz = 50ns for 1 UI
50ns x (32/1,000,000) = 1.6pSec
This means that the 20MHz clock oscillator will nominal 50ns clock cycle +/-1.6pSec

Alternatively:

20MHz x (32/1,000,000) = 640Hz
This means that the 20MHz clock oscillator will nominally be 20MHz +/-640Hz.

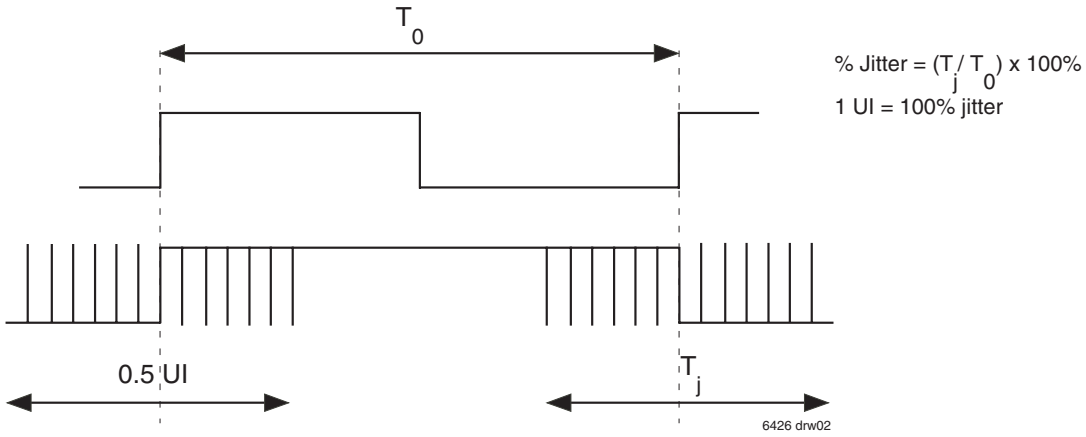

Figure 1. The Unit Interval (UI)

CYCLE-TO-CYCLE JITTER:

Is a comparison of periods between adjacent clock cycles. "This measurement shows the instantaneous dynamics that a down-stream clock-recovery PLL will encounter." Maximum cycle-to-cycle phase shift on the clock outputs in holdover is 0.78ns. Maximum cycle-to-cycle phase shift on the frame pulse outputs in holdover is 5ns (5 nS/125µS).

PERIOD JITTER:

Is not really a jitter measurement. It is really a measurement of the period of each clock cycle. Maximum cycle-to-cycle jitter is most often calculated using period information. The peak-to-peak jitter (Max period-Min period) is the cycle-to-cycle jitter MAX.

TIE (TIME INTERVAL ERROR):

Measures how far each active edge of the clock varies from it's ideal position, where the ideal position is determined by a reference or recovered clock. On the DPLL, the ideal clock is the internal APLL. TIE is used to show the cumulative effect that period jitter has over time. TIE is calculated by subtracting the nominal (or ideal internal) clock period from the measured period for a duration of time and then integrating over that time. The WAN PLL stores this TIE data so that if there is a loss of clock, the WAN PLL can continue to produce output clocks which look like the old input reference. The output characteristics will be based on the TIE data stored in the WAN PLL.

PERIODIC JITTER (PJ)/SINUSOIDAL JITTER:

"Repeats in a cyclic fashion. Since a periodic waveform can be decomposed into a Fourier series of harmonically related sinusoids, this kind of jitter is called sinusoidal jitter. PJ is typically caused by external deterministic noise sources such as switching power-supply noise or a strong RF carrier. It may also be caused by an unstable clock recovery PLL."

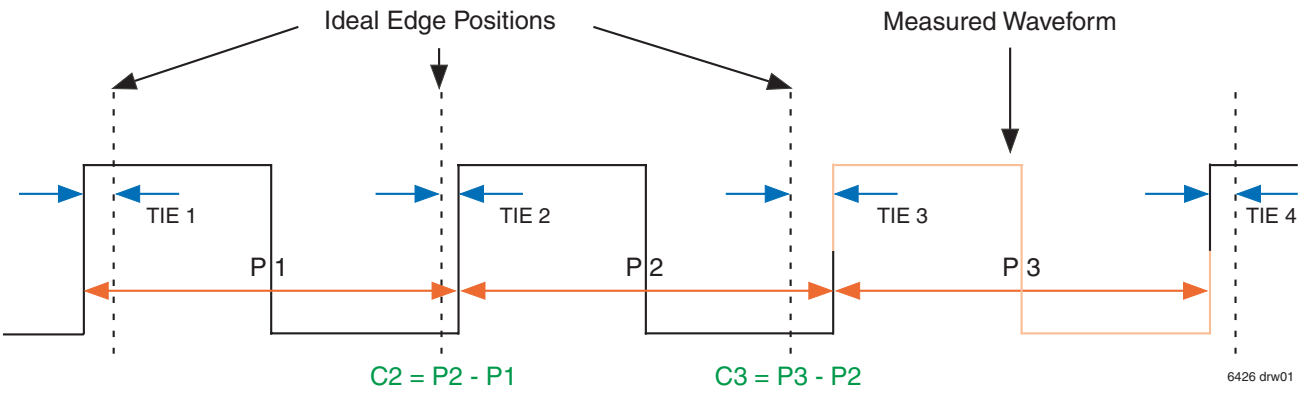

Figure 2. Period Jitter vs. Cycle-Cycle Jitter vs. Time Interval Error (TIE)

INDICATORS OF INPUT CLOCK REFERENCE QUALITIES:

The WAN PLL accepts an input clock with which a system will be synchronized—Fref. The WAN PLL has three different output indications that describe the quality of that input clock—Lock, Mon_Out, and Normal/Holdover. These indications can be used by the system designer to meet the clocking requirements of the system.

LOCK:

The "Lock" indication means that the average input frequency is equal to the average output frequency +/-0.4ppm over a 2 second interval.

```
if (timer == 2 seconds & Mode == Normal Mode){
    if (|average Input ref freq- average output clock freq | <0.4 ppm){
                Lock=H;
    } else {
                Lock=L;
    }
}
```

It should be noted that Lock is really only a useful indication in the Normal mode. When the WAN PLL goes into Holdover mode, the internal APLL is used; this APLL will always be locked—unless the 20MHz clock oscillator is pulled!

Lock Output Pin:

Input ref < +/-0.4ppm, Lock=L
Input ref > +/-0.4ppm, Lock=H
Freq * (0.4/1,000,000)
8KHz +/-0.0032Hz — 7999.9968Hz-8000.0032Hz
1.544MHz +/-0.6176Hz — 1543.999382KHz-1544.0006184KHz
2.048MHz +/-0.8192Hz — 2047.999181KHz-2048.00081KHz

MONITOR OUTPUT:

The monitor output pin is used most often as the indicator to perform a reference switch. According to the Telcordia GR-1244-CORE standard, the WAN PLL should be able to reject references that are off the nominal frequency by more than ± 12ppm. The IDT82V3002A monitors TIE Control Block input frequency and outputs a MON_out signal to indicate the monitoring result. Whenever the reference frequency is off the nominal frequency by more than ± 12ppm, the MON_out pin goes high. The MON_out signal is updated every 2 seconds. The MON_out pin will give an indication of the quality of the Fref independent of the mode of the WAN PLL. In other words, if the WAN PLL goes into Auto-holdover, the system can apply a new Fref and the MON_output will give an indication of the quality of the input. Of course, if the input is good, the WAN PLL will go back to the normal mode.

MON_out output pin (any mode)
Input ref < +/-12ppm, MON_out=L
Input ref >=+/-12ppm,MON_out=H
Freq*(12/1,000,000)
8Kz+/-0.096Hz — 7999.904Hz-8000.096Hz
1.544MHz+/- 18.528Hz — 1543.981472KHz - 1544.018528KHz
2.048MHz+/- 24.576Hz — 2047.975424KHz - 2048.024576KHz

NORMAL/AUTO-HOLDOVER INDICATIONS:

Although there are no specific specifications for which the Normal pin and Holdover pin are designed, these pins do give indications as to what mode the WAN PLL is actually in. Remember, the Model1-0 pins put the WAN PLL into a specific mode—Normal mode for instance. However, if the quality of the input is bad, the WAN PLL can actually be in Auto-holdover mode. In short:

Mode	Freerun Pin	Normal Pin	Holdover Pin
Freerun	H	L	L
Normal	L	H	L
Holdover	L	L	H
Auto-Holdover	L	L	H

Input ref < +/-18Kppm, Normal
Input ref > +/-18Kppm, Auto-holdover
Freq * (18,000/1,000,000)
8KHz +/-144Hz — 7856Hz - 8144Hz
19.44MHz +/- 349.920KHz — 19090080Hz - 19789920Hz
Input ref < +/- 36Kppm, Normal
Input ref > +/- 36Kppm, Auto-holdover
1.544MHz +/- 55.584KHz — 1488.416KHz - 15992584KHz
2.048MHz +/- 73.728KHz — 1974.275KHz - 2121.728KHz

CAPTURE RANGE:

The capture range of the Fref inputs of the WAN PLL is 230ppm. This means that in order for the WAN PLL to bring in or start to track the Fref, the Fref cannot exceed 230ppm. Once the WAN PLL has locked on input Fref, the input can fall outside of the capture range and it is possible that the WAN PLL can continue to track and lock on the Fref. As the input crosses the thresholds of the indicators discussed above, the output indicator states will change. In short, it is possible for the WAN PLL to track (be locked on) the Fref inputs even though the Mon_outpin is high.

TIME INTERVAL ERROR (TIE):

The WAN PLL incorporates a TIE block which allows a new or secondary input to drive the outputs where the inputs is phase shifted. In essence, the outputs are following the inputs but the inputs is phase shifted. Max TIE need only be based on half a clock period. If the phase difference between the input, Fref, and the corresponding output is greater then half the clock cycle a TCLR will force the outputs to phase shift in direction A. If however, the phase difference between the input, Fref, and the corresponding output is less than half the clock cycle, a TCLR will force the outputs to phase shift in the directions B—opposite direction A. In other words, a TCLR will force the outputs through the phase slope limiter to the nearest corresponding edge. Since the maximum phase shift is half the UI, the TIE storage circuits will only store half a UI. See Figure 3 (Phase Shift Left) and Figure 4 (Phase Shift Right)

a) 8K, TIE Max = 125µs/2 = 62.5µs
b) 1.544MHz, TIE Max = 648ns/2 = 324ns
c) 2.048MHz, TIE Max = 488ns/2 = 244ns
d) 19.44MHz, TIE Max = 51.4ns/2 = 25.7ns

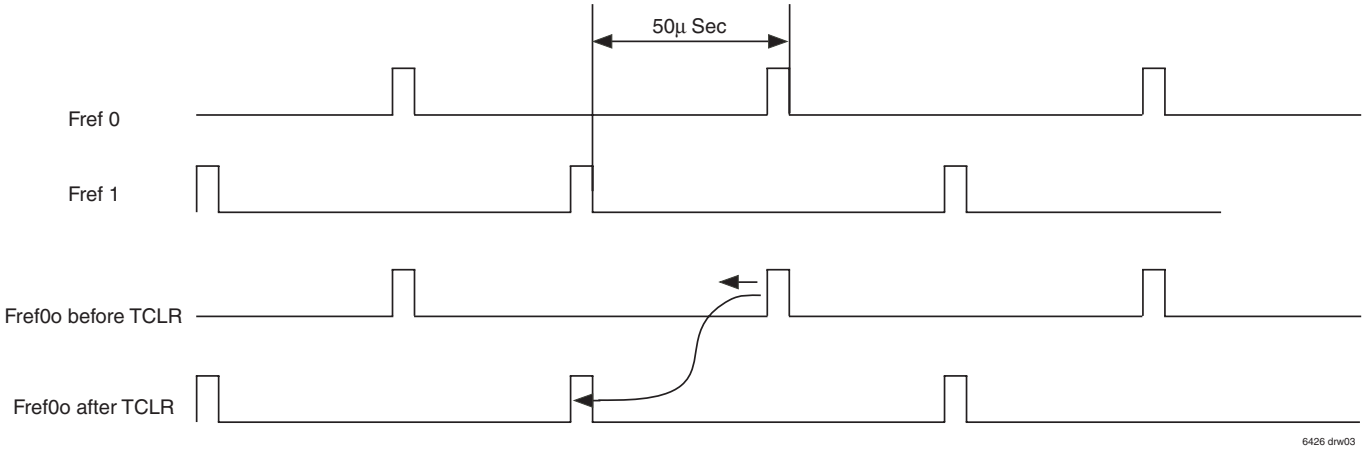

Figure 3. **WAN PLL** *Phase Shift Left*

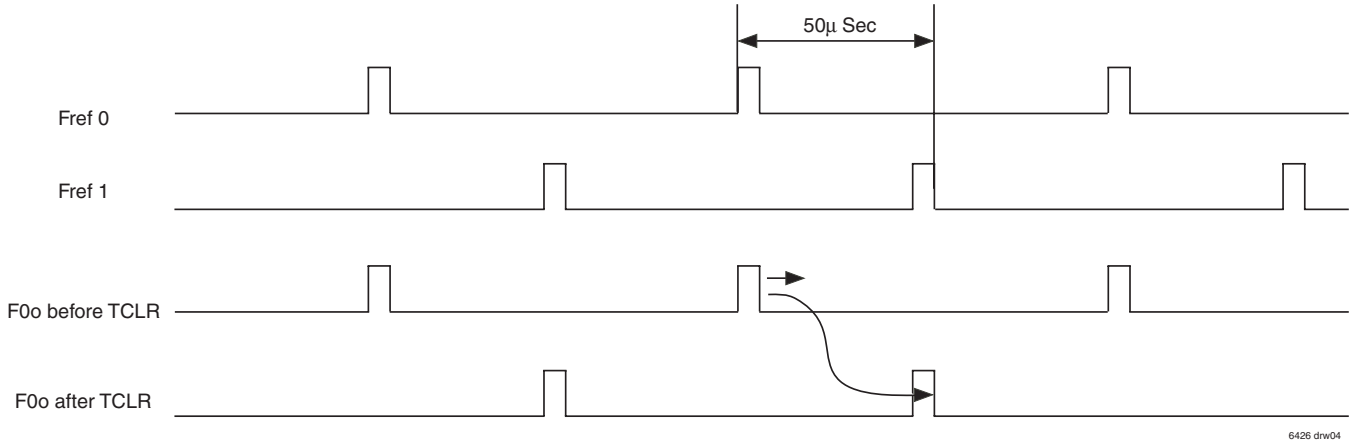

Figure 4. **WAN PLL** *Phase Shift Right*

PHASE SLOPE LIMITER (PSL):

The Phase Slope Limiter is the part of the device which limits how much the phase can shift on the outputs when a TCLR is issued. The Phase Slope Limiter in the WAN PLL is 5ns/frame (5ns/125µS) Max. The PSL is designed in such a way that when it is used in a system, which has framing devices, these outputs phase shifts will not produce any bit loss or frame loss. In the case where there is a phase difference between the input reference and the corresponding output, a TCLR will clear the TIE block, and force the outputs through the PSL over a number of frames. It should be noted that although the PSL is designated as 5ns/frame, the WAN PLL does not always induce the maximum phase shift on the output.

Example:

The phase difference between the 8KHz input Fref and F0o (8KHz) is 50µS. It will require more than 10,000 frames before the outputs are phase aligned with the input.

50µSec/ (5ns/frame) = 10,000 frames
10,000 frames / (8000 frames/sec) = 1.25 Seconds

HOLDOVER FREQUENCY ACCURACY:

Holdover frequency accuracy is a measure of how accurate the WAN PLL will maintain outputs without an input reference. For the WAN PLL, it is 0.025ppm. This means that the outputs will not deviate by more than 0.025ppm from their nominal frequency while in the Holdover mode.

FREQUENCY OFFSET:

Frequency offset can be defined as the real frequency minus the nominal frequency. Frequency offset=real frequency - nominal frequency

Recommended TCXO for stratum 3 requirements:

CMAC information:
Code:E2869
C-MAC PN: CFPT-9006 AC Frequency: 20MHz
7*5mm package
Frequency stability; 0.3 Vs Operating Temperature (0-70)
3.3V

Fordahl:
DFE S4-LH
25 x 22 x 11 mm package
20.00 MHz
+/-0.37ppm/24hours Vs -40 to 85C
+/-4.6ppm.15years
3.3V

Interquip Limited:
149-2G series
7*5mm package
Frequency stability; 0.3 Vs Operating Temperature (0-70)
3.3V

Other TCXO venders exist and different operating temperature and board conditions may require different specifications for the TCXO. This is included in the document for reference purposes only.

SCENARIOS:

1) The basic and permanent reference switch using TCLR. TIE is enable.

a) Ref 1 is good
b) Ref 2 is good
c) Ref 1 has a LOS
d) WAN PLL goes into Auto-holdover. Output phase continuity is maintained.
e) SW switches to Ref 2 which has a different phase alignment than Ref 1.
f) WAN PLL maintains outputs now offset from the input.
g) SW issues TCLR to WAN PLL
h) Outputs phase shift over time until the outputs are phase aligned with the Ref 2.

Comments:

This is the recommended use of the WAN PLL.

2) The basic reference switch no TCLR. TIE is enabled.

a) Ref 1 is good
b) Ref 2 is good
c) Ref 1 has a LOS
d) WAN PLL goes into Auto-holdover. Output phase continuity is maintained.
e) SW does not issue a TCLR to WAN PLL. The outputs will be maintained with a phase offset from the input.
f) WAN PLL maintains outputs now offset from the input
g) SW does not issue a TCLR to WAN PLL. The outputs will be maintained with a phase offset from the input.

Comments:

The WAN PLL can maintain this offset indefinitely. If the reference switch is permanent however, a TCLR is recommended.

3) The temporary reference switch. TIE is enabled.

a) Ref 1 is good
b) Ref 2 is good
c) Ref 1 has a LOS
d) WAN PLL goes into Auto-holdover. Output phase continuity is maintained.
e) SW switches to Ref 2, which has a different phase alignment than Ref 1.
f) WAN PLL maintains outputs now offset from the inputs.
g) Ref 1 comes back (!LOS)
h) SW switches back to Ref 1.
i) Outputs will be maintained in the currents phase position. If Ref 1 has shifted from its previous position, the WAN PLL will maintain a phase offset with Ref 1.

Comments:

None.

4) ANALYSIS OF A PHASE SHIFT:

Conditions:

a) Reference switch from Ref 1 to Ref 2
b) Ref 2 is phase offset from Ref 1 by 50µS

Analysis:

a) First, the clock input must be 8KHz. There can only be a phase offset of 59µSec with a 8KHz clock since the cycle time of 2.048MHz is 488ns and 1.544MHz is 648ns.
b) When the reference switch occurs, the outputs will still be phase aligned to "Ref 1" but will have a 50µS phase offset.
c) If TCLR=L, the WAN PLL will slowly release phase offset and the outputs will eventually be phased aligned with Ref 2 input while still in lock status.
d) It will take > 1.25Sec for the outputs to become phase aligned with Ref 2. 50mSec/(5ns/frame)=100000frames=1.25Sec. The WAN PLL will not necessarily induce the maximum phase offset allowable per frame.

5) A CLOSER LOOK AT A REFERENCE SWITCH:

a) During a reference switch, there will be a short switch transient.
b) During a reference switch the WAN PLL will enter into Auto Holdover for a short duration.
c) During an interval the WAN PLL will measure TIE value between feedback and new reference.
d) If the input reference is not LOS (does not have a large frequency offset) then the WAN PLL will enter back in to normal mode.

FAST LOCK DEMYSTIFIED:

1) The GR-1244-CORE Standard:

a) Normal Mode — In the normal mode, the clock is synchronized to a reference. The output frequency of the clock is traceable to the input reference frequency over the long term, and the phase difference between the input and output is bounded. It is intended that all clocks other than stratum 1 clocks operate in this mode except under the failure condition of loss of all references.

b) Fast-start mode (Fast LOCK) — This optional fast-tracking mode may be used for fast pull-in of the clock to a reference (e.g., when recovering from holdover or when the input reference has an abrupt change in frequency). After the clock achieves lock, the clock automatically changes to the slower-tracking normal mode.

2) The devices and the Modes:

a) Normal Mode:

The WAN PLL can automatically achieve the GR-1244 normal and fast lock. As a result it is not even necessary to use the fast lock mode.

b) Fast Lock Mode:

IDT3002A/3001A/3012/3011 is designed for testing purposes or special applications where there may be a large frequency offset (200ppm). In the testing case, perhaps frequent and repeated system starts are required to debug another portion of the system. To minimize the start-up time the WAN PLL may be put in to Fast Lock Mode. Again, however, fast start is used at power-up, reset, or start-up and not during normal operation.

3) The Objective:

It is well understood that there is a strong desire to reduce lock time when switching from auto-holdover to normal mode. Fast lock however is not going to produce that result or any useful results during normal operation. If Ref 2 to the WAN PLL is good, the WAN PLL will lock quickly because the frequency difference will not exceed 4.6 ppm between the input clock and holdover output. In short trying Lock to FLOCK will not provide any improvement as far as lock time is concerned.

The secondary case, and most common case, is using the Normal pin as an indication to do a reference switch. As the Normal indication accepts a wider range of input frequency, it will take longer for the DPLL to indicate the input is good and there should be little to no penalty hits.

4) Negative Consequences of Tying FLOCK to LOCK:

If there is excessive wander or jitter, the LOCK pin will be if the LOCK pin is toggling then the FLOCK will be toggling—from a system perspective this is undesirable.

5) When in Fastlock Mode, the phase slope limiter is disabled and this can have adverse effect on the outputs—this is usually not desired during normal operating mode since you do not want to induce any frame slips on a system.

6) If lock was achieved, then lost, and finally regained, usually the WAN PLL will not take a long time to relock. According to the GR-1244 requirement, if there is a frequency difference (e.g. 4.6 ppm) between your input clock and the WAN PLL holdover output, the lock time is significantly faster when going back to normal mode.

7) If FLOCK is tied to LOCK you may get faster lock, but this is at the expense of potentially causing excessive slip on the output. This is not considered acceptable in most designs.

8) The WAN PLL can be used as a way to tell if a reference input is "good" but should not be done using the Lock pin. If the Lock pin is used, some kind of integration algorithm must be performed by the system. Lock will have to be sampled multiple times over some time interval to see if it is truly good. This should be done because if there is excessive jitter, the WAN PLL may fall in and out of lock. In other words, if Lock is sampled once, then that sample would be just that—one sample of the quality of the input. If the input is "bad", it may actually be okay at the sample point but not really good. In other words you'll get a false positive on the sample point. That being said, there will be cases in some systems, where a signal is either good or bad, and not somewhere in between. Given these factors FLOCK should not be tied to LOCK. The Mon_outpin is the best indicator of the quality of Fref inputs since it will indicate if the inputt exceeds the GR-1244 limits on jitter or frequency.

REFERENCES

Tektronix Application Notes:
"Understanding and Performing Precise Jitter Analysis"
"Analyzing Clock Jitter Using Excel"
"Performing Jitter Measurements with the TDS 700D/500D Digital Phosphor Oscilloscopes"
"Sampling Oscilloscope Techniques" Technique Primer 47W-7209
"The Most Comprehensive, Convenient and Cost-Effective Answer to Resolving Jitter Issues in Your Designs"
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