PHASE-LOCKED LOOP CLOCK GENERATORS

APPLICATION NOTE AN-155

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INTRODUCTION

Phase-locked loops(PLLs) are used extensively in the areas of analog system design and communication systems. With the increasingly stringent timing constraints in high performance systems today, phase-locked loops are being introduced in more general digital designs as well. The computer motherboard is one example of such a mainstream application.

The key advantages that PLLs bring to clock distribution applications are phase/delay compensation, frequency multiplication and duty-cycle correction. This application note introduces users to PLL operation and gives guidelines on their use and application.

IDT makes several PLL-based clock drivers :

- FCT88915TT - 8 outputs with external loop filter capacitor, 3-state outputs and TTL output voltage swings
- FCT388915T - 3.3V version of the 88915TT
- FCT3932 - 3.3V programmable PLL with 18 outputs

Most of the discussion below is geared towards IDT's PLL-based clock chips. The reader is advised to refer to individual datasheets for specific device characteristics.

TABLE OF CONTENTS

PHASE-LOCKED LOOP OPERATION

A phase-locked loop is a closed loop system with negative feedback. As the name implies, the output signal "locks" onto an incoming reference signal. Figure 1 is a simplified block diagram showing the main components of a phase-locked loop.

A PLL typically consists of 4 main components - the phase-frequency detector(PFD), the charge pump, the loop filter and the voltage-controlled oscillator(VCO). The phase-frequency detector(PFD) compares feedback and reference signals and generates an error signal which is proportional to the magnitude of the phase/frequency difference between them. This error signal is fed to the charge pump. The charge pump current controls the magnitude of charge stored in the loop filter thus converting the PFD output to a control voltage input recognizable by the voltage controlled oscillator(VCO). The VCO generates an output frequency proportional to this control voltage. The output frequency may be further divided down before being fed back to the PFD, as shown in Figure 1.

When the PLL is "locked", there is a constant phase difference (usually zero) between the feedback and reference signals and their frequencies are matched.

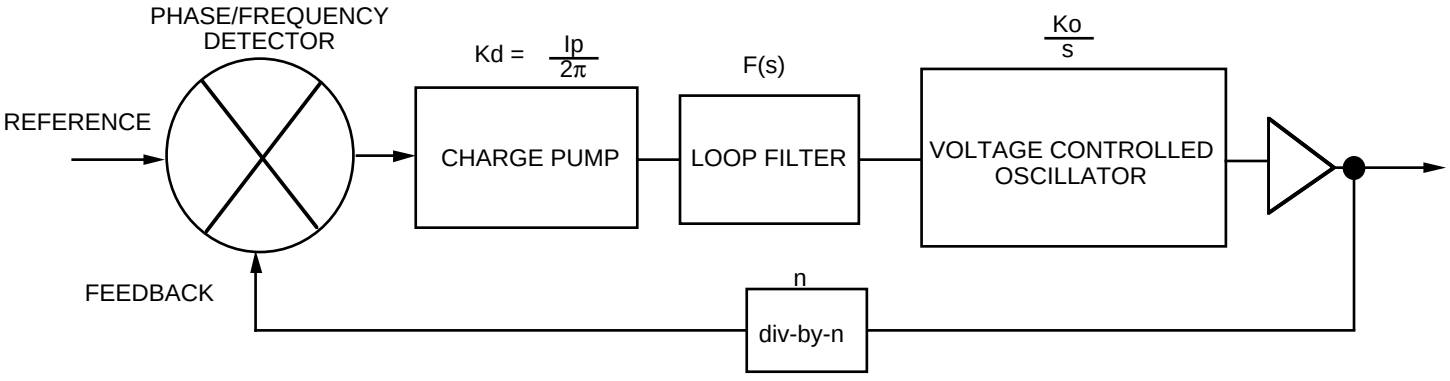


Figure 1. Phase-Lock Loop

PHASE-FREQUENCY DETECTOR

The function of the Phase and Frequency Detector is to generate an output signal proportional to the phase/frequency difference between the reference and feedback signals. Figure 2 shows an example of a PFD implementation. Here the output signal takes the form of UP or DOWN pulses which in turn activate the charge pump switch.

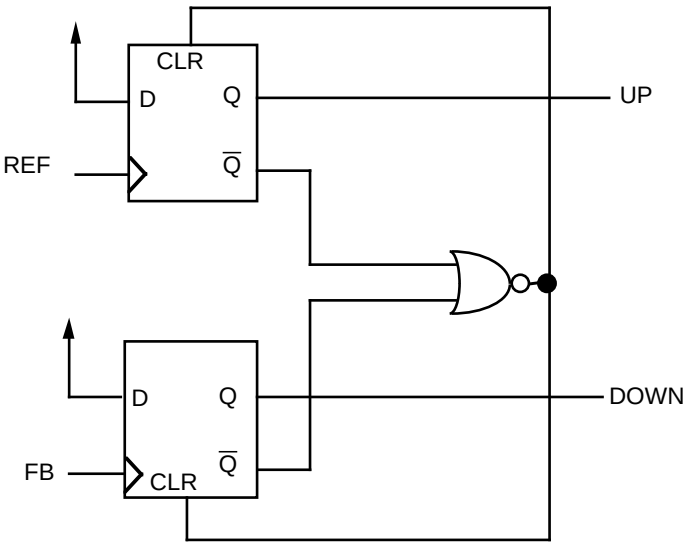


Figure 2. Phase Frequency Detector

The UP signal is asserted on every REF clock rising edge and cleared when both UP and DOWN are high. The DOWN signal is asserted on every FB clock rising edge and also cleared when both UP & DOWN are high. If the feedback is found to lag the reference signal, the output frequency is increased. When the feedback leads the reference signal, the output frequency is decreased. Thus any adjustment of output phase or frequency is made by adjusting the VCO frequency. Phase error may cause the frequency to overshoot and/or undershoot around the input frequency until a steady-state operating point is reached, where both phase and frequency are matched.

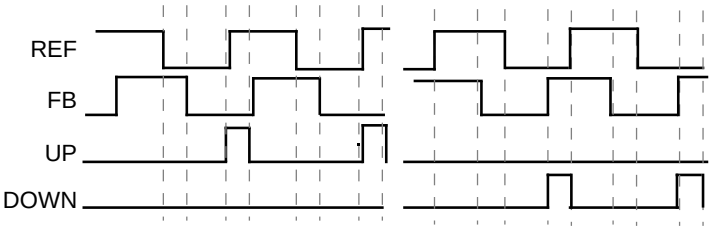
$$tP = | \theta e / \omega i |$$

where

tP = Duration of UP or DOWN pulse

θe = Phase error between REF and FB signals

ωi = Frequency of REF signal



(a) REF leads FB (b) FB leads REF

Figure 3. PFD operation

Frequency detection capability shortens LOCK time. Combinatorial PDs do not have frequency detection capability. This phase-only detect is required in datacom where the reference signal is not periodic.

CHARGE PUMP

The charge pump is analogous to a 3-pole switch. It has only 3 allowable states : UP, DOWN and OFF. When the FB leads REF, the VCO has to slow down, therefore DOWN is activated and current I_{DOWN} flows in one direction. When it lags, the VCO has to speed up hence UP is activated and current I_{UP} flows in the other direction. When the PLL is locked, PFD output is in 3-state condition and no current flows.

The purpose of this circuit is to deliver a constant pump current, Ip, to the loop filter. The duration of the switch ON time controls the amount of charge stored in the loop filter, and consequently the VCO control voltage. The combined transfer function or gain of the PFD and charge pump is given by ,

$Kd = Ip/2\pi$

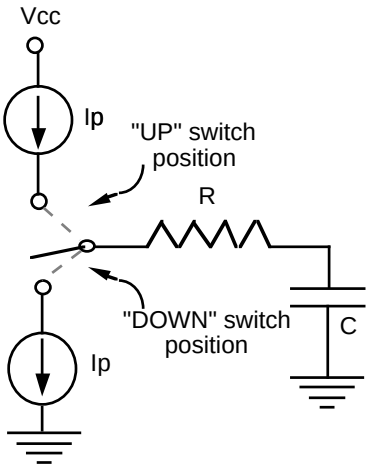


Figure 4. Charge Pump & Loop Filter configuration

LOOP FILTER

The function of the loop filter is to convert the output of the charge pump to the VCO control voltage and also to filter out any high frequency noise introduced by the PFD. An active or passive loop filter may be employed. IDT PLLs typically employ a 2nd order passive RC network for the loop filter implementation. Some PLLs, require external loop filter components while others integrate all components on the chip itself. The IDT FCT88915TT and FCT3888915T, require a single external capacitor to be connected externally and the IDT FCT3932, FCT3907 and FCT3908 use internal filters. Normal parametric variations have small effect on the PLL due to the large internal loop filter resistance typically used.

One of the simplest passive loop filter configurations consists of a single resistor and capacitor as shown in Figure 4. This constitutes a 1st order filter. A simple 1st order filter is sufficient to ensure that transient disturbances do not affect operation, but designers often use an additional high frequency pole to filter out ripple noise. The transfer function of the 1st order loop filter takes the form,

$$F(s) = [\ 1/sc\ ] / [\ R + 1/sC\ ]$$

$= 1 / [1 + sRC]$

2nd order filters are also commonly used in PLLs because of their good stability characteristics.The 2nd order loop filter transfer function takes the form,

$F(s) = [R_2 + 1/sC] / [R_1 + R_2 + 1/sC]$

$= [1 + sR_2C] / [1 + s(R_1 + R_2)C]$

A 3rd order filter may be employed but tends to increase the chances of instability.

VCO

The VCO is typically a simple multivibrator (schmitt trigger) or an n-stage current-starved inverter ring. A VCO introduces an additional pole at the origin since its output phase is an integral of frequency over time. The VCO gain or transfer function is given by

$Kv = Ko/s.$

The VCO output may be divided down to obtain the required output frequency. This ensures better clock resolution and also increases the loop gain which is desirable as will be shown later.

VCO design considerations include - linearity, operating frequency range, duty-cycle, gain and noise performance. A linear transfer function is desirable since it makes overall PLL performance more predictable. VCO linearity should accommodate process, temperature and Vcc variations.

LOOP ANALYSIS

The frequency domain is commonly used in the analysis of PLLs as a matter of convenience and simplicity. Although a PLL is generally composed of both linear and non-linear elements, the Laplace transform is widely used for determining loop stability and frequency response characteristics. Justification for this is found in [1] and [2]. Figure 1 shows a simple linear feedback system, where the open loop and closed loop transfer functions are given by,

Open Loop Transfer Function = $\theta o / \theta e = G(s).H(s)$

Closed Loop Transfer Function = $\theta o / \theta i$

$= G(s) / [1+ G(s).H(s)]$

The corresponding transfer functions for a PLL, also shown in Figure 1, are given by,

$G(s) = Kd. F(s). Ko$

$H(s) = n$

Thus,

PLL Open Loop Transfer Function = $\theta o / \theta e$

$= Kd. F(s). Ko. n$

$= n. Ko.Ip.F(s) / 2\pi s$

PLL Closed Loop Transfer Function = $\theta o / \theta i$

$= Kd. F(s). Ko / [1+ Kd. F(s). Ko. n]$

$= Ko.Ip.F(s) / [2\pi s + n. Ko.Ip.F(s)]$

Ideally, PLL output is required to follow the PLL input closely. From the above equation, this is possible if G(s) is infinite and H(s) is finite and non-zero. Infinite gain being imposible, a high loop gain is desirable. In addition, the loop is required to reject noise and also maintain stability in the range of interest. In order to reject noise, the loop should have appropriate cut-off or bandpass characteristics.

Absolute and relative stability of the loop can be determined by a number of popular graphical and analytical techniques such as the Root Locus method, Nyquist plots, Bode plots and the Routh-Hurwitz criterion.

Root-Locus

Here the locus of the roots of H(s)G(s) or the open loop transfer function is sketched with the loop gain, K, varying from zero to infinity.

For stability, all poles must lie in the left half plane. The relative positions of the poles and zeroes of H(s)G(s) determine the relative stability of the loop.

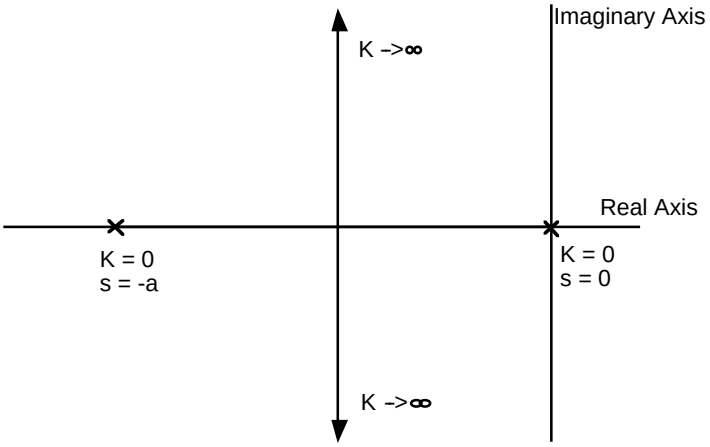


Figure 5. Example of Root-Locus plot

For example if H(s)G(s) = A / [s (s+a)], 2 poles exist at s=0 and s=-a and zeroes at plus and minus infinity. Thus the root locus moves from the poles to the zeroes as shown in Figure 5.

Nyquist plot

The Nyquist plot is a plot of the open loop transfer function G(s)H(s), with s varying from zero to infinity.

The Nyquist stability criterion states that a system is stable if the Nyquist plot encircles the (-1, j0) point as many times as the number of poles of G(s)H(s) that are in the right half of the s-plane and the encirclements, if any should be in the clockwise direction.

Bode plot

This technique involves plotting the magnitude and phase of the closed loop transfer function over frequency as shown in Figure 6. The loop is unstable if the gain magnitude is greater than zero for values of phase below $-\pi$.

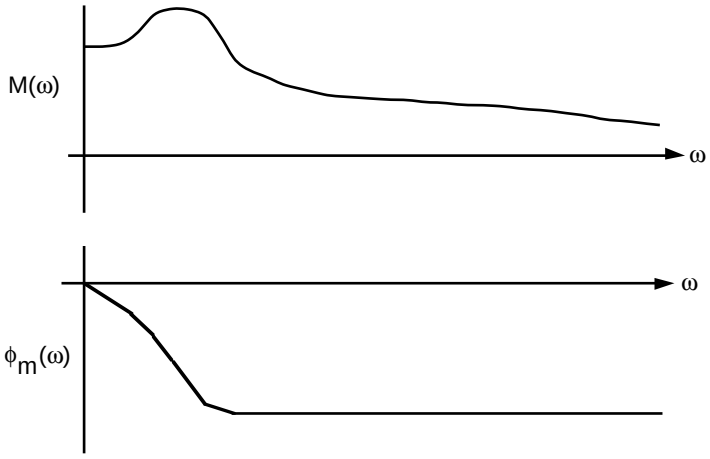


Figure 6. Example of Bode magnitude and phase plots

Routh-Hurwitz

This analytical technique uses the roots of the characteristics equation - 1 + G(s)H(s) to determine absolute stability.

ACHIEVING LOCK

If the FEEDBACK signal follows (once the phase error falls within the specified t_{PD} LOCK-in range a n-bit counter is activated) the REFERENCE signal for n consecutive cycles, the "LOCK" output is asserted. In this condition, FEEDBACK is within t_{PD} nasoseconds of REFERENCE. If the phase error wanders outside this range, the counter is reset and the "LOCK" signal is deasserted.

DELAY COMPENSATION

Typically any delay through the PLL itself is compensated out because a PLL phase shifts the output so that the phase difference between FEEDBACK and REFERENCE is no more than the t_{PD} limit. In the locked state, the PLL has a constant static phase error which is referred to as the t_{PD} or propagation delay of the PLL. In most cases this static phase error is quite small and PLLs are treated as "zero-delay" devices. The static phase error limit of the PLL is represented by the propagation delay or t_{PD} specified in datasheets.

A mismatch in the paths from the output to the receiving device input and from the output to the feedback input may also cause some phase shifting of the output signal relative to the PLL REFERENCE input. Any downstream delay in the output path can be compensated out by matching the output and feedback path delays. Figure 7 shows a few examples of such delay compensation using a PLL.

FREQUENCY MULTIPLICATION

Divisors in the feedback loop cause the REFERENCE to be multiplied up, as long as the stepped up output frequency is within the operating frequency range of the PLL. The table in Figure 8 illustrates how the value of the divisor in the feedback path affects the PLL output frequency.

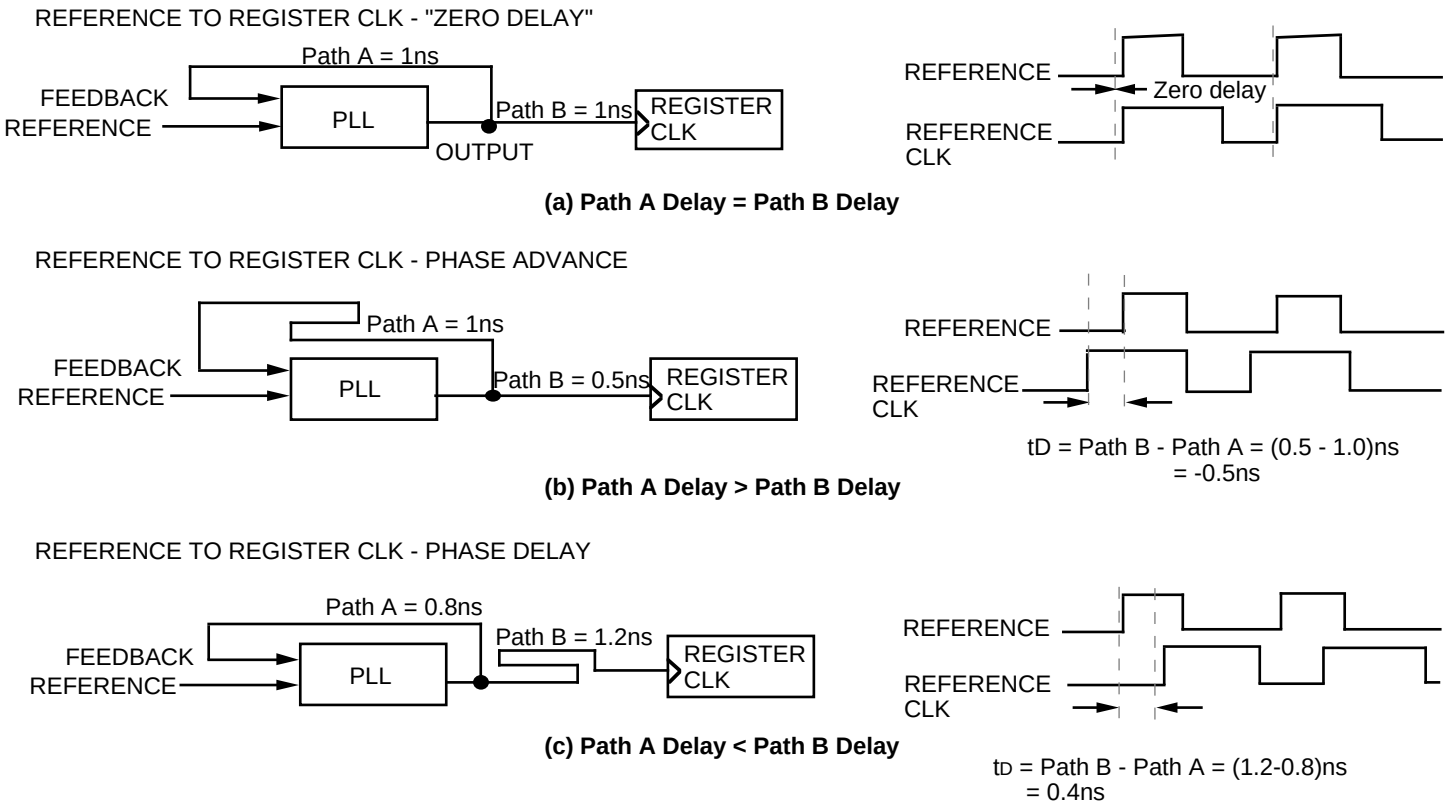
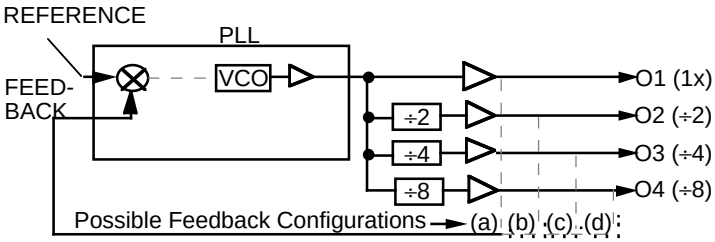


Figure 7. Delay Compensation using PLLs



The VCO output is often divided down to different outputs

MAX $f_{REF} = f_{MAX}(1/n)$

where,

1/n = Prescale factor in the feedback loop

If Reference frequency = f,

Feedback Configuration	Feedback from	Output frequency			
		O1	O2	O3	O4
(a)	O1	f	f/2	f/4	f/8
(b)	O2	2f	f	f/2	f/4
(c)	O3	4f	2f	f	f/2
(d)	O4	8f	4f	2f	f

Figure 8. Using PLLs to step up/down frequency

JITTER

Jitter is a measure of short term frequency stability. It is the deviation of the signal edge from its expected position when the PLL is locked. System noise is a key factor contributing to jitter so standard guidelines on reducing switching and power line noise should be observed to reduce output jitter.

Peak jitter parameters measure the difference between the clock period of the signal on a particular cycle and the ideal clock period. Peak or absolute jitter is sometimes referred to as phase jitter.

Cycle-to-cycle jitter refers to the difference in clock period of the signal from one cycle to the next cycle. Cycle-to-cycle jitter is also known as period jitter.

In both cases many such measurements can be taken and standard deviation and mean values can be computed. The important thing is that the sample rate be no slower than half the sampled signal frequency.

Setup and hold time failures in a system are primarily caused by differences in the clock period from one cycle to the next rather than the difference between real and ideal clock periods. Consider the synchronous pipeline in Figure 10. The cycle-to-cycle jitter could cause a hold (or setup) time violation. Except for very large magnitudes of jitter, the difference between the actual and ideal clock output does not affect system operation because no signal is referenced to or clocked on the “ideal” clock edge. For this reason, peak jitter is not as relevant a parameter in real applications as is cycle-to-cycle jitter.

Time interval analyzers or counters and spectrum analyzers are used for measuring the various jitter parameters. High resolution scopes are also able to graphically depict peak jitter. Instrumentation with a high enough sample rate, good resolution (under 100ps) and sufficient memory should be used for jitter measurements on high frequency clocks.

There are various methods of viewing or representing jitter (both peak and cycle-to-cycle) in both time and frequency domains. Some of these are histograms, stripcharts, and simple peak or standard deviation measurements with no graphical display of data.

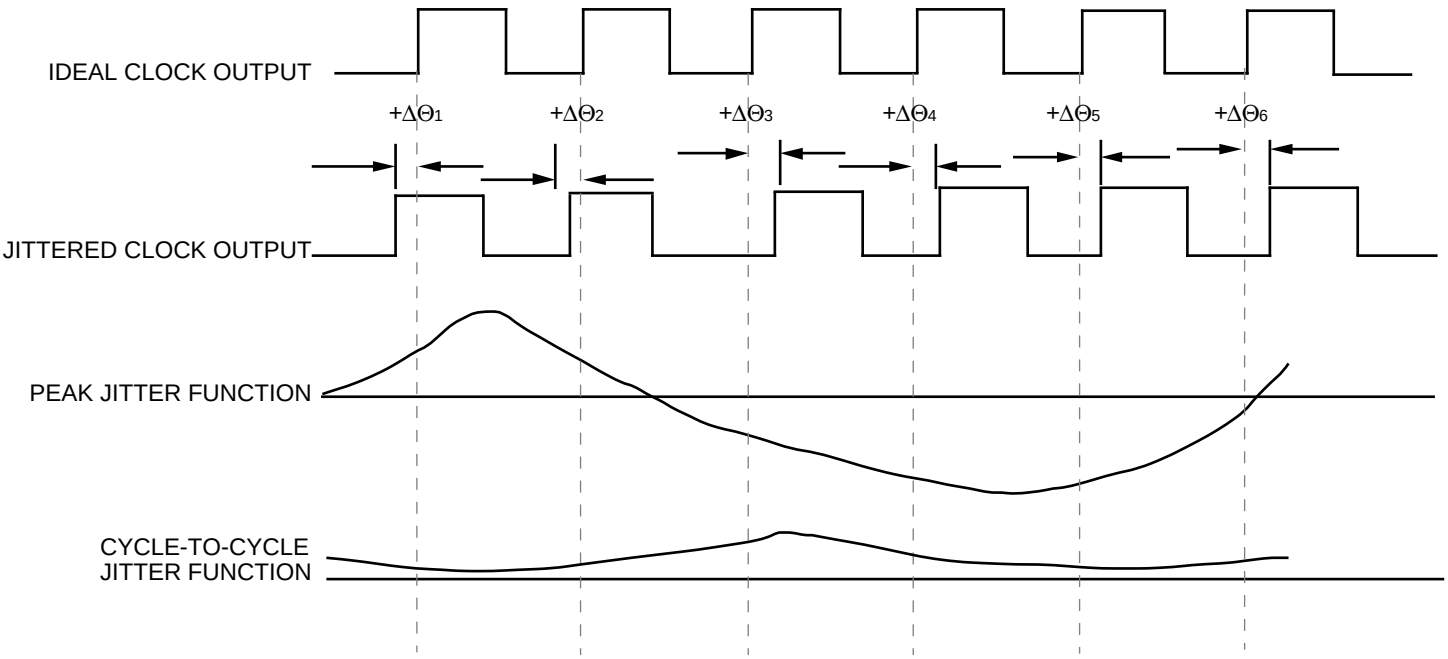


Figure 9. Output jitter

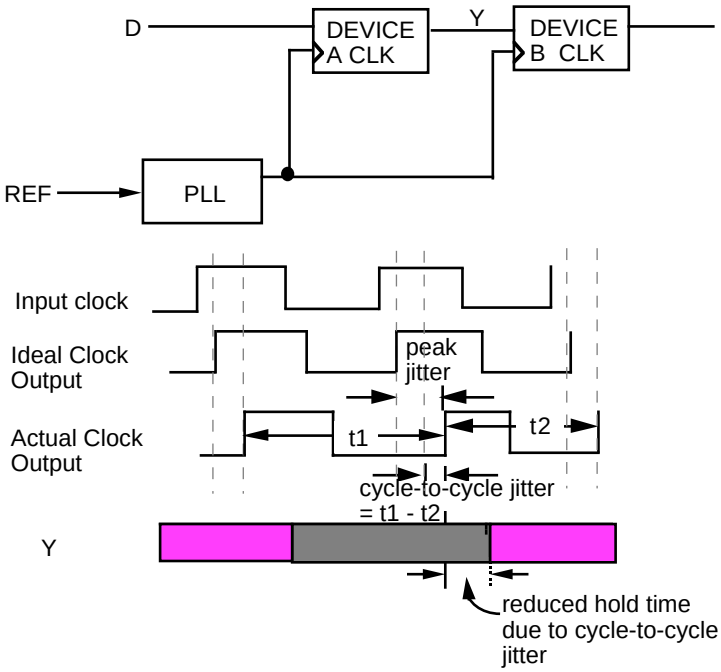


Figure 10 Peak vs Cycle-to-cycle jitter

SUMMARY

This application note seeks to familiarize the reader with PLL operation and terminology. Some background on the fundamental components of a phase-locked loop and a correlation to general control system theory is provided in order to give designers some insight into loop behavior.

REFERENCES

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