

By Stanley Hronik

## INTRODUCTION

Bus-hold retains the last active state on a bus when the bus is disabled or has no active driver. Bus-hold is a function of bus inputs only and is not present on control inputs or bus outputs (except designated I/O ports). Bus-hold components are pin and function compatible with standard Double-Density components, and can be identified by the H in the part number (e.g. FCT162H244T).

## TABLE OF CONTENTS

|                                 |    |
|---------------------------------|----|
| ADVANTAGES OF BUS-HOLD .....    | 59 |
| HOW BUS-HOLD WORKS .....        | 59 |
| BUS-HOLD SPECIFICATIONS .....   | 59 |
| BUS-HOLD CURRENT LEVELS .....   | 60 |
| Hold Characteristics .....      | 60 |
| Overdrive Characteristics ..... | 60 |
| HYSTERESIS .....                | 60 |
| DESIGNING WITH BUS-HOLD .....   | 60 |
| CONCLUSION .....                | 60 |

## **ADVANTAGES OF BUS-HOLD**

Bus-hold provides several advantages over competing design methodologies.

1. Prevents 'floating busses'.
2. Reduces part count (eliminates pull up resistors).
3. Reduces bus loading.
4. Doesn't toggle the bus when the bus is released.
5. Reduces power dissipation.
6. Improves device output hold time

Bus-hold prevents a floating bus. Good design practice dictates that any bus that can transition to a high impedance state should be pulled up<sup>1</sup> to prevent the oscillations that may develop from noise pickup. Additionally a floating bus may increase power dissipation as inputs drift near the toggle region, causing internal device leakage.

The primary competing design practice is the use of pull up resistors on the device inputs. With bus-hold, the pull up resistors can be eliminated, significantly reducing the part count and assembly costs.

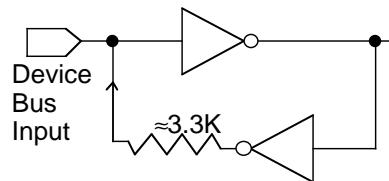
Adding a pull up resistor adds bus loading every time the bus toggles low. With bus-hold, once the transition has been made through the toggle point, the bus-hold input will be assisting the driver rather than fighting and causing a current drain.

When using pull up resistors, the bus will be pulled high when released, causing unnecessary transitions. Bus-hold components will always retain the last known state, avoiding transitions.

In very power sensitive applications, the current leakage of the pull up resistor (when the bus is low) can be avoided with

a bus-hold input. Also, since the input will avoid unnecessary transitions through the input threshold, the device power dissipation will be reduced ( $\Delta I_{cc}$ ).

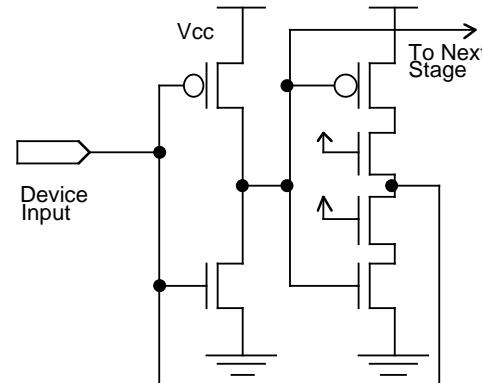
In applications where it is desirable to maintain a longer hold time when a bus goes 3-state (usually memory applications), bus-hold may provide the needed, added margin required.



**Figure 1, Bus-hold Block Diagram**

## HOW BUS-HOLD WORKS

Bus-hold is a small positive feedback current on device inputs. When an input changes logic state, the bus-hold circuit will return a small current back to the device input, effectively adding to the transition of the input. This positive feedback will then hold the final logic level until an active driver toggles the input voltage to the opposite logic state, where bus-hold will then again hold the logic state. A block diagram of a bus-hold input is shown in Figure 1 and the schematic representation is shown in Figure 2.



**Figure 2. Bus-hold Schematic Representation**

## **BUS-HOLD SPECIFICATIONS**

Bus-hold specifications identify the strength of the sustain (hold) current at the TTL logic threshold levels of 2.0V and 0.8V and the overdrive current at the input toggle point (typically 1.5V). Input current levels on a bus-hold circuit should approach zero when the input voltage approaches zero or Vcc as shown in Figure 3. The specified maximum limit on overdrive current has not yet been established.

| Symbol     | Parameter                                       | min. | max. | unit    |
|------------|---|------|------|---------|
| $I_{BHL}$  | Bus-hold LOW Sustaining Current <sup>(1)</sup>  | 50   | —    | $\mu A$ |
| $I_{BHH}$  | Bus-hold HIGH Sustaining Current <sup>(2)</sup> | -50  | —    | $\mu A$ |
| $I_{BHLO}$ | Bus-hold LOW Overdrive Current <sup>(3)</sup>   | —    | tbd  | $\mu A$ |
| $I_{BHHO}$ | Bus-hold HIGH Overdrive Current <sup>(4)</sup>  | —    | tbd  | $\mu A$ |

#### NOTES:

1. The minimum current the bus-hold circuit is guaranteed to sink if a logic LOW input is raised to 0.8V.
2. The minimum current the bus-hold circuit is guaranteed to source if a logic HIGH input is lowered to 2.0V.
3. The maximum current required from an external driver to switch a bus-hold input from a logic LOW to a logic HIGH.
4. The maximum current required from an external driver to switch a bus-hold input from a logic HIGH to a logic LOW

## BUS-HOLD CURRENT LEVELS

Figure 3 shows the typical input current level as the input voltage transitions from zero to 5V (Vcc). It should be observed that the current levels are the highest near the input toggle point of 1.5V as the bus-hold circuit attempts to pull the voltage away from the threshold region. As the input voltage reaches the steady state logic levels of 0.0V for a LOW or 3.5V for a HIGH, the current levels approach zero.

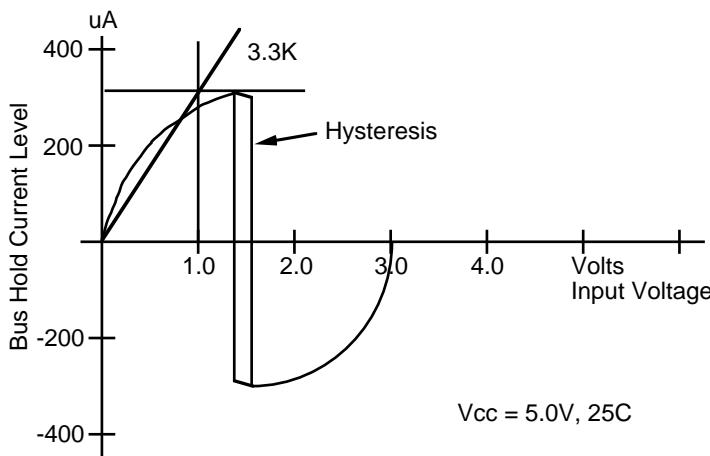


Figure 3, VI Characteristics for Bus-hold

## HOLD CHARACTERISTICS

Examining Figure 3, it can be seen that the slope of the VI curve is approximately  $3.3\Omega$  for voltages of less than 1.5 volts (logic low). Therefore, for a logic LOW condition, bus-hold is typically equivalent to a  $3.3\Omega$  resistor to ground. For voltages of greater than 1.5 volts (logic HIGH), the curve resembles an impedance from  $V_{oh}$  (rather than  $V_{cc}$  as in the case of a resistor). For a rough comparison, this may be compared to a  $3.3\Omega$  resistor to 3.5V (typical).

## OVERDRIVE CHARACTERISTICS

The current necessary to overcome the bus-hold current during an input transition can reach  $500\mu A$  near the input toggle voltage of 1.5V. At 1.5V, most bus drivers are capable of driving a large current, meaning that bus-hold does not affect the bus loading significantly. For example if a Double-

Density Balanced-Drive component were driving a bus-hold component, the Balanced-Drive output drives  $115mA$   $I_{odL}/I_{odH}$  typically at 1.5V. Comparing this to the bus-hold overdrive current of less than  $500\mu A$ , it can be seen that the bus-hold input (or several bus-hold inputs tied together) would not have a significant loading effect on the driver. It is easier to overdrive a bus-hold input than to drive a pull up resistor of equivalent value to a logic LOW.

## HYSTERESIS

All of IDT's logic components have input hysteresis including bus-hold components as shown in Figure 3. The addition of bus-hold to an input amplifies the effect of input hysteresis by driving the bus-hold current back into the source impedance of the driving circuit. The amplitude of this effect is dependent upon the source impedance of the driver.

## DESIGNING WITH BUS-HOLD

Bus-hold can be used in most applications in place of a pull-up resistor. When bus-hold is used, there is no need to tie unused device inputs high or low, but doing so has no adverse effects. One bus-hold component on a bus is all that is required to hold the bus, but as many bus-hold inputs as desired can be tied to the same bus. If large quantities (100s) of bus-hold inputs are tied together, the designer must insure that the bus driver has sufficient drive capability to drive the components beyond the 1.5V threshold.

## CONCLUSION

Components with bus-hold offer several advantages over the use of external pull up or pull down resistors. With the cost of bus-hold components at parity with standard components, most applications can benefit from the use of bus-hold components.

#### NOTES

1. References to "pull-up" also imply "pull down" with the necessary adjustments throughout the document.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).