QUALITY SEMICONDUCTOR, INC.

Use Quickswitch® Bus Switches to Make Large, Fast Dual Port RAMs

Application Note AN-12

Abstract

Dual port RAMs are effective devices for high-speed communication between microprocessors. Typical dual port RAMs are specialty SRAMs of small size (1K to 4K bytes) and medium speed (25-50ns). Because of their relatively low density, it is usually impractical in terms of chip count and cost to make large dual port RAM systems from these chips. There is another approach to making dual port RAMs, however. QuickSwitch bus switches can be combined with standard high-speed SRAMs to make large, fast time shared dual port RAMs and high-performance pingpong RAM systems at low chip count and low cost.

Background

A dual port RAM is a single RAM, typically an SRAM, which can be accessed simultaneously from two different ports, one port per microprocessor. Each microprocessor sees a simple SRAM interface, and the contents of the SRAM are common to both microprocessors. A block diagram of a dual port RAM in a dual microprocessor system is shown below. In this case, a conventional CPU communicates with a DSP CPU through the common memory of the dual port RAM.

A true dual port RAM has one set of SRAM cells and two independent sets of addressing logic, called ports. The RAM cells may be read or written by either side independently and simultaneously. This capability is valuable because each port may access the RAM cells without regard to activities on the other port. There is one exception to this simultaneous access. If one port is writing to a cell while the other port is reading the same cell, the data may be changing during the read which could cause errors. Most dual port RAMs provide address contention logic to prevent this unlikely condition by causing one side to wait if both are trying to access the same cell.

True dual port RAMs have some limitations. The dual port RAM cell is approximately twice as large as its single port SRAM counterpart. This makes true dual port RAMs more expensive than SRAMs, especially at higher densities. However, there is more than one way to achieve the dual port RAM function.

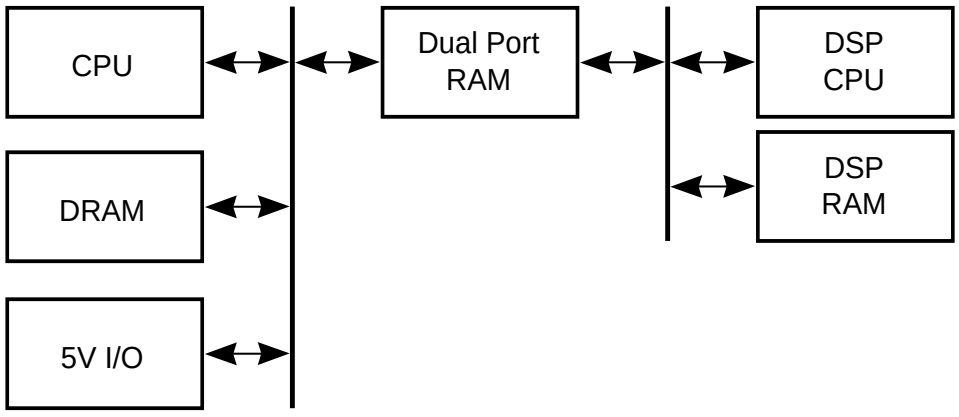

Figure 1. Dual Port RAM in Dual Microprocessor System

Time Shared Dual Port SRAM

The dual port RAM function requires that each port have a simple SRAM interface and its access be independent of activity on the other port, to a first approximation. If the system timing for both ports is related or synchronized such as by being generated from the same clock, a dual port RAM function can be created by time sharing a single SRAM. This approach uses conventional SRAMs which combine high-density, high-speed and low cost. A block diagram of this approach is shown in Figure 2.

In the system shown in Figure 2, a single SRAM is switched between the two buses of the CPU and the DSP CPU. A flip-flop (FF) driven by the clock is used to switch the SRAM between the buses. Let us assume, for the moment, that both CPUs are driven by the same clock and have the same bus transfer conditions, i.e., that an SRAM read or write transfer can be completed in one clock pulse.

When the SRAM is connected to one bus, it is temporarily unavailable to the other bus. However, this condition lasts for only one clock period. In this case, the FF can be used to drive the WAIT input of each CPU if that CPU attempts to access the SRAM when it is connected to the other bus. This means that the dual port SRAM has an access time of 1.5 clock periods because the accessing CPU will have to wait one clock period 50% of the time. More sophisticated logic and timing could eliminate this 0.5 clock period wait state in most cases, if necessary.

There are several advantages to the time shared dual port SRAM. Conventional SRAMs can be used, allowing high-density and speed at low cost. Since one switch is used, the SRAM subsystem can be of arbitrary size; a big dual port SRAM is as easy to make as a small one. Finally, there is no contention between the two ports. Contention occurs in true dual port SRAMs when the same cell is being simultaneously written by one port and read by the other port. In this case, data will be changing during the read. This does not occur in time shared dual port SRAMs because the time shared SRAM is connected to only one port at a time. The write operation occurs at a separate time from the read, and the read data cannot change during the read.

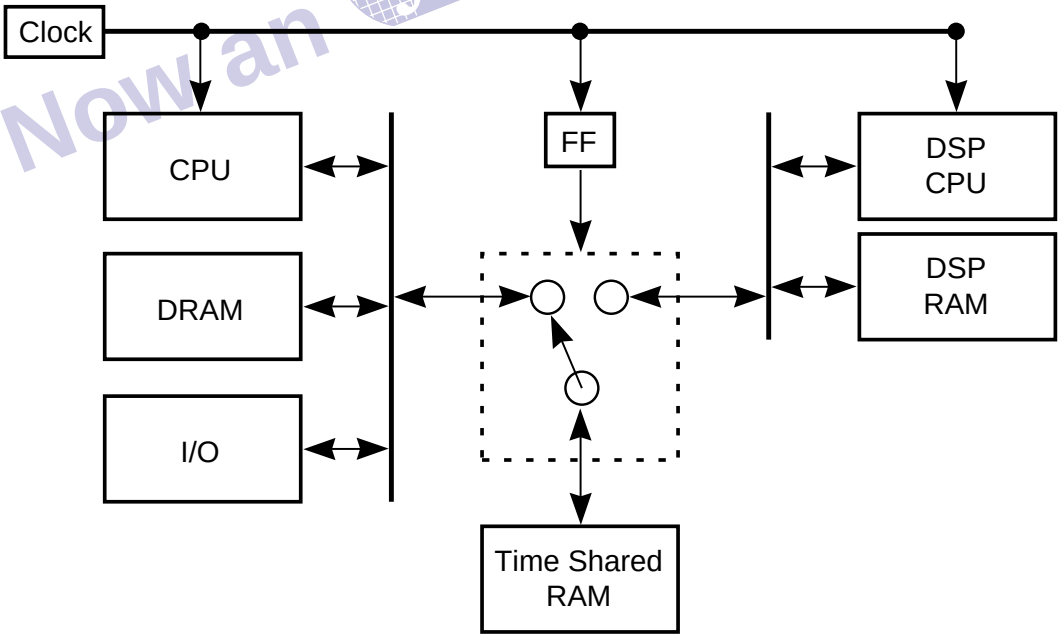

Figure 2. Time Shared Dual Port SRAM

Time Shared Dual Port SRAM Timing

A block diagram of a time shared dual port SRAM using QS3383 bus exchanger for the switching element is shown in Figure 3. The QS3383 devices are being used as 2:1 multiplexers. Each QS3383 controls 5 signals. A 64Kx16 SRAM with 16 address, 16 data, one WE and one OE line have (16+16+1+1) = 34 signals and require seven QS3383 devices.

A timing diagram of this design is shown in Figure 4. Shown in the timing diagram is a read cycle on bus A followed by a write cycle on Bus B. The effective access time of the SRAM for the read cycle is the bus switch time plus the SRAM T_{AA}. The switch time is the sum of the FF settling time and the QS3383 switch time. For a FF such as the 74FCT374C with a clock to output delay of 5.2ns and a QS3383 with a switch time of 6.5ns, the total switch time is 5.2 + 6.5 = 11.7ns. If a 10ns T_{AA} SRAM is used, this results in an effective T_{AA} of 21.7ns. The cycle time for the write cycle is the same, with both address and write data being delayed by the QS3383 QuickSwitch switching time. Thus, it is reasonable to construct a time shared SRAM with a 25ns half cycle time, allowing operation on 40MHz buses. If the delay through the FF can be compensated for, 20ns half cycle times may be possible, corresponding to 50MHz buses.

Note that the SRAM Write Enable (WE) input must be HIGH on both ports when the buses are being switched. Since this occurs at the beginning of the cycle when the WE signal on both buses is HIGH (assuming the same bus timing), the QS3383 output will remain HIGH when switching between them.

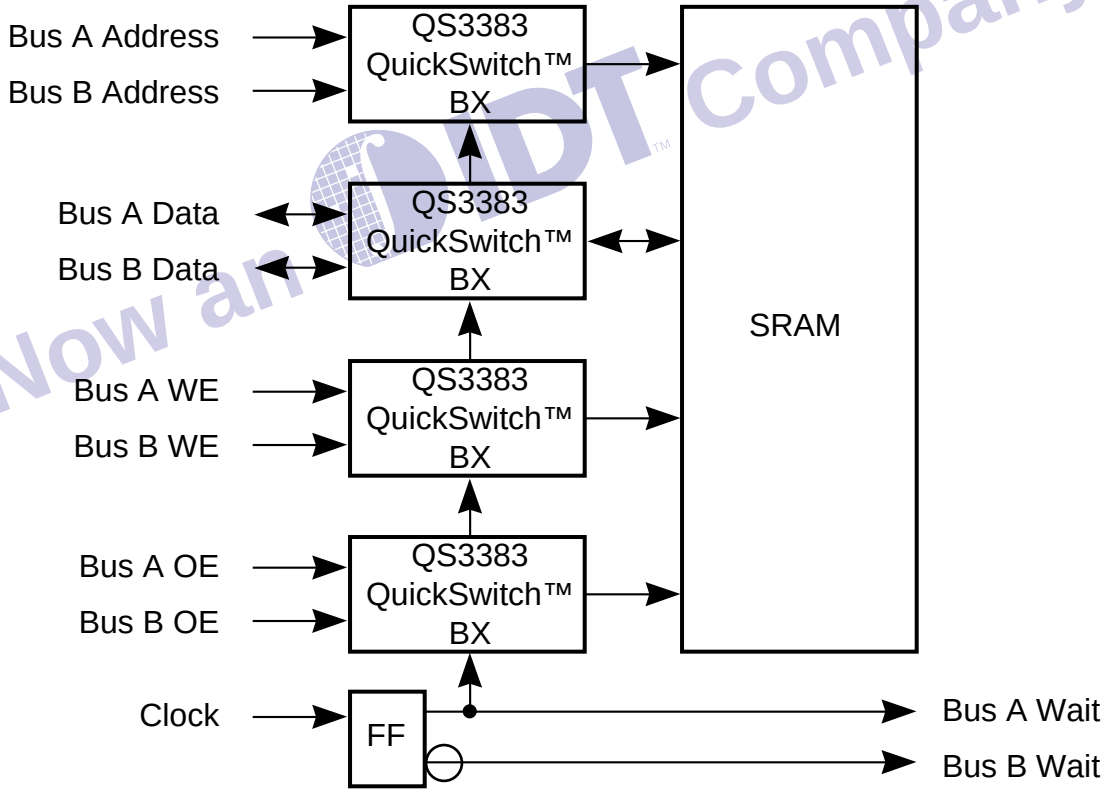

Figure 3. Time Shared Dual Port SRAM Using QuickSwitch

Ping Pong Dual SRAM

The highest performance dual port RAM architecture is the ping pong RAM shown in Figure 5. The ping pong RAM provides the ability to exchange blocks of data between processors rather than individual words. In the ping pong RAM, two RAMs are used, one for each processor. Each processor performs data on the contents of its RAM. When computation is complete, the two RAMs are exchanged. This approach allows a dual port function with performance equal to that of the individual SRAMs. The design of Figure 5 uses QS3383 QuickSwitch bus exchange switches with two SRAMs to form a ping pong dual SRAM system. When the BX line to the QS3383's is in one state, the DSP CPU is connected to SRAM A and the main CPU is connected to SRAM B; in the other state, the QS3383's connect the DSP CPU to SRAM B and the main CPU to SRAM A.

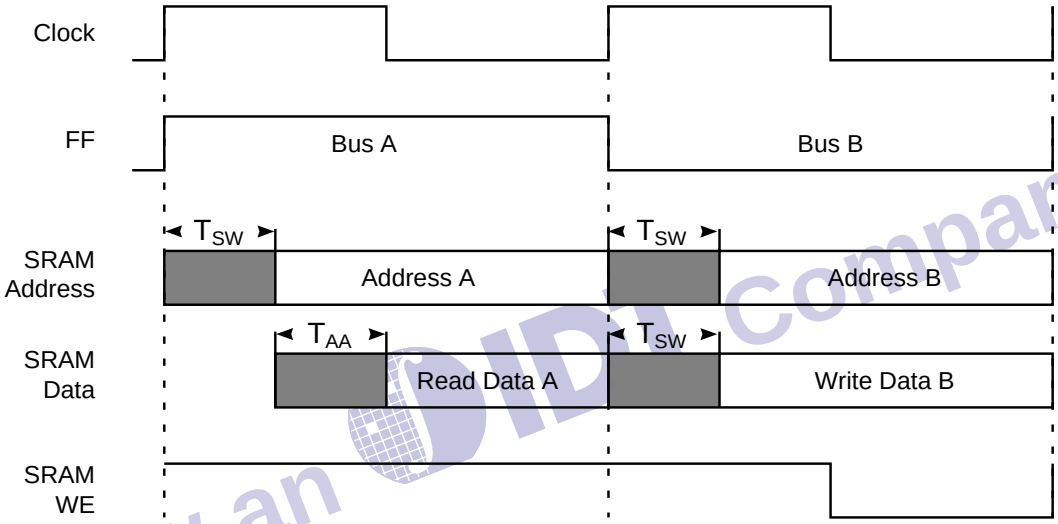

Figure 4. Time Shared Dual Port SRAM Timing Diagram

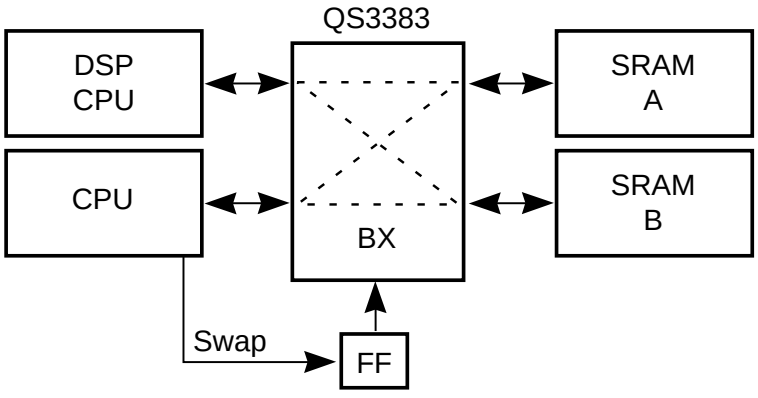

Figure 5. Ping Pong Dual SRAM System

In a typical operating sequence, the DSP CPU works on data in SRAM A, while the main CPU works on data in SRAM B. The DSP CPU could be working on an DSP calculation using the data in SRAM A, while the CPU retrieves the results of the previous DSP calculation in SRAM B and sets up the next calculation. When the DSP calculation is complete, the CPU sends a clock to the flip flop (FF) which causes the two SRAMs to be effectively exchanged. The DSP CPU now accesses SRAM B, while the main CPU accesses SRAM A.

The advantage of using the QS3383 in this ping pong RAM design is that the QS3383's introduce no propagation delay. They connect the selected SRAM to its CPU "just like a wire". The only exception to this is the few nanoseconds of delay when the QS3383's exchange the SRAMs. This means that very fast ping pong RAM systems can be made. The speed of the ping pong RAM is equal to the speed of the individual SRAMs. Systems with 10ns access time are possible, for example. Also, there are no restrictions on RAM type: i.e., burst mode SRAMs are as readily accommodated as standard types.

There is an additional advantage to using QS3383's to make a ping pong RAM system. Because the exchange function is incorporated into the QS3383, a ping pong RAM system can be made in half the number of packages that would be required in a slower design using conventional TTL bus logic devices.

Conclusion

QuickSwitch bus switches can be used to overcome the limitations of conventional dual port RAMs. They can be combined with standard high-speed SRAMs to make large, high-speed, time shared dual port RAMs and high-performance ping pong RAM systems at low chip count, low board area and low cost.