Design Tool Overview

The active filter design tool (hereafter called the "tool") is intended to accelerate a designer's progress towards a working filter implementation by assisting in the op amp selection and component value solutions. The tool is intended to support LowPass (LP), HighPass (HP), and Bandpass (BP) filter requirements – as of this revision (1), the LowPass is implemented with HP and BP intended for addition to the tool in 2010.

As with most board level, op amp based, active filter design tools, this tool proceeds to implementation through a combination of 1st and 2nd order filter stages. A desired higher order filter shape (>2) will be built up as a combination of 1st and 2nd order stages. The tool currently supports 2nd through 6th order designs which would then require 1 to 3 amplifier stages. Any desired filter will have a frequency range in which the input signal is intended to be passed to the output with some gain. The tool works in gain "magnitude" but allows each of the stages to be set up for either a non-inverting or inverting signal gain in that stage.

While the known universe of op amp based active filter circuit implementations is truly immense, this tool limits the available topologies for design implementation to a manageable subset of those. These 4 circuit topologies are (for the LP case).

1st Order Stages

Buffered single pole for non-inverting signal path (this is an RC pole followed by a non-inverting gain stage).

Active single pole for the inverting signal path (this is an RC in the feedback path of an inverting op amp configuration).

2nd Order Stages

Sallen-Key (on VCVS) for the non-inverting signal path stages.

Multiple Feedback (MFB – also known as infinite gain) for the inverting signal path stages.

Design flows can follow one of two paths through to implementation. The default is a semi-automatic flow where the designer selects which of several standard filter shapes they desire and lets the tool allocate the stage gains and Fo, Q for each stage. The alternate path, if for instance the designer has desired poles and stage gains from some other source or previous design, is to select the manual pole entry feature and proceed by entering the desired pole locations and gain for each stage. The manual path also expands the range of allowed frequencies and gains beyond the semi-automatic flow.

Getting Started

The entry point for the iSim SmartFilter tool is shown in Figure 1– a log-in page along with a graphic illustrating the flow through the tool.

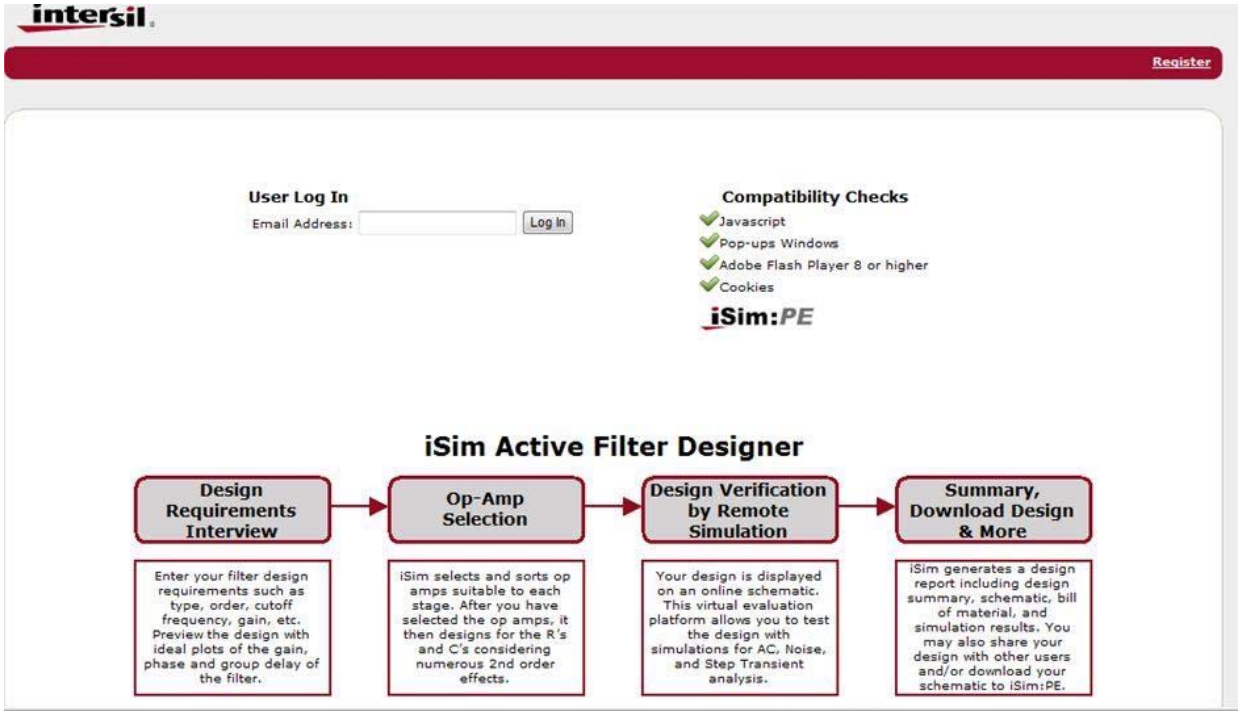


FIGURE 1. ENTRY POINT FOR ISIM ACTIVE FILTER DESIGNER

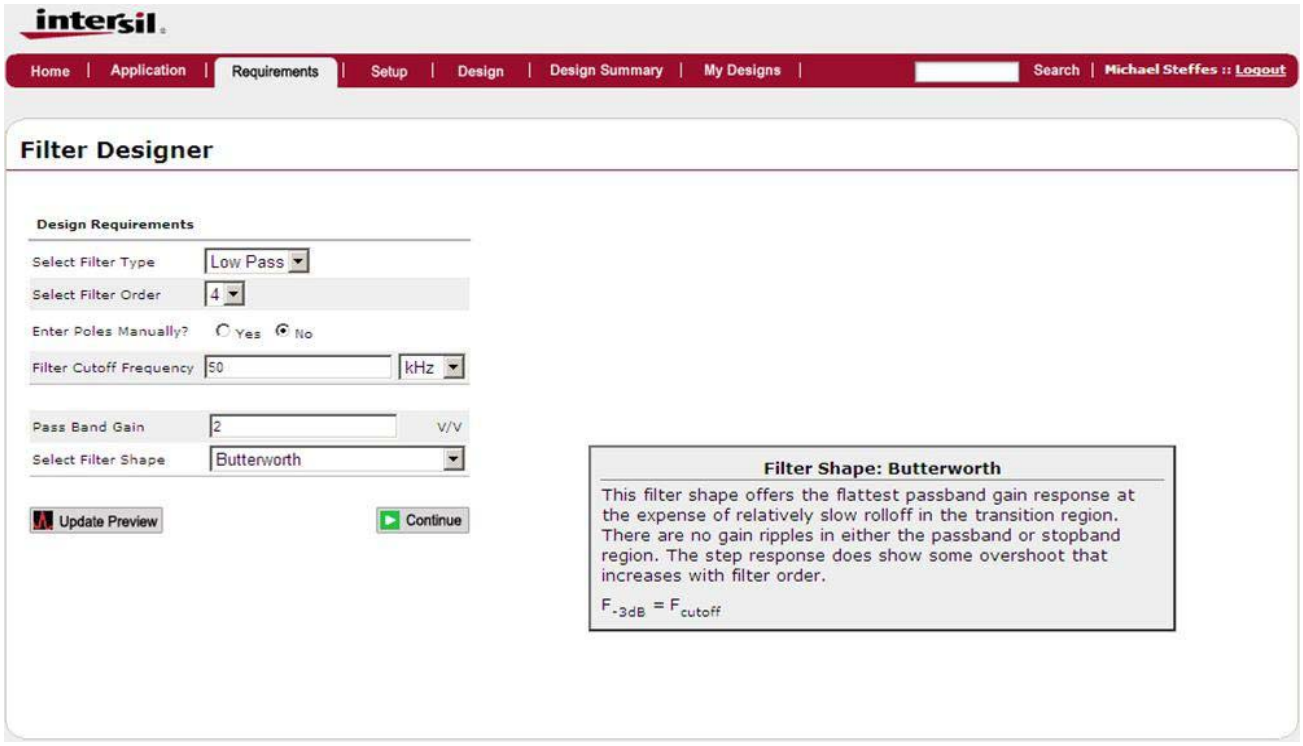


FIGURE 2. "REQUIREMENTS" SCREEN

Once you are logged in, every stage of the tool starts with default selections and values – those defaults will be noted throughout this description. There are also built in user entry limits to bias the design flow towards a successful implementation – these will also be noted throughout the discussion.

The easiest path is for the designer to select:

1. Filter Type – Low Pass, High Pass, or Bandpass (Low Pass is default)
2. Filter order from 2 to 6th order (4th order is default)
3. Passband Gain (total gain from input to output in V/V from 1 to 10 for the semi-automatic design flow). Filter gains are always magnitude only, but inverting implementations are supported in the design flow. (default gain is 2V/V or 6dB)
4. Fcutoff for the Low Pass Filter – limits are currently 20Hz to 20Mhz for the semi-automatic flow and 5Hz to 50Mhz for the manual pole entry. (default is 50kHz)
5. Filter shape – preselected options depending on filter type. For the low pass, this defaults to "Butterworth".

This "Requirements" screen, immediately after login, appears as shown in Figure 2.

The alternate path is for the designer to manually enter the desired stage characteristics for 1 to 3 stages (set by the selected filter order) after the filter type and order are selected. In this flow an expanded range of frequencies and gains are allowed to push the limits of the available devices in the tool. The user entered items in the "Requirements" page for the manual option are as follows:

1. Fo and Q for each stage (can also be entered as real or imaginary un-normalized pole locations). Min/max range on Fo is 5Hz to 50Mhz while Q for 2nd order stages must be between 0.5 and 10.
2. Stage gain (1 → X where maximum X depends on the number of stages desired):
    a. 1 stage; maximum gain is 20
    b. 2 stages; maximum gain is 10 in each stage for a maximum cascaded gain of 100V/V (40dB)
    c. 3 stages; maximum gain is 5 in each stage for a maximum cascaded gain of 125V/V (41.9dB)

Choosing to follow the preset filter shape path will also implement the design in a recommended Fo, Q and gain (Kn) sequence for multiple stage designs. For the low pass flow, this sequence is intended to achieve an improved implementation considering the following factors (these apply mainly to designs where the filter gain >1 and the order >2).

1. For a given Fcutoff for the total filter, the higher Q stages operate at lower gains while the lower Q stages provide more of the total gain (for filters with a total gain > 1). This acts to hold the required amplifier bandwidths clustered in a tighter range allowing designs an improved probability of using the same device.
2. Placing the high Q, lower gain, stages earlier in a multistage design (order >2) will also act to hold the required slew rates more tightly clustered - again improving the probability of using a single op amp model number in a multi-stage design. This again applies mainly when the overall filter gain >1.

3. Sequencing the poles from high Q to low Q in ascending gains (for order >2) will also act to reduce the possibility of output clipping due to step response overshoot or frequency response peaking in each individual stage.
4. Reducing the Q from first stage to last stage will also act to lower the broadband integrated noise output from the filter. High Q stages will always show a high spot noise peak in the frequency response and following these by lower Q or real pole stages will act to attenuate that peak relative to a design where the highest Q stage is the last stage.

The gain allocations and 2nd order stage sequencing can be manually entered by following the manual pole entry path. This allows alternate implementation plans from 3rd party filter design tools to be tested within the context of the iSim Active Filter Designer.

Both the manual and semi-automatic path designs place any real pole (total filter order equal to 3 or 5) as the last stage. This has significant noise and stopband rejection advantages. Any filter design developed inside the Active Filter Designer, can be ported to the iSim PE Spice simulator tool where numerous other re-design options are possible. This includes re-sequencing the stages to put the real pole first as described in "Appendix 3" on page 41.

Once the target pole locations and gains for each stage are set through either the built-in algorithms, or through manual entry, the tool proceeds to implementation through 3 steps, as follows:

1. Design constraint definition and op amp selection for each stage
2. Design solution with simulation options and re-design features
3. Summary design information

Each will be described in detail for the different filter types.

The emphasis for the iSim Active Filter Designer is to provide a successful implementation for a desired filter shape applying a wide range of Intersil op amps. While there is a moderate capability to preview possible filter shapes (from a set of pre-loaded choices or the manually entered pole locations), **the tool is not intended as a filter shape design tool**. If the available standard shapes provided in the tool do not encompass the designer's needs, a manual pole entry feature is also provided to implement a filter shape derived from an alternate source. There are numerous vendor, or academic, tools available that focus on deriving the required order and pole locations for a desired filter shape. Those results can then be used in the tool through the manual entry feature to take advantage of the numerous implementation features built into this tool.

Disclaimer: *As the tool evolves and enhancements are added, some of the example Figures shown in this user's manual may appear different in the "live" version of the tool.*

Quick Start Example

Once you are logged into the tool, it is very easy and quick to arrive at a proposed active filter design. You need only pick the filter order, Fcutoff, total gain, and filter shape to proceed to the next stage of the design (picking op amps). Using the semi-automatic flow, let's design a 5th order, equiripple phase 0.5deg with an Fcutoff of 20kHz and a total gain of 10. This filter gives a very nice step response with minimal overshoot and ringing. Logging in and entering these settings into the "Requirements" fields and hitting "Update Preview" will display the screen shown in Figure 3.

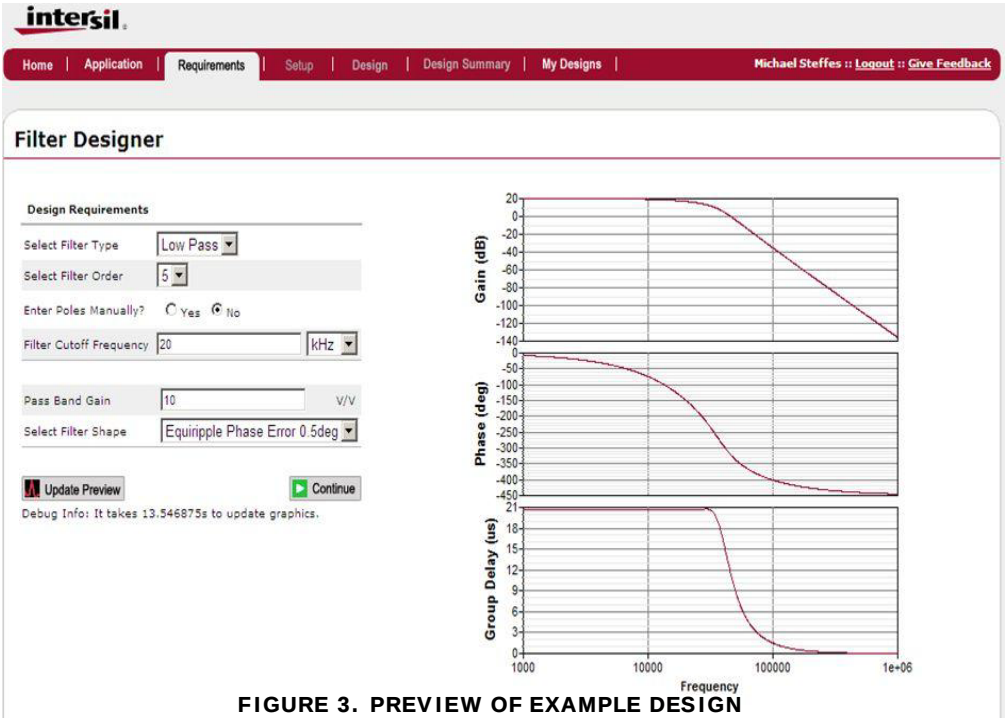


FIGURE 3. PREVIEW OF EXAMPLE DESIGN

The top plot shows the low frequency gain of 20dB (10V/V) while the bottom shows the almost constant group delay to 1.5XFcutoff typical of this filter. These ideal calculated gain, phase, and group delay will be used later to compare to the actual filter simulated AC response.

Hitting "Continue" from this screen goes to the "Setup" screen where the tool generated stage poles and gains are displayed along with the design constraints. Doing that displays the screen of information shown in Figure 4.

Here, this 5th order design has been broken into 3 stages where the Stage3 is the "active" stage for updating the part selection in that stage. The targets for each stage are listed across the top and the "active" stage is indicated by the Red tab of Stage3. Entering this screen from the "Requirements" page starts with the default design constraints shown in Figure 4. All stages are non-inverting (but can be switched to inverting in the drop down above the schematic) and the design starts with:

- 5V total supply voltage (this will be split in ± halves for the design)
- $2V_{P-P}$ output swing as a final stage nominal maximum output swing
- 1% resistor tolerances

In this screen, the tool has already selected a proposed op amp for each stage. These are listed in red in the stage description boxes across the top. **The design constraints can only be updated when the last stage is "active" since it is looking for the final output voltage swing of the filter as a critical piece of design information.**

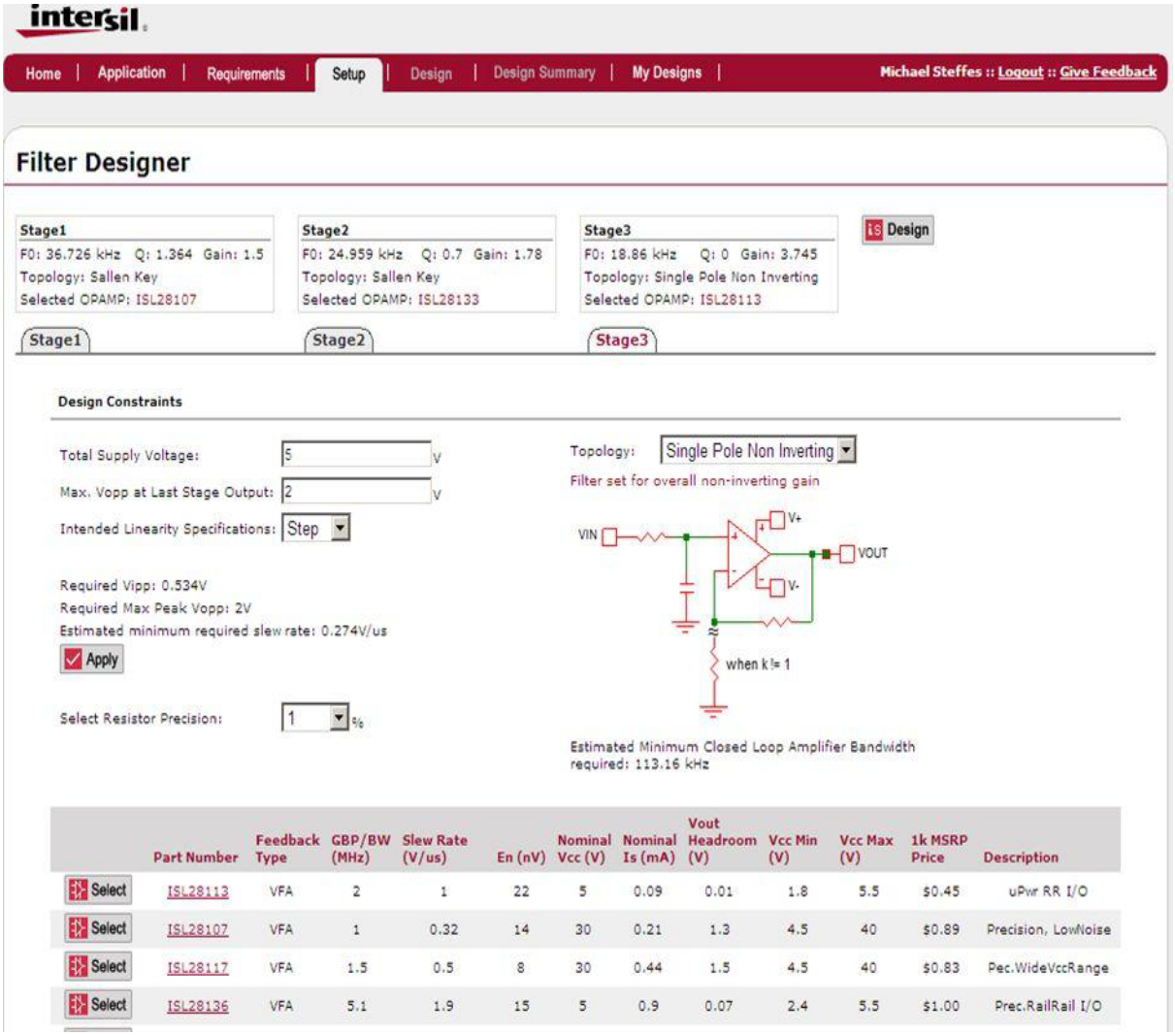


FIGURE 4.

Changing the supply voltage to 30V and the desired output swing to 20V and hitting the "Apply" key, will display the screen shown in Figure 5.

Here, the amplifier list has been rescreened for this new set of application conditions. There are a limited number of op amps to choose from at 30V total supply and this speed, and the tool has already selected the ISL28127 for each of the 3 stages as the best solution.

A short listing of op amp specifications are included at the bottom for op amps selected as suitable to this stage. This list will often update to a different set of parts at each stage. To see those, click the Stage2 or Stage1 tabs to check and/or select the op amp for that stage. Hitting "Design" will execute the solution for the R's and C's and take you to the "Design" tab.

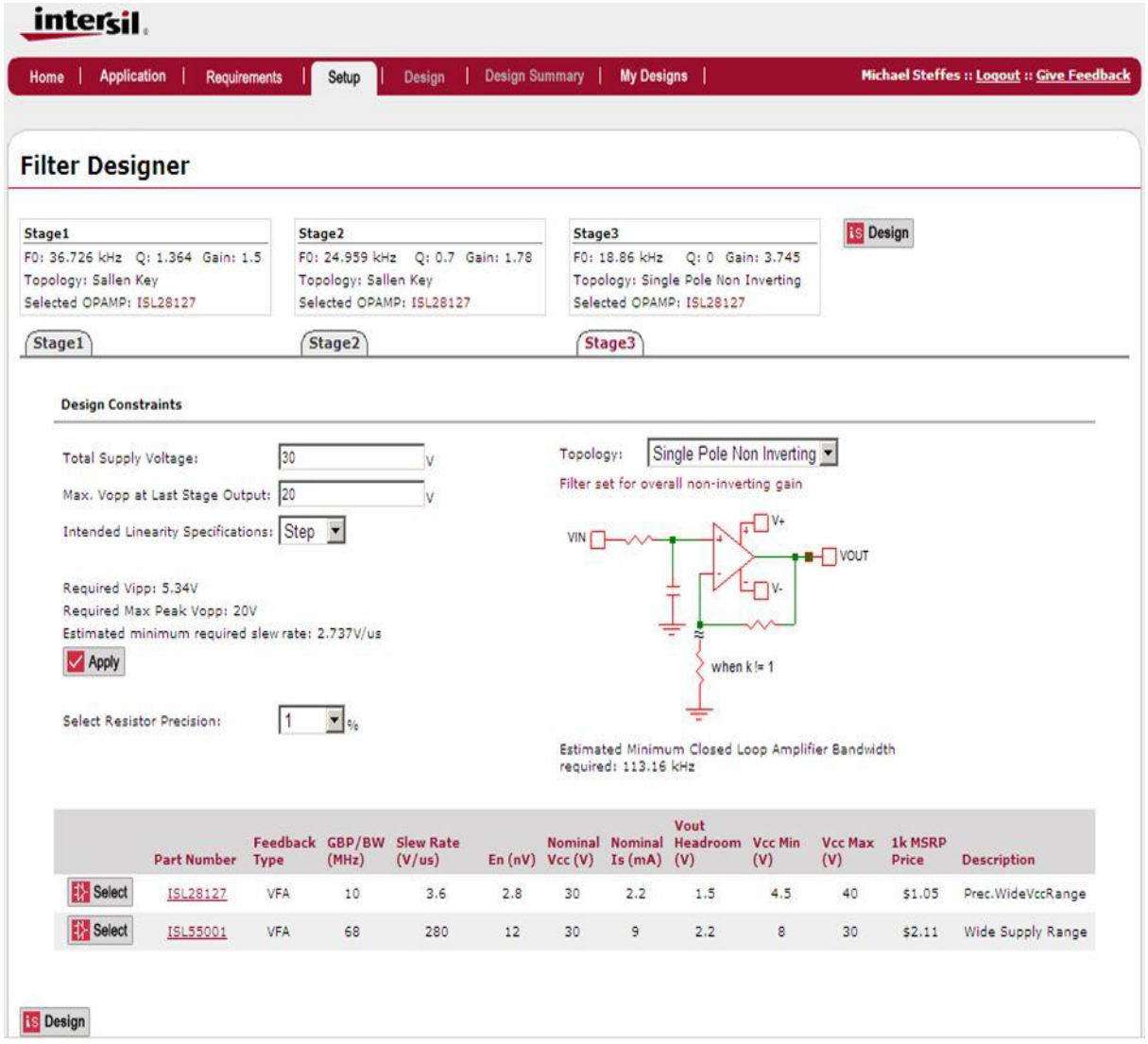


FIGURE 5.

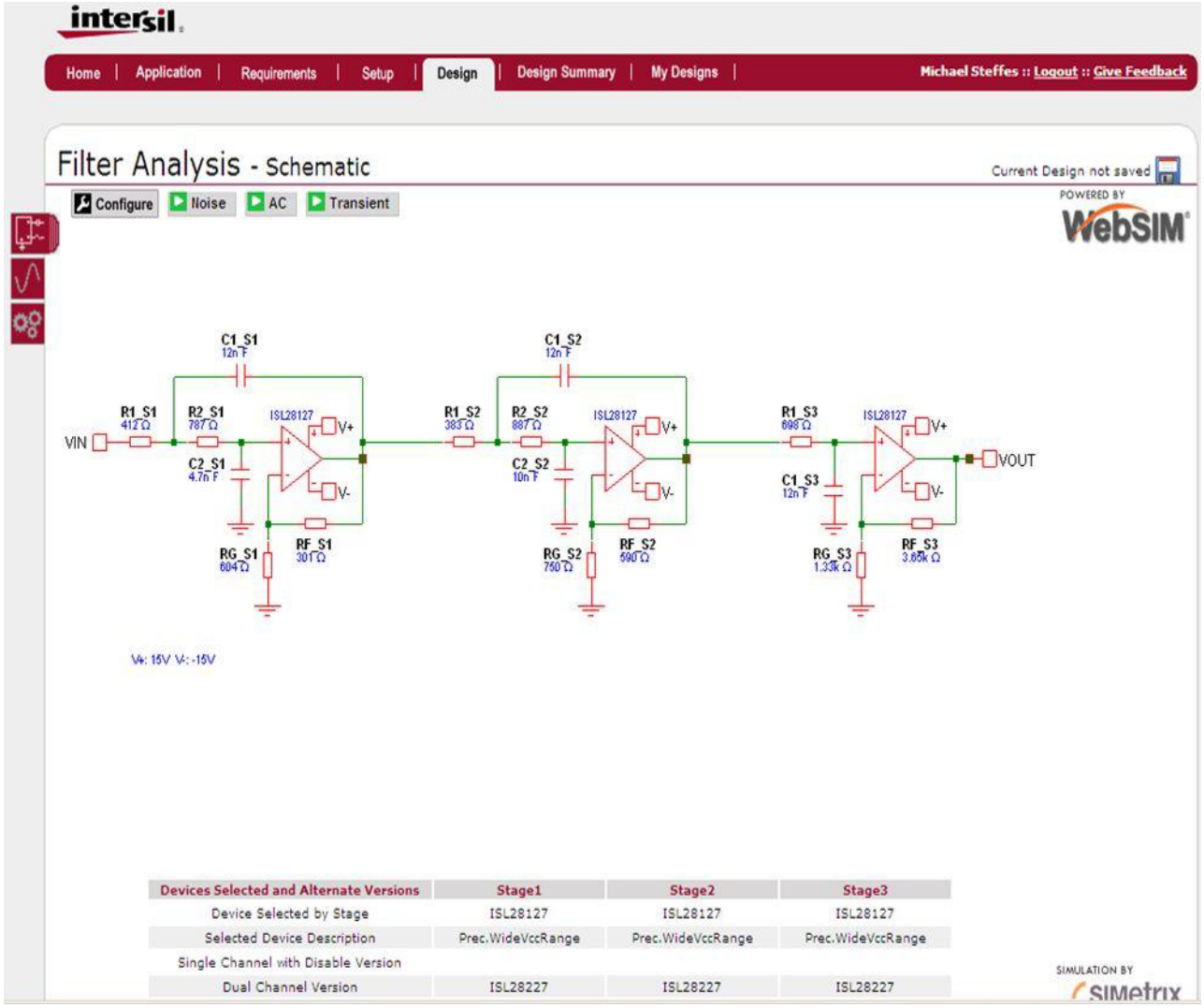


FIGURE 6.

Figure 6 shows the proposed implementation circuit with the 3 possible simulation options listed in green across the top. Hitting the "AC" tab will display the screen shown in Figure 7.

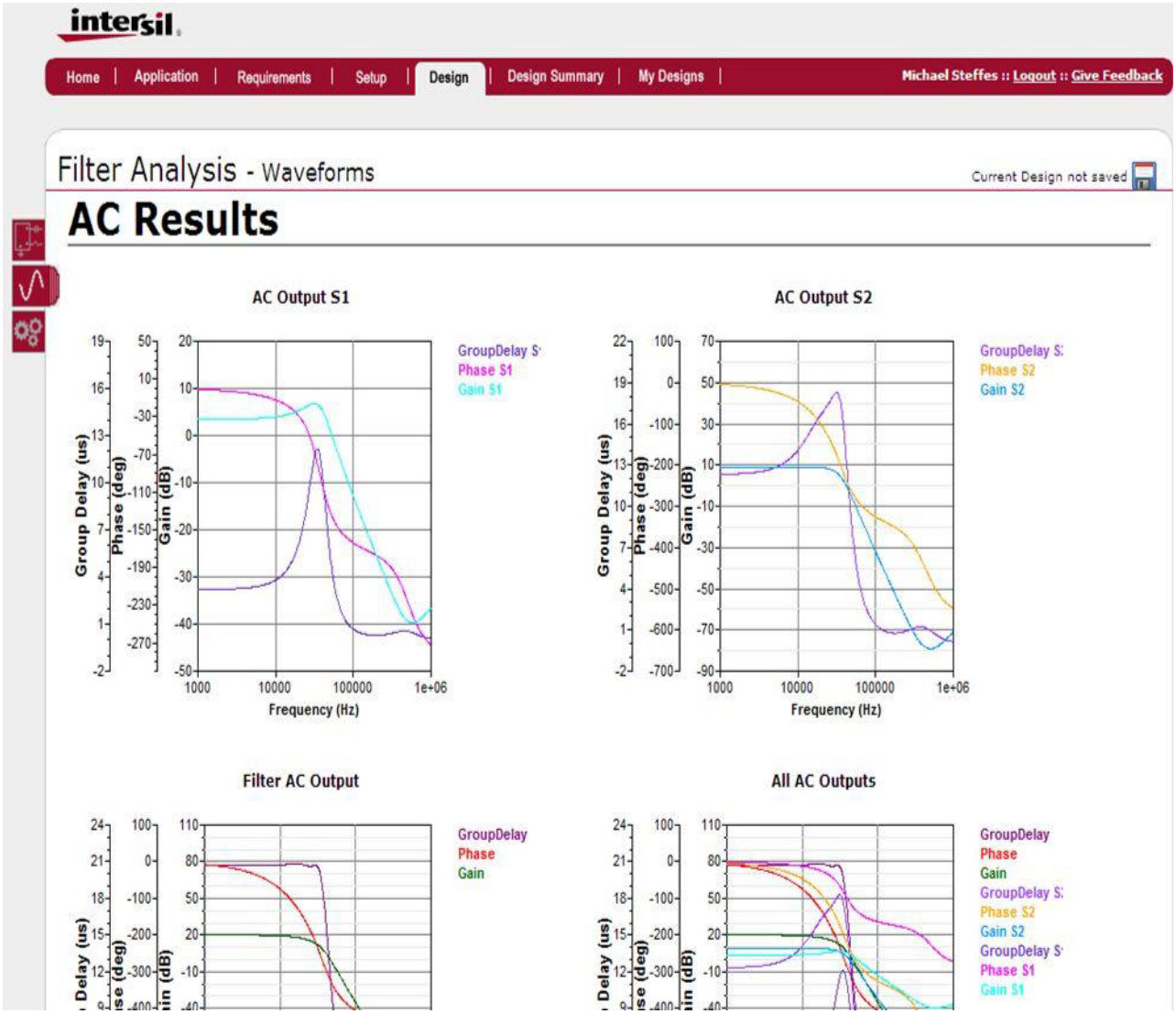


FIGURE 7.

The tool delivers outputs for each stage, the final output (Filter AC output, lower left) and all outputs. Clicking on any plot opens up a waveform viewer. Doing that on the Filter AC output and selecting to add the "Ideal" outputs on the upper right (from the preview plots) will show the following screen (Figure 8) where the very close match to ideal is shown.

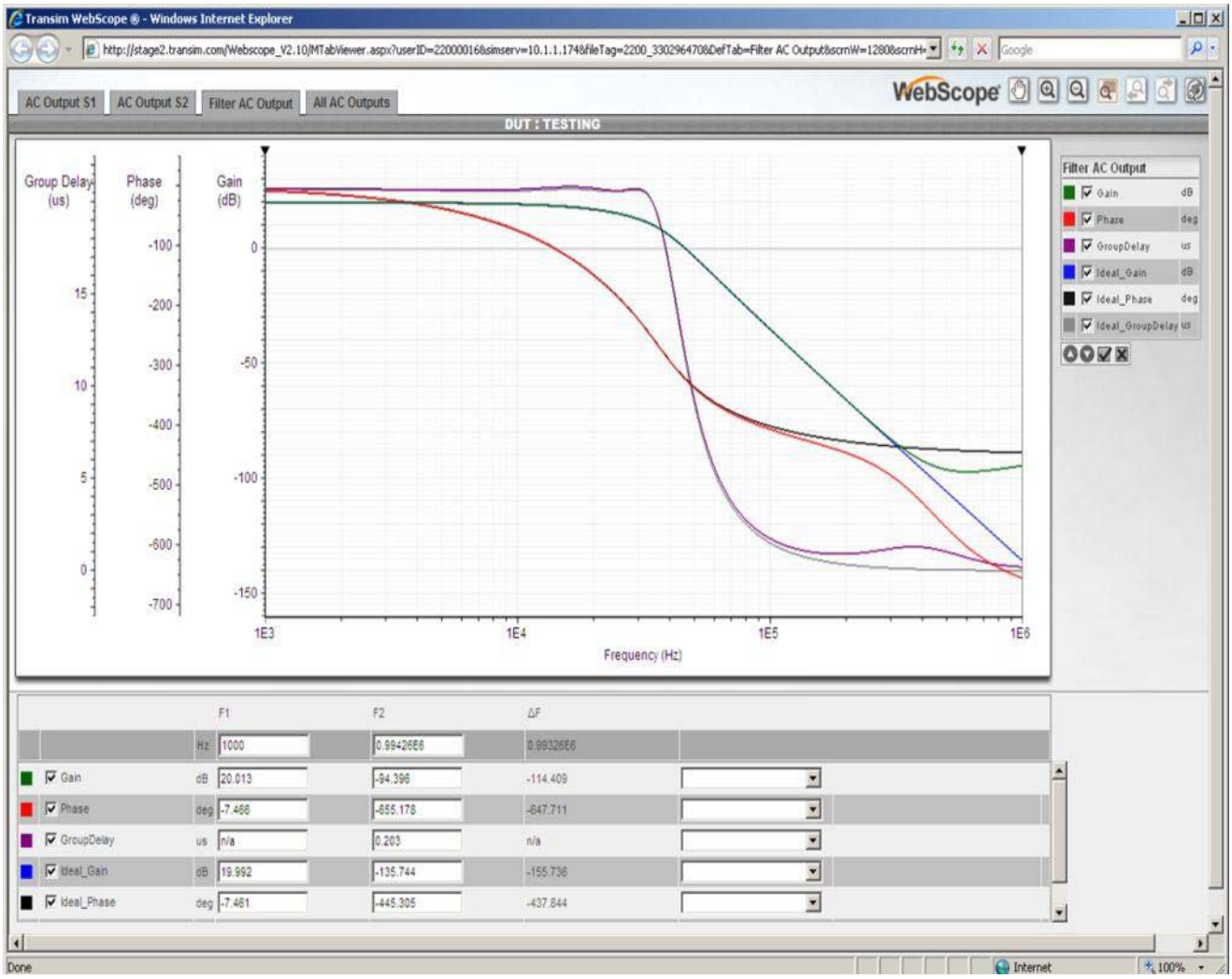


FIGURE 8.

Since this filter shape is supposed to have a very good step response, going back to the "Design" tab and hitting the Transient key, and clicking on those output plots for "All Outputs" will show the build-up of the target $20V_{P-P}$ swing in the final output progressing through the filter. This is going to the waveform viewer window. Here we see the input waveform (±2V) and then the overshooting outputs of the first 2 stages. The final stage delivers the very low overshoot final step response as desired.

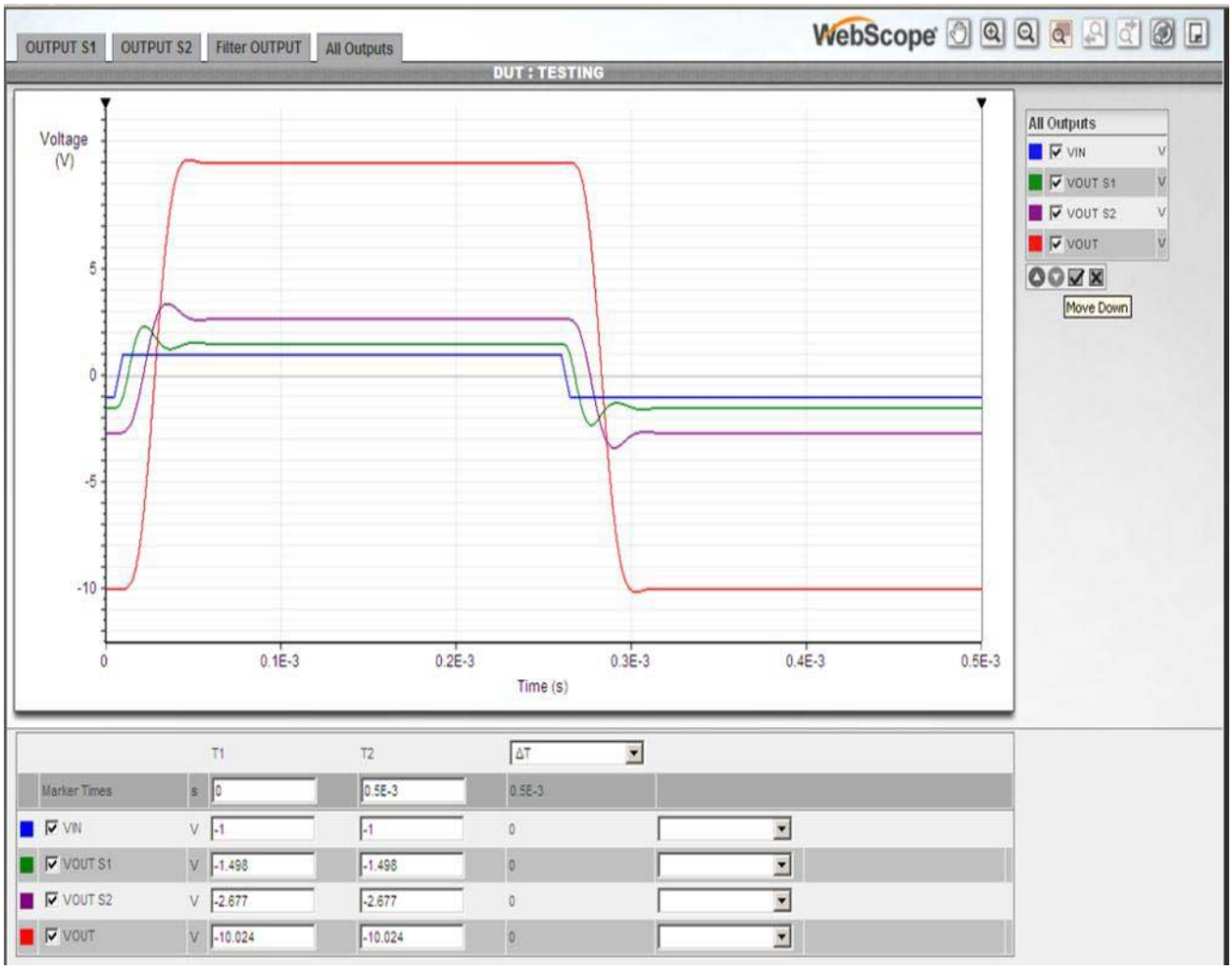

OUTPUT S1
OUTPUT S2
Filter OUTPUT
All Outputs
WebScope
DUT : TESTING
Voltage (V)
5
0
-5
-10
0
0.1E-3
0.2E-3
0.3E-3
0.4E-3
0.5E-3
Time (s)
All Outputs
VIN
VOUT S1
VOUT S2
VOUT
Move Down
T1
T2
ΔT
Marker Times
s
0
0.5E-3
0.5E-3
VIN
V
-1
-1
0
VOUT S1
V
-1.498
-1.498
0
VOUT S2
V
-2.677
-2.677
0
VOUT
V
-10.024
-10.024
0

FIGURE 9.

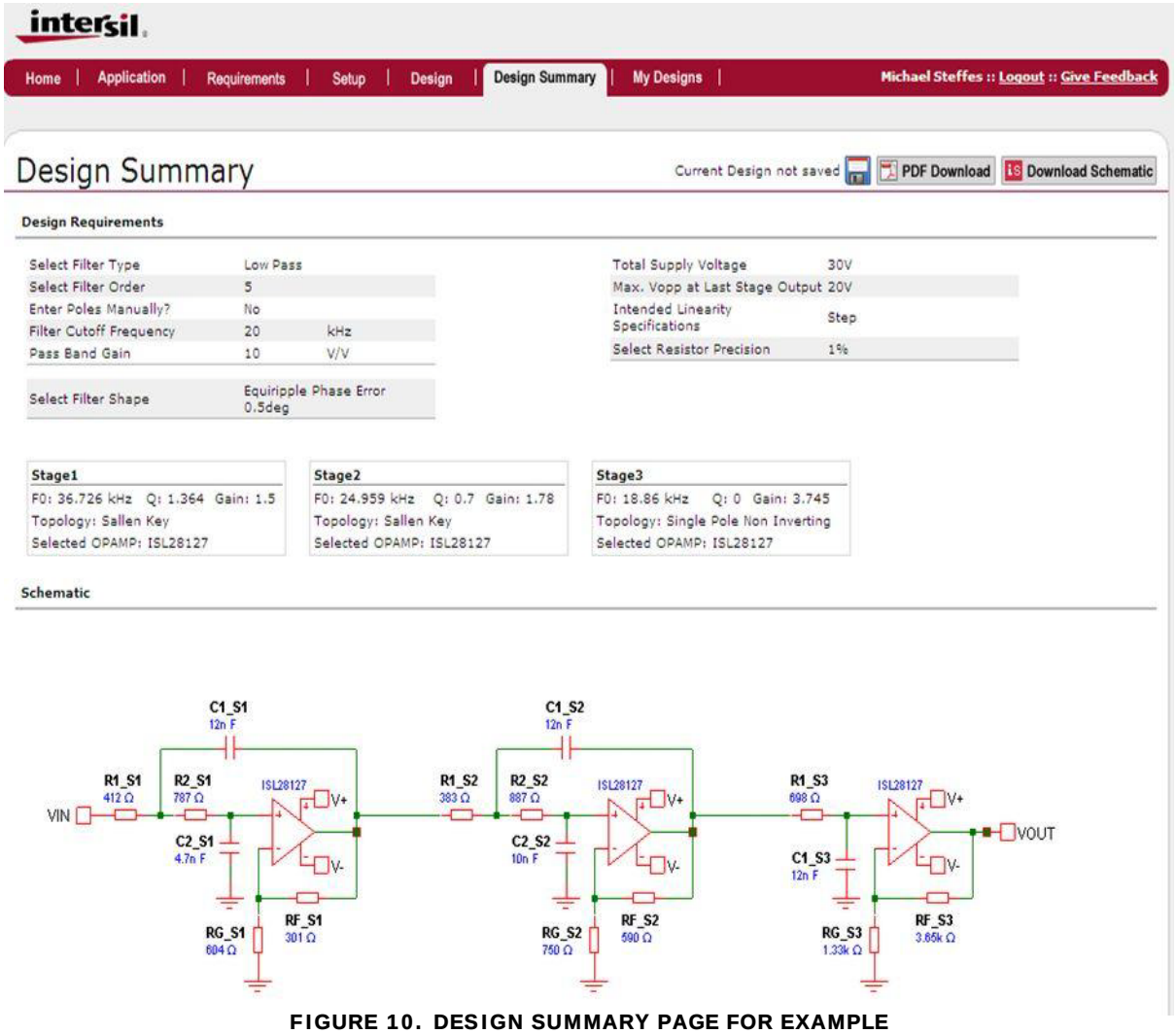


FIGURE 10. DESIGN SUMMARY PAGE FOR EXAMPLE

The next step is to summarize the design. Going to that tab across the top shows the screen displayed in Figure 10 where all of the simulation outputs are down below. That data is available to be downloaded to a PDF or saved to a local design file. It can also be ported to iSim PE for further design work.

The saving and sharing options are shown in the upper right corner of this screen.

Component Selection Comments

The end result for the active filter design tool is a combination of op amps, R's and C's that will give the desired filter shape. The iSim Active Filter Designer initiates the design offering only the simplest (single channel) versions of the available Intersil op amps. These devices span a wide range of speeds, technologies, supply voltage ranges, and topologies. Multi-channel devices, and versions offering shutdown, of these core devices are not explicitly included in the main design flow but are listed in the design summary page as implementation options for the designer. Since these other versions of a core single channel device share the same simulation macromodel, it would be redundant to include those in the filter design flow when they can be selected as implementation options once a design is completed.

For each stage, the tool will take the designer's desired filter requirement, supply voltage, output swing, a desired linearity target, and stage topology to direct the designer to devices that will best satisfy those targets and constraints. It will first eliminate from the option list those parts that cannot support the desired supply voltage and output swing or the required bandwidth and/or slew rate. It will then sort the remaining devices in approximate ascending order of design margin. The top few devices listed are typically well suited to the requirement for that stage while devices listed farther down either exceed the bandwidth or slew rate requirements of that stage or fall a bit short (within 10% though). The tool currently defaults to select the top device in each stage when it enters the Design tab. That device selection can be overridden in each stage using the added devices listed at the bottom of the page.

The target filter entries can easily exceed the capability of the amplifiers currently loaded into the tool. This will happen most commonly with Fo > 20Mhz, with high gain and/or high Q targets. The design flows are set up to pick amplifiers that will provide enough closed loop bandwidth margin to provide <±2% filter shape variation for approximately ±15% bandwidth variation in the amplifiers themselves. The tool is also checking slew rate requirements and margin in each stage so that high SFDR targets or high step amplitudes can be delivered without hitting slew rate related limitations. When the design flow fails to find any part that can meet the stage requirements, it will warn the designer at first a global level (one or more stages require performance not currently available) and then at a stage level. The designer is given the option to reset the requirements or continue the design with a manual selection from the available op amps. Continuing through to the manual selection first screens by supply voltage, then by topology (inverting stages can only use VFA op amps) and then lists in descending Bandwidth order the available amplifiers.

Once an implementation amplifier is selected for a stage, the R's and C's must be resolved. Presuming the goal for implementation is to derive a design that hits the intended filter shape over volume production and some ambient operating temperature range, the available types of capacitors that are suitable becomes constrained quickly. If those capacitors are further constrained to multi-layer ceramic SMD devices, the most suitable dielectric type for active filter designs appears to be C0G (sometimes called NPO) type capacitors. These offer the best available initial tolerances and tempco's for readily available, low cost, capacitors.

While these types of capacitors can be purchased over a wide range of initial tolerances, they appear to be only readily available in E24 (5%) value steps. Since the capacitors are so constrained in value resolution, the designs have been set up to select the capacitor values first using standard E24 values, then find the required resistors that will hit the target stage filter characteristics. The designs are normally delivered using exact capacitor values in these available E24 steps (at very low capacitor values <3pF, the tool switches to exact solved values). Capacitor and resistor tolerance issues can be assessed using MonteCarlo simulation techniques. This is supported in the iSim PE simulator tool for filter designs that have been ported into that tool as described in "Appendix 2" on page 37.

The available range of capacitor values in the design flow has been further constrained by practical considerations. Very low filter capacitor values (<10pF) run the risk of being dominated by amplifier input capacitance parasitics and/or board layout parasitics. The design equations attempt to include these parasitics but their accuracy is less well controlled than the filter capacitors. Each design implementation has a different low value limit depending on that topology, but they typically range from 2pF to 6pF for a minimum filter capacitor. When these limits are overridden, the tool switches to exact value capacitors in the design flow.

On the high end, the C0G type of SMD capacitor appears to be readily available up through the 12nF value. At higher values, they appear to become more of a special order device. All of the design flows currently limit the maximum implementation capacitor value to 12nF. However, the re-design step allows the designer to override the capacitor values selected in the design flow and re-execute the design to find the resistors using user specified capacitor values.

The design flows narrow in on a starting value for each capacitor first, then proceeds to resolve the required resistors. The tool allows the tolerance for those resistors to be selected as Exact, 0.5%, 1%, or 2%. This has the effect of snapping the implementation values to the available resistors for that tolerance. There is an initial error in the filter pole locations due to these discrete value steps that will be anticipated by this feature. Using the "Exact" option eliminates this error source while testing the design in the tool.

The range on the resistors is similarly limited due to parasitic considerations. On the low end, very low resistor values run the risk of loading prior stages or the amplifier used in that filter stage. Inverting designs limit the input R's to > 200Ω and non-inverting to >10Ω. On the high end, extremely high resistor values start to introduce parasitic poles due to their parasitic C that can interact with the desired filter shape. They also can cause slow initial turn on to correct operation and DC offsets in the operating point for the amplifier. The maximum R values used in the current design flows are limited to < 15MΩ. These can be effectively overridden using the re-design feature by scaling the capacitors down from the recommended values. The re-design feature of the tool accepts designer entry of the desired filter caps and does not constrain the resulting resistor values beyond snapping to standard values consistent with the selected resistor tolerance.

The tool concludes the design flow with capacitors chosen that are set to available E24 values and with resistors set to values available in their selected tolerance. The production variation in the filter shape can then be assessed through Monte Carlo simulation by applying the desired purchase tolerance to the nominal capacitor and resistor values chosen for the design. It is important to realize that while the capacitor values are set to 5% tolerance values, they can be purchased in those values to much tighter tolerance if desired.

Circuit Implementation Comments

The tool includes at least 4 possible op amp based circuits to implement the 2nd order and 1st order poles. To arrive at working active filter designs, from a frequency response standpoint, the tool constrains its

designs to bipolar supply, ground centered signal swing, implementations. The tool uses a specified total supply voltage to execute a design where that total is then split into ± halves to show an implementation. So, for instance, a 10V supply specification will be showing ±5V designs. This greatly simplifies the design flows to arrive at working R & C values for the filter without considering single supply issues. Once a design is proposed, it can be adapted to single supply and/or differential implementations through several techniques. Those are not currently supplied in this tool due to the wide range of possible approaches that interact with the specific filter delivered.

For instance, a low pass filter is by definition DC coupled. One easy way to translate a bipolar, low pass, design to single supply is to AC couple at the input and control a common mode operating point through each stage - but now the design is really a Bandpass design. That might be acceptable in some cases, but in others, alternate approaches that retain the signal path DC coupling might be required. This level of complexity is not supported in the current Active Filter Designer and it is left to the designer to adapt bipolar, single-ended, designs to either single supply and/or differential implementations. All of those techniques need to start with suitable R's and C's for the filter and those are the primary intended output of this tool.

Low Pass Filter Design Flow

Using the tool for low pass filter designs starts on the Requirements page. In all designs and design steps, the tool will start with default entries in the user entry cells that can then be overwritten by the designer. In Figure 11, the "Requirements" page will appear as it would when the designer first enters the filter design tool.

Here, the "Requirements" default to a low pass design, 4^{th} order, gain of 2, with a 50kHz cutoff using a Butterworth shape. Going in order down the page as follows:

- The filter type allows a Low Pass, High Pass, or BandPass filter to be chosen (Rev. 1, Low Pass only)
- Filter order can be from 2 to 6 – clicking the down arrow will show the choices.
- Pass Band Gain can be from 1 to 10 for the non-manual entry option (magnitude only, total gain through all stages)
- Enter Poles manually is clicked to "No" by default
- Select Filter Shape gives the pre-loaded options for that filter type.

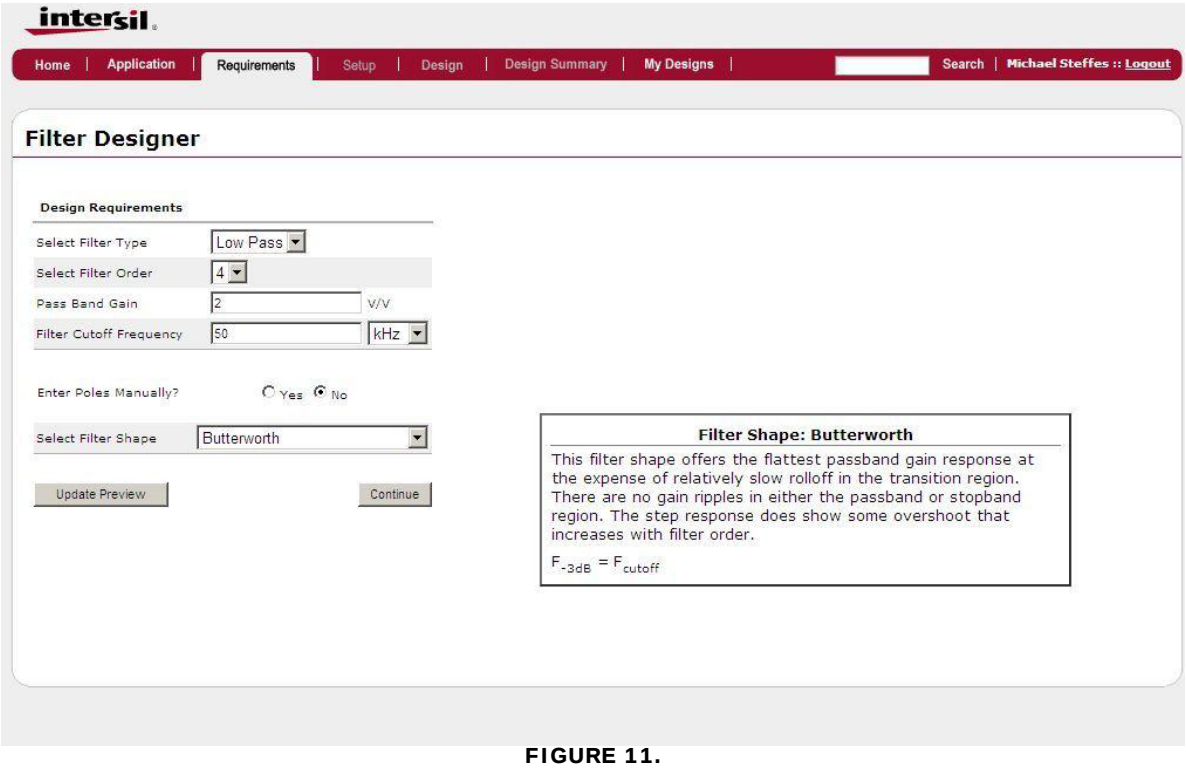


FIGURE 11.

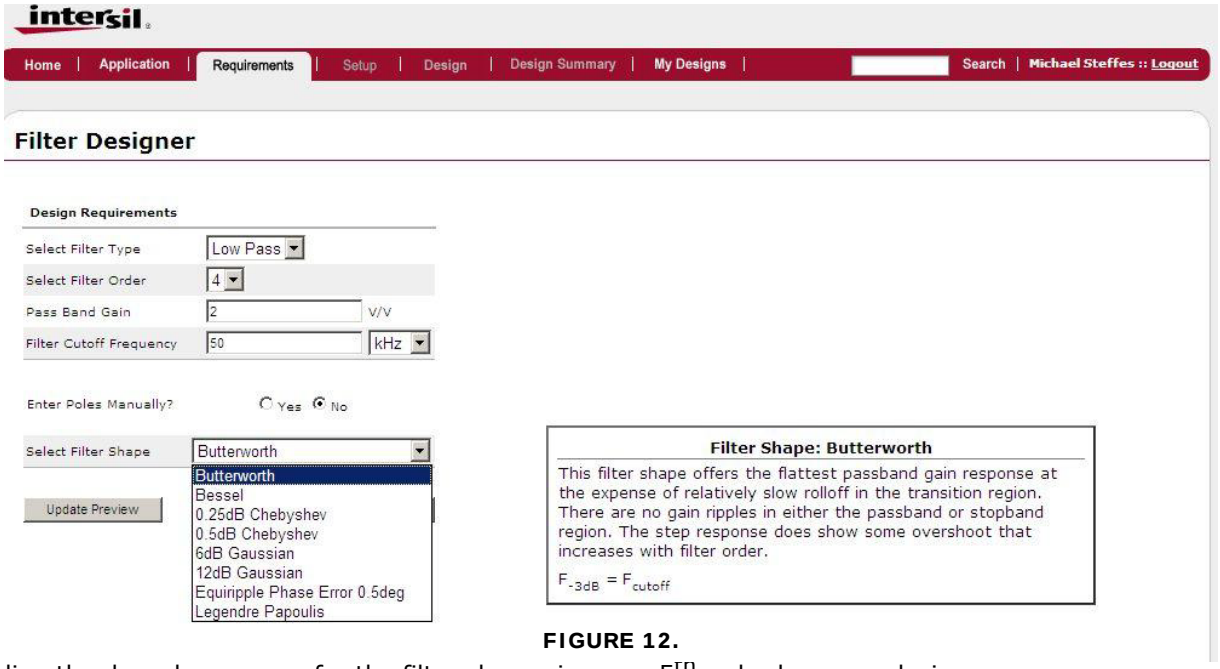


FIGURE 12.

Expanding the drop down menu for the filter shapes in the Low Pass type shows the choices displayed in Figure 12, which have been built into the tool.

The drop down shows the 8 possible standard low pass filter shapes available in the tool. Selecting any of these will also bring up a short description to the right and the relationship between the specified F_{cutoff} and F_{-3dB} for that filter shape. Normally, they are equal but that is not the case for the Chebyshev filters.

Once a filter shape is chosen, a preview of the AC response is available by hitting the "Update Preview" key. Figure 13 illustrates a specific filter that has an approximately constant group delay. Here the targets have been changed to a:

- 5^{th} order low pass design
- Pass Band gain of 10V/V (20dB)
- 200kHz Fcutoff
- Equiripple Phase Error 0.5°

This data from the AC preview plots are also be used to compare to the AC simulation output for the design implementation delivered by the tool. This gives the ability to compare actual to ideal in the plot output pages.

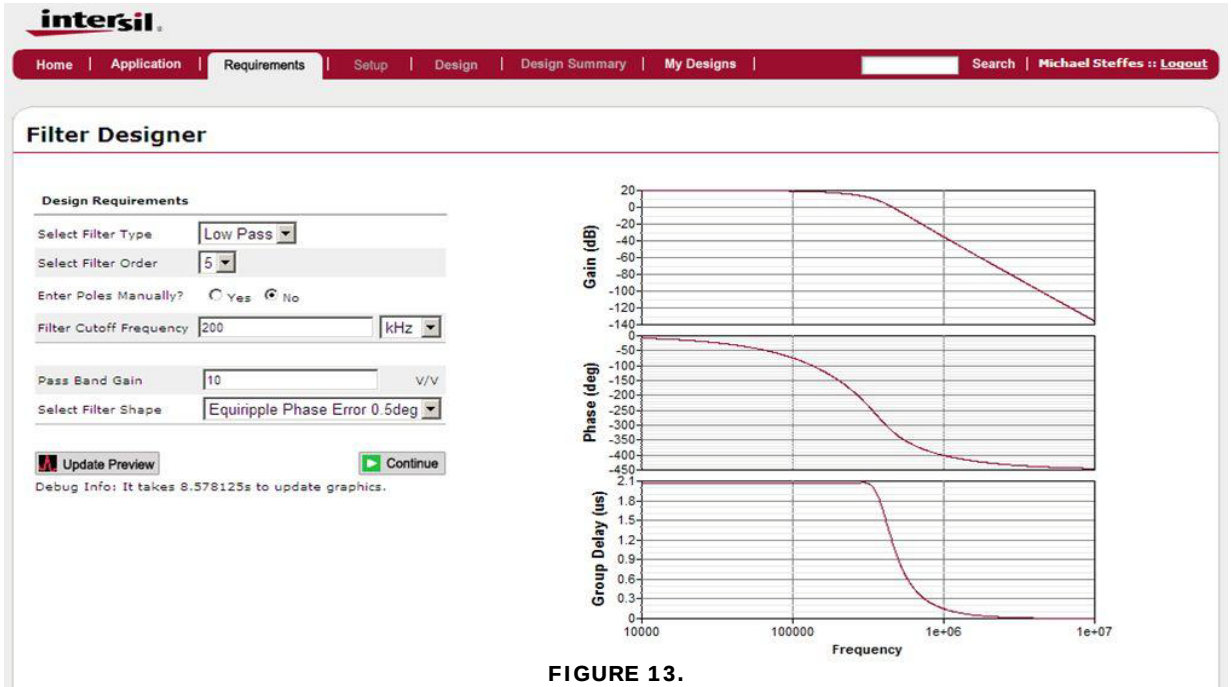


FIGURE 13.

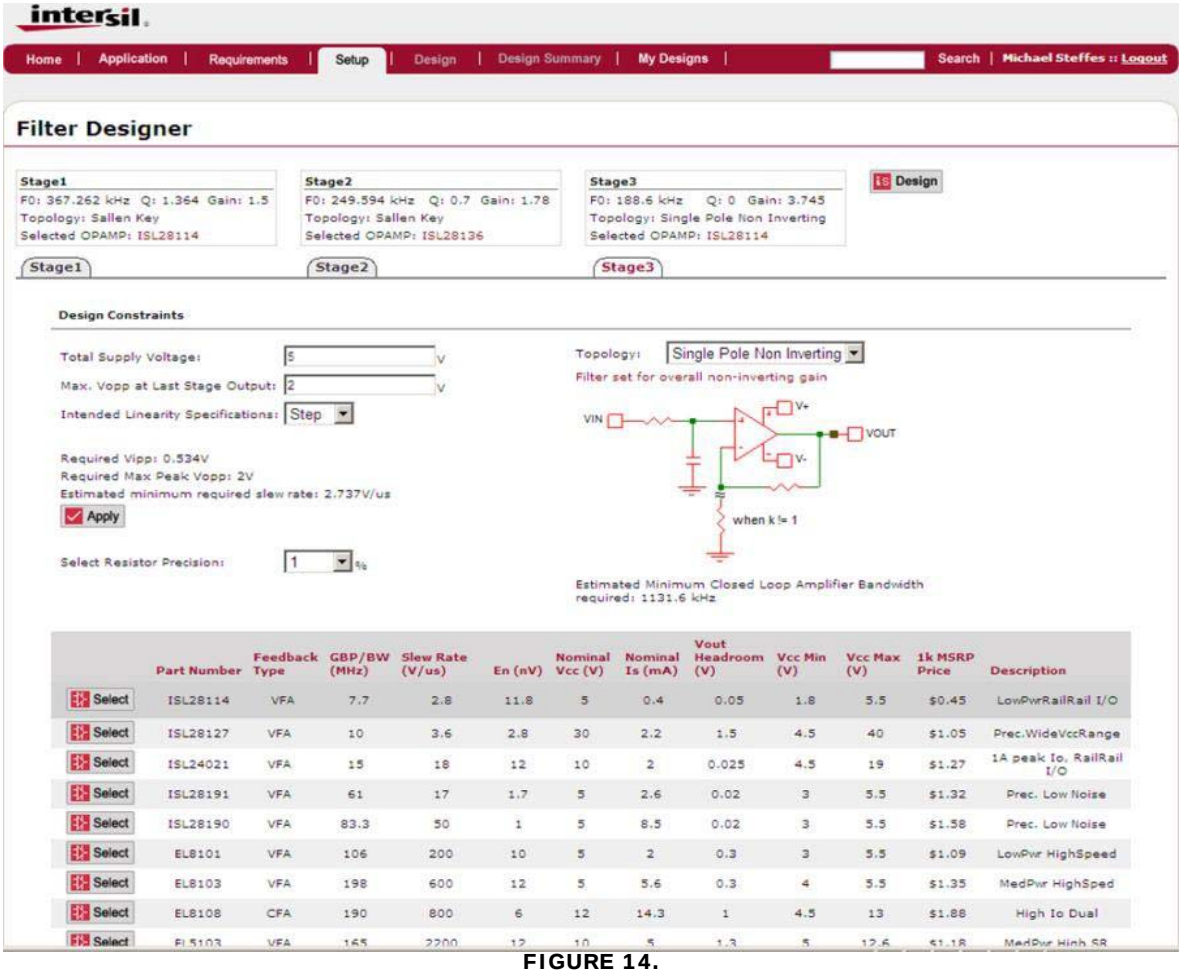


FIGURE 14.

Once a desired target design is set up in the "Requirements" tab, hitting "Continue" will go the next "Setup" step. Here the design is broken into the required number of stages, the target Fo, Q and Kn (gain) is assigned to each stage and is reported across the top, the default design constraints are assigned, and the available amplifiers assessed for application to each stage. Hitting "Continue" on the design example shown in Figure 13 will display the screen shown in Figure 14 (note – as devices are added to the tool, the part list at the bottom and devices selected might change from this example).

Here the design has proceeded to a solution using several default assumptions. It also always starts with the last stage "active". This can be noted by the red color of "Stage3" shown in Figure 14 – clicking on the "Stage1" or "Stage2" tabs will allow you to select amplifiers or topology for those stages. **However, the Design Constraints listed to the left can only be updated when sitting on the last stage screen.**

The initial constraints (and their allowed range) are as follows:

1. Total supply voltage is 5V (range is 1.8V to 40V)
2. Desired final output swing is $2V_{P-P}$ (allowed range is between 10% and 90% of the supply voltage)
3. Principally interested in a good Step response (this is chosen depending on filter shape to be either a step or SFDR oriented linearity specification). Can be toggled with drop down arrow – this sets the design margin for the slew rate.
4. 1% resistor tolerances (drop down allows exact, 0.5%, 1% or 2% to be chosen)
5. All stages are non-inverting.

All of these can be changed. The design constraints are global to the design and can only be changed when the active stage is the last stage. Here, since this is a 5^{th} order design, we have 3 stages and the last stage is a non-inverting buffered real pole. The active stage is identified by which of the Stage tabs are in red. A real pole has the option of being an active inverting stage and changing that using the drop down list above the schematic will immediately recalculate the limits implied in this stage.

Clicking a tab for an earlier, 2^{nd} order stage, allows the option to change that stage to an inverting MFB topology. The MFB has several pros and cons from an implementation standpoint. One disadvantage might be that only VFA op amps can be used (becomes limiting when very high GBP is required), but a pro is

that they offer much better stop band rejection than the Sallen-Key implementation.

Updating new constraint entries by hitting the "Apply" key will recalculate the signal requirements in each stage. The stage targets are listed across the top where here we see the lower gain, high Q stage, coming first and the real pole last. The gains have been spread through the stages in ascending order left to right. Those cannot be changed except by going back into the "Requirements" tab and resetting the target filter gain.

For each stage, the desired filter target, implementation circuit, and the global constraints are used to calculate limits on the amplifier specifications. The results of these calculations are shown as each stage tab is selected. For the last stage above (Stage3), the tool is estimating the following limits:

1. Closed loop BW ≥1131kHz. Since the non-inverting stages can be implemented with either Voltage Feedback Amplifiers (VFA) or Current Feedback Amplifiers (CFA) the closed loop bandwidth is reported here. Here, a VFA has been chosen so the required Gain Bandwidth Product (GBP) is the gain of this stage times this closed loop bandwidth, or 3.745*1.131Mhz = 4.24Mhz gain bandwidth product. The part that has been selected, the ISL28114 has 7.7Mhz GBP so it satisfies this constraint.
2. The maximum required output V_{P-P} can be set by the designer but defaults to $2V_{P-P}$ when first entering this step. With a step response as the desired linearity specification, the tool calculates a peak dV/dt for this stage then targets a 2X minimum slew rate to that requirement in setting this constraint. Here, that is showing an estimated minimum slew rate of 2.74V/µs which is again within the 32.8V/µs capability of the ISL28114 chosen for this stage.
3. The required maximum V_{OPP} is adjusted from the nominal number to include overshoot or peaking produced by this stage. The max. V_{OPP} is just the $2V_{P-P}$ for this real pole stage since there is no overshoot produced in this stage. This number is then compared to the supply voltage minus 2* the amplifier's headroom specification. Here the ISL28127 has a 5V – 2*.05V = 4.9V which is plenty of design margin for this stage.
4. The maximum input V_{P-P} is calculated as the nominal (unpeaked) output V_{OPP} divided by the stage gain. That is compared to the supply voltage minus 2*the input headroom specification for non-inverting stages. That data is not shown in the listed parameters for the table of candidate parts, but is used to constrain parts that might hit an input range limit.
5. For multi-stage designs, this computed input V_{IPP} becomes the nominal V_{OPP} for the prior stage and the calculations are repeated for that stage. Switching to that stage's amplifier selection will show those targets and the recommended amplifier solutions.

At any point, selecting a different op amp from the list at the bottom will update the selected amplifier for that stage. The possible amplifiers a listed in approximate ascending order of design margin. The one at the top (ISL28114 for the last stage) offers the minimal design margin, while the EL5103 would have far greater GBP and Slew rate than required for this stage.

An easy way to see a different set of amplifiers is to change the intended total supply voltage for the design. Going to the last stage and changing the total supply to 10V and hitting update, will list all the parts that will work up to 10V. Going to 30V for the total supply will reduce the list as there are fewer parts at that supply voltage and speed.

When the Setup page has an amplifier selected for each stage (part number shown in red in each of the requirements boxes at the top), hitting the "Design" key will execute the proposed solution for the R's and C's. Doing that for the design example shown in Figure 14 will give the results shown in Figure 15.

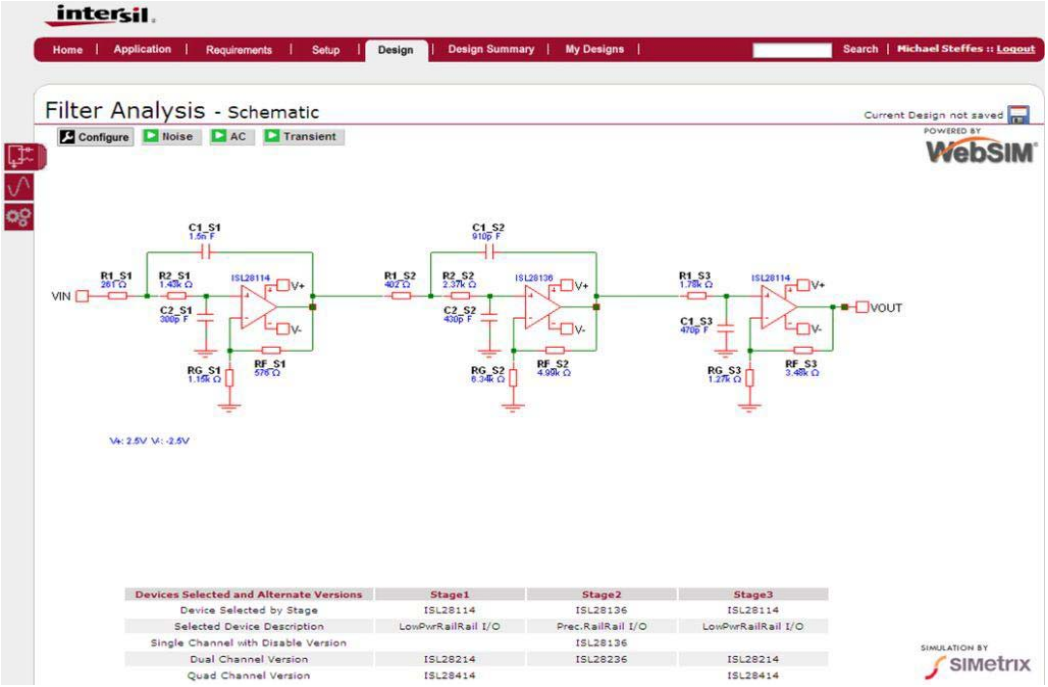


FIGURE 15.

The proposed design is shown in the schematic. The bipolar supplies used in setting up the design are shown in the lower left. The selected and related parts for each stage are shown across the bottom while the green simulation options at the top are used to select which simulation to perform.

The "Configure" button allows you to change the default conditions for each simulation (frequency range and max. time in a transient). The 3 red tabs in the upper left select what is displayed in this step. The top is the current circuit and what is shown here. The middle is the simulation results generated thus far and the bottom takes the designer to a re-design page.

The design algorithms have attempted to deliver a design that will achieve the desired frequency response and signal gain while considered the following 2nd order effects:

1. Constrain the resistors to limit their noise contribution vs. the op amp noise terms. This does not necessarily mean that this is the lowest noise solution, just that the resistor noise does not impact the total output noise of the op amp stage too much (<12% increase in V/√Hz). The noise plot will therefore be showing principally the noise generated by the op amps selected. If that is too high, select lower noise op amps for the filter design (like the ISL28190 and ISL28191).
2. Choose capacitor values that are standard E24 steps and within the range discussed previously.
3. Constrain the resistors to limit their loading on the amplifier given the required output swing in each stage. This is a stage specific calculation and only a global constraint (a rough estimate) on input R's are included to limit loading on the prior stage.
4. Constrain the filter R and C ratios to reduce the in band noise gain peaking typical of 2nd order active filter designs.
5. Include several op amp parasitic effects in the design for the R & C values – these are:
    a. Input capacitance for the op amp selected
    b. Finite bandwidth effects for the op amp – this is used to slightly adjust the R values from those that an ideal op amp design would predict. Hence, putting these design output R's and C's into ideal active filter equations might appear to be giving results that are slightly off target – these are the adjustments to include the op amp bandwidth. These are often very minor if the amplifier bandwidth far exceeds the requirement for that stage but become very obvious if the design has passed through the warning that no parts are fast enough for the stage targets. In that case, the algorithms will be making large adjustments from the ideal R values to account for op amp bandwidth effects.
    c. Optimize CFA based designs for best achievable bandwidth by adjusting the feedback resistor value.
    d. Limit the loss in phase margin for VFA designs due to feedback network impedance to the inverting parasitic input capacitance
    e. Set the feedback R in non-inverting stages to get input bias current cancellation for VFA op amps that offer a low input offset current (when this does not violate some other consideration).

It is these considerations that have delivered the design shown in Figure 15 that uses midrange resistor values in the design. Since the ISL28114 is a moderate noise

device, at 11.8nV/√Hz input referred voltage noise, the filter resistors end up in the kΩ region. However, its feedback and gain resistor networks have not been set up for bias current cancellation as this device does not offer a lower offset current vs. it's input bias current. The design for the middle stage using the ISL28137 have set the Rf and Rg resistors to hit the gain and achieve bias current cancellation since that part does have a lower Ios than the Ib terms. Hence, Rf||Rg = R1 + R2 in that stage.

From this initial design output page, numerous options are possible to the designer. Hitting any of the simulation options at the top will deliver those simulations for the total filter and each of the inter-stage outputs for multistage designs. The other option offered at any time on this design page is to save the design by clicking the Save icon in the upper right corner. The tool will then ask for a design name and comments to save the design.

Hitting "AC Analysis" for instance will generate a wait indicator then return with the screen displayed in Figure 16.

Here, all of the AC analysis outputs are presented. Note that the middle red tab on the upper left is now highlighted indicating you are in the results page for this design. Each plot shows the gain, phase and group delay first for the first stage output (S1), then the second stage output (S2), then the filter AC output (last stage) and then all outputs. Clicking on any of these plots will open a waveform viewer that offers additional options for zooming and placing the ideal response on the final output responses. This ideal response is only available for the Filter AC Output or the All AC Outputs plots. Selecting the Filter AC Output and clicking on the Ideal gain phase and group delay choices in the upper right, will display the screen shown in Figure 17.

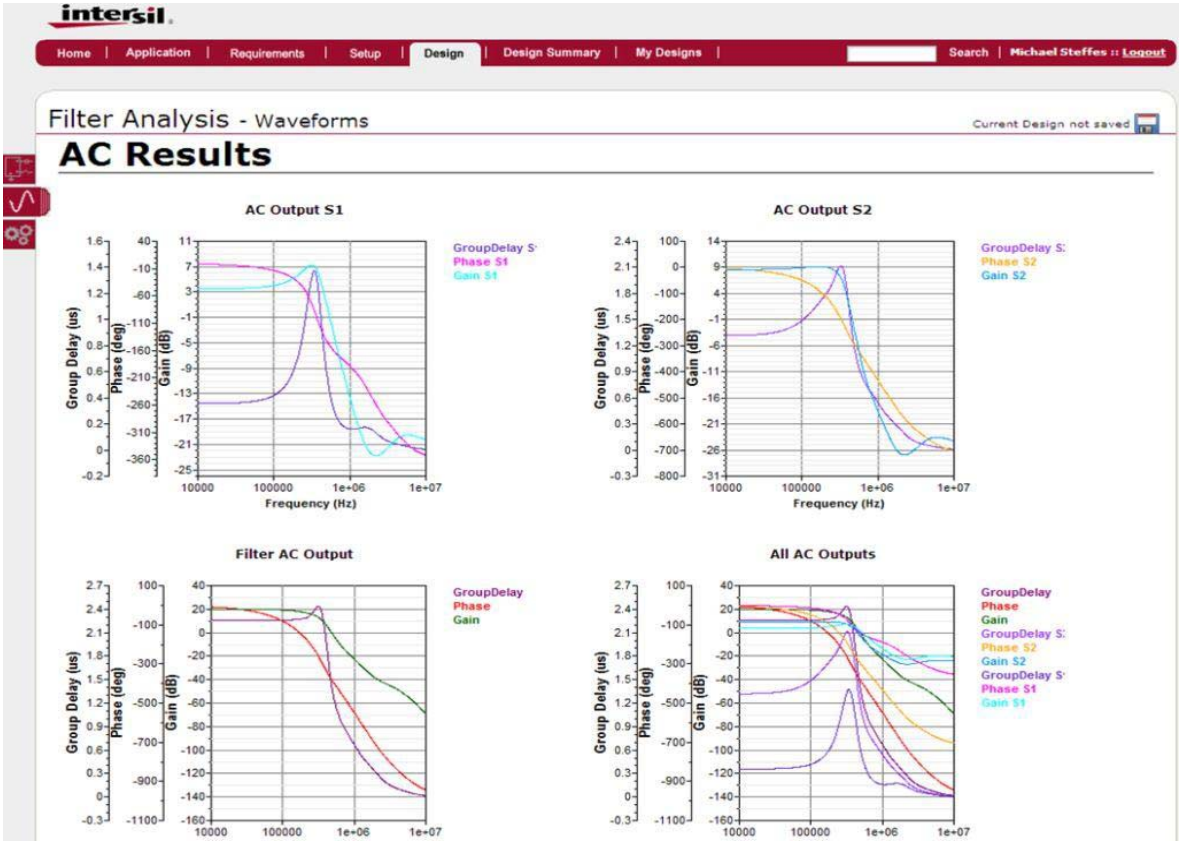


FIGURE 16.

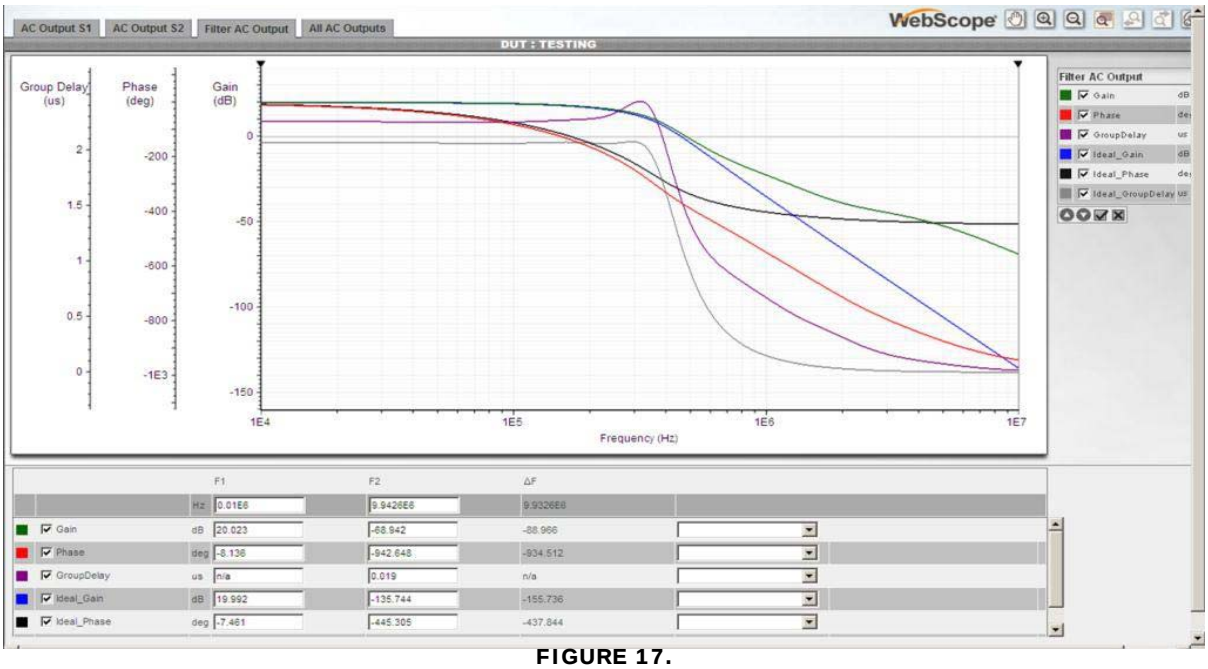


FIGURE 17.

Here we are seeing reasonable gain fit through about 500kHz then some deviation from ideal. Using faster devices (such as the ISL28191 in this case) will improve the fit on all filters at f > Fcutoff. The group delay plot is always higher then the ideal plot since it includes the propagation delay of the actual amplifiers (maroon vs. gray plot).

The WebScope tool allows the designer to zoom in on areas of the response by moving the mouse over the curves and creating a zoom box. Doing that in the 200kHz F_{-3dB} region shows how well the proposed design matches the Ideal output in the F_{-3dB} region. Here, one of the two cursors has also been moved to 200kHz to report that actual output for each of the plotted curves. This plot is also showing the actual vs. ideal phase and group delay. Here the cursor labeled F2 (the little black arrow at the top which you can move by clicking and dragging) is set at 200kHz where it shows the actual gain is 17.274dB vs. the ideal gain of 16.996dB. Re-running this design using ISL28191 shows an improved fit (try it).

FIGURE 18.

These outputs are in a new window vs. the Design outputs window. Going back to that window and clicking circuit tab (top on the left side red tabs) and then clicking the noise analysis option gives the simulated spot noise at each output stage in the design while clicking the Transient Analysis gives the step response at each output stage in the design. Doing that gives the two output plots shown in Figures 19 and 20 for this example design.

The noise plot (Figure 19) is showing the noise at each output. The first stage is relatively low noise but with the peaking intrinsic to a higher Q target in that stage. The output of the 2nd stage includes this plus the noise contribution and gain of that stage and is less peaked, while the final stage adds most of the gain to the low frequency spot noise but rolls off the peaking quite a bit as it is a single pole low pass stage. The output noise in this simulation turns up at higher frequencies as the individual stage amplifiers rolloff only slightly above the desired filter frequency. Following the last stage with a simple RC well above the desired filter shape (1Mhz for instance) can control this out of band noise, or using faster parts in the design will show a much more attenuated output noise at high frequencies (again, try this design with the ISL28191 which is also a much lower noise device).

The transient response defaults to a trapezoidal input stimulus that hits the desired V_{OPP} as a bipolar swing at the final output. The time scale is chosen to give one full cycle of what should be a fully settled step response for most filter shapes. If that is too long or too short a time, it can be re-set using the wrench key on the design output page. The plots displayed in Figure 20 show the higher overshoot in the earlier stages, then the almost zero overshoot at the final output typical of an equiripple phase filter design.

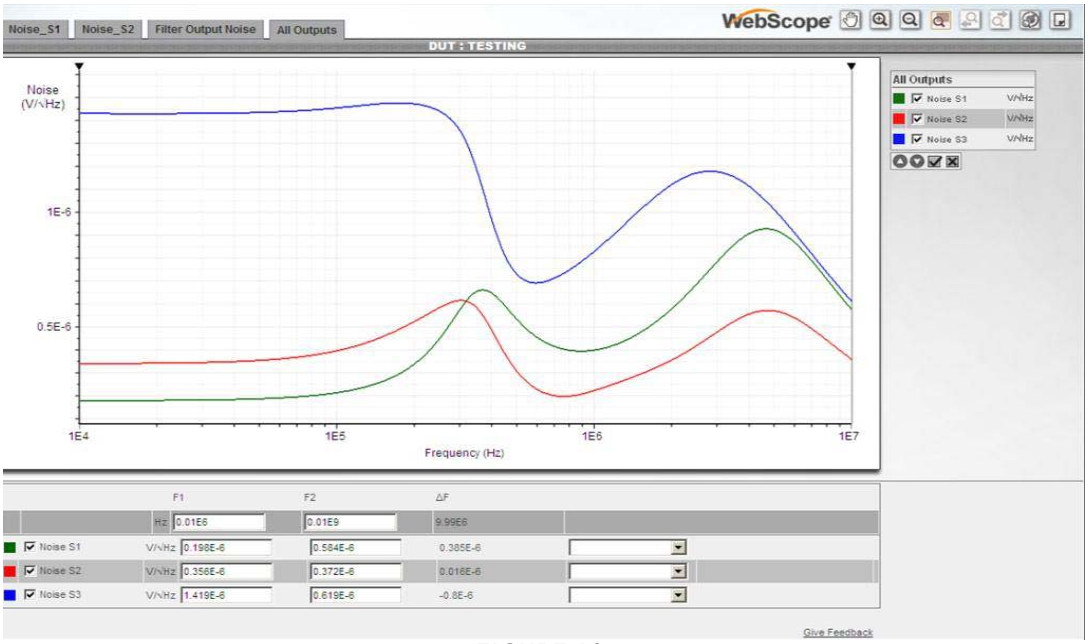


FIGURE 19.

FIGURE 20.

Re-design Options

Sitting on the Design page with a completed schematic offers several simple redesign options. The amplifier(s) used cannot be changed here, but on the setup page they can be from the available list of parts.

Highlighting any R or C using the cursor can be used to change just that passive component value if needed. Left clicking the cursor on a resistor or capacitor will open a window to allow that element value to be changed. Note that this can easily move the design point for that stage well away from the intended filter characteristic for that stage, so the new simulations results (hitting any of the response keys at the top) might change the response quite a bit. However, if a designer has an existing design using the Intersil devices selected, this might be an easy way to get the expected response for that design. Or if the feedback and gain resistors in non-inverting designs seem non-ideal, this is an easy place to override those selections while holding the same ratio.

A more sophisticated re-design option is provided using the lowest of the 3 option tabs on the upper left of the design output window. Hitting this opens up a new window where the capacitor values may be manually set (with no range or standard value constraints) then the design algorithms re-run to find the necessary resistors to hit the same stage filter designs using these new capacitor values. This proceeds in several steps, as shown in the following.

In the screen shown in Figure 21, windows are opened under each stage to allow manual entry of the capacitor values for that stage. Under each 2nd order stage is a limit equation and calculation for the allowed C1/C2 ratio to get a valid solution given the desired Q and Kn (Gain for stage n).

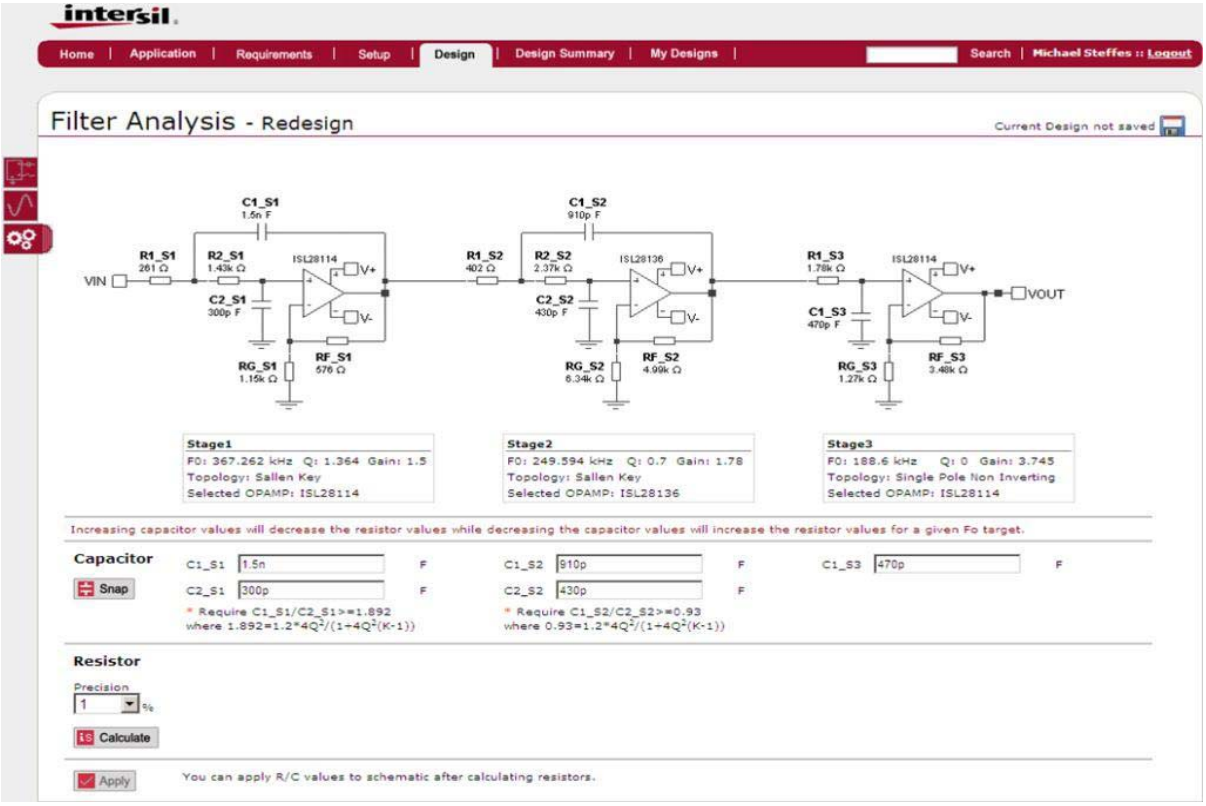


FIGURE 21.

For example, Figure 22 shows all of the capacitors scaled up, which will reduce the resistor values. Hitting the Snap button will take your capacitor entries to standard E24 (5%) steps but is optional. Then hitting calculate, gives the preview shown below of the new resistor values. Then hitting the apply key will update the simulation schematic to allow the performance sims to be re-run with the new values.

As you can see in Figure 22, all the proposed new resistor values are lower than the original circuit. This should reduce the noise a bit, but the original circuit was designed to limit the noise impact due to the resistors already. These lower values might also expose loading limited bandwidth issues in the selected op amps (the simulation models attempt to include loading effects in the BW response).

Hitting "Apply" in this screen will update the schematic to the new values (try it).

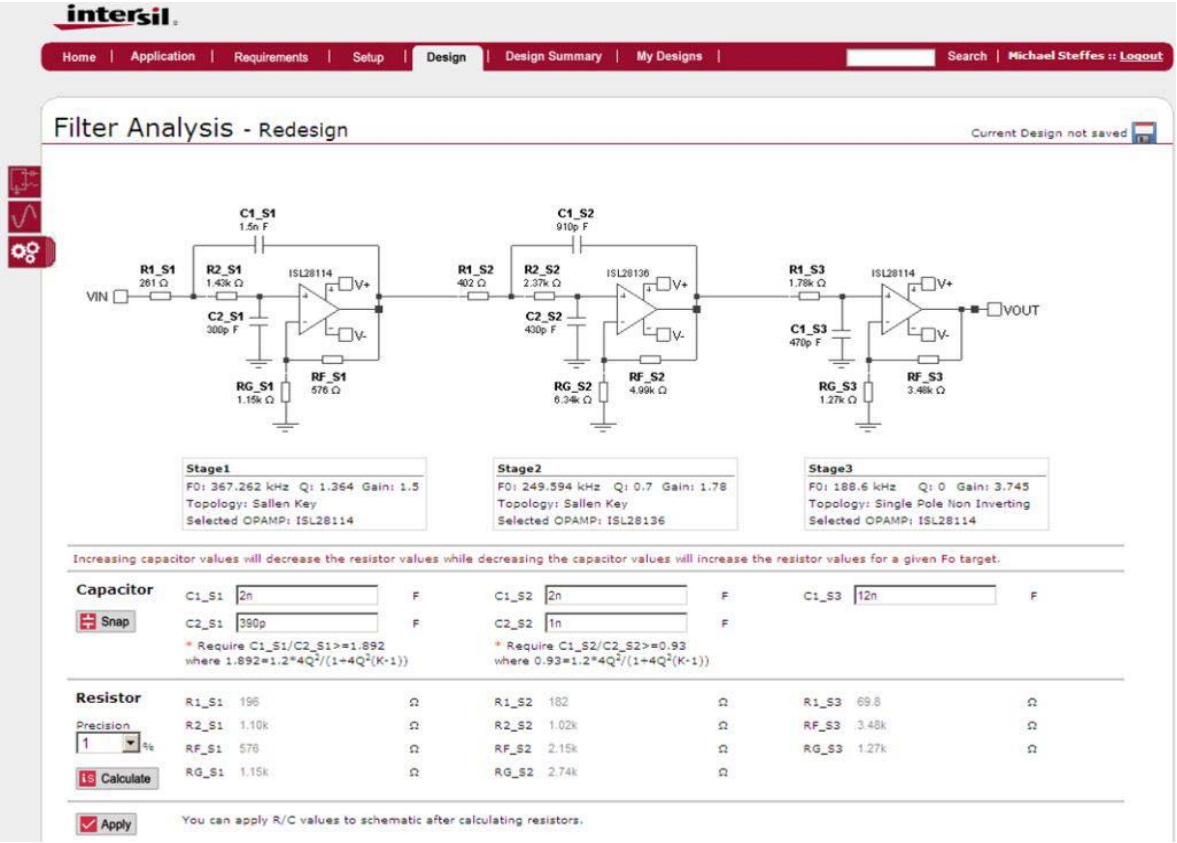


FIGURE 22.

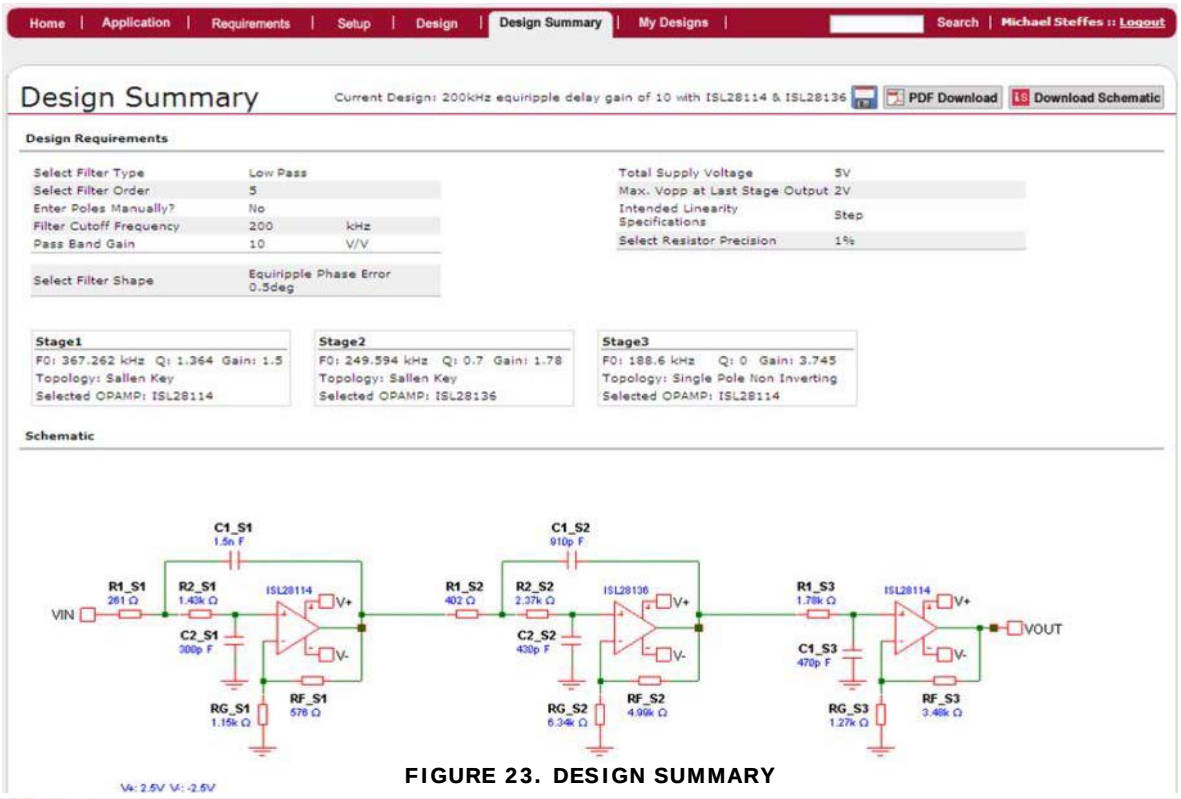


FIGURE 23. DESIGN SUMMARY

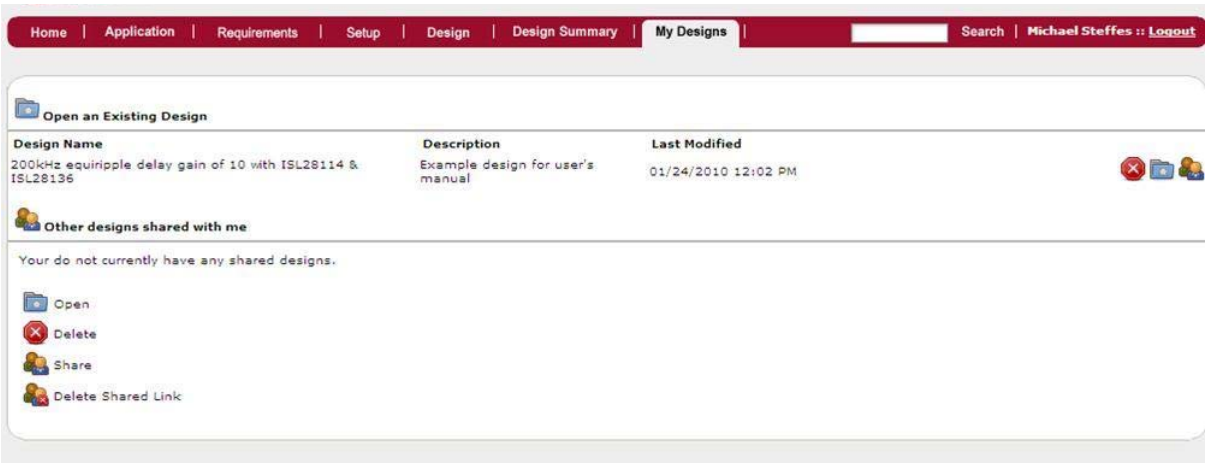


FIGURE 24. SAVED DESIGNS

Design Summary, Sharing & Porting to iSim PE

Once the design is done and the simulations generated, the next step in the design flow is the design summary page. This shows the targets, implementation, and simulation outputs for the design to this point. The screen shot in Figure 23 shows the top portion of this page with the list of component values and simulation results down below.

This is showing the top portion of that screen where it has now been saved locally using the little floppy disk tab at the top as "200kHz equiripple delay gain of 10 using ISL28114 & ISL28136".

The other options here are to download the design summary as a PDF to easily share the results in Email or to download the schematic to the iSim PE simulator tool using the "Download Schematic" button.

Once the design is saved inside the Active Filter Designer, it can be brought up for further work later on and shared with other colleagues. Going to the MyDesigns tab will show your saved designs and offer several options on those designs. Doing that here gives the page shown in Figure 24. The most recent design is at the top (the one being used here). The 3 options at the right provide a delete, open, or share function. Opening the share icon on a row gives a place to enter another iSim Active Filter Designer email address. Typing in the address and hitting send, will allow another user to open up and start using/editing the design locally in their workspace.

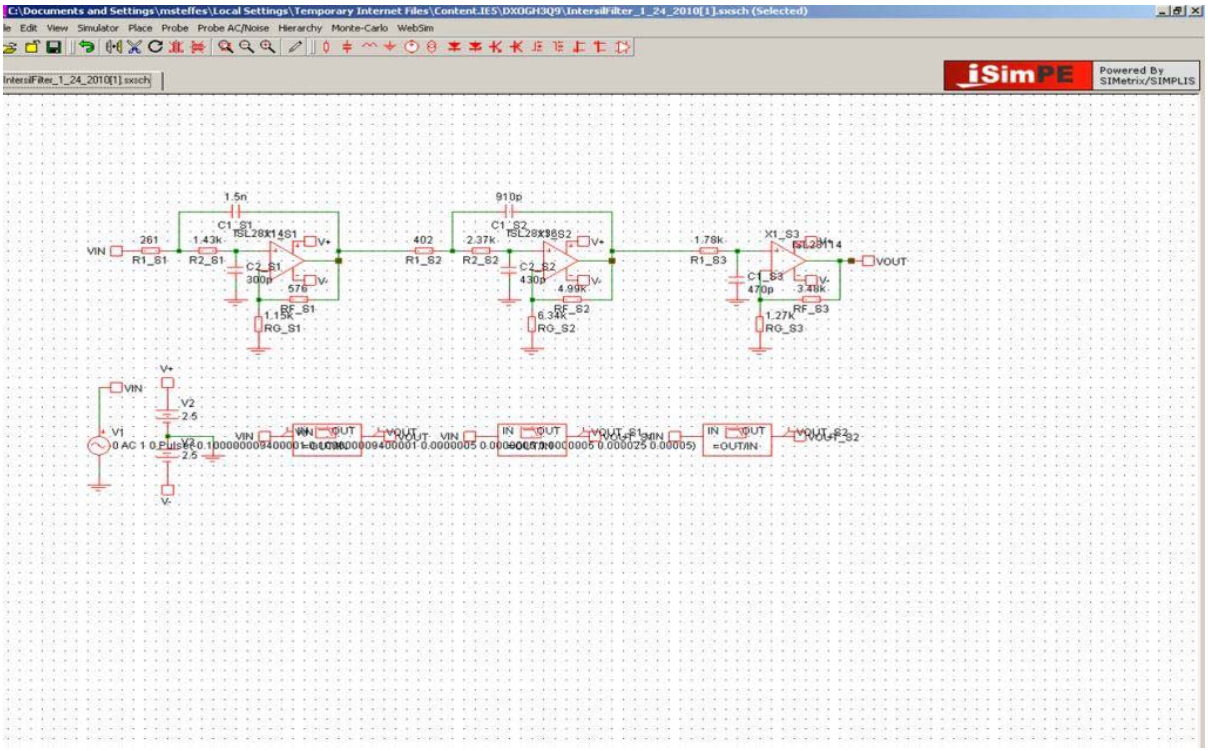


FIGURE 25.

Hitting the "Download Schematic" button in the Design Summary page will display the screen shown in Figure 25 (if iSim PE has been loaded locally onto your computer).

Taking the schematic into the iSim PE tool then allows all the usual Pspice operations to be performed. It is here that you can do a Monte-Carlo simulation putting a tolerance on the resistors and capacitors, or interchange the order of the stages. You can also edit the component values and change the design to single supply in the desired fashion.

Manual Pole Entry

Going back to the "Requirements" tab and clicking Yes on the "Enter Poles Manually" line changes this screen to that shown in Figure 26. Here, it is still set for a 5th order filter and it retained the 200kHz Fcutoff. In this mode the Filter Cutoff frequency is only used to set the frequency response plotting range. The specified frequency will appear in the left 3rd of the AC and Noise output plots. So this needs to be manually updated to be consistent with the region of interest for the poles to be entered (this field in not updated by pole entries shown in Figure 26).

The Pass Band Gain is now calculated from the entries in the stage lines listed in Figure 26. These start out as a default 1 magnitude (can change any stage to inverting in the Setup section).

This mode is looking for the gain for each stage and either the real/imaginary pole locations or the Fo and Q values for each stage (a real pole is Q = 0 and Fo = F_{-3dB} for that stage). The default is Fo & Q while hitting the drop down key will give you the Complex (Real and Imaginary) option as shown in Figure 26.

The poles are entered in un-normalized format. The frequency limits are expanded here to be 5Hz to 50Mhz for Fo. Entering frequencies > 20Mhz with high gains and/or Q's can ask for op amp speeds not available. That will be flagged in the next "Setup" step if that is the case. The setup page will still calculate the required op amp bandwidth for each stage where it will be easy to see if the target requirements are asking for excessive op amp bandwidths.

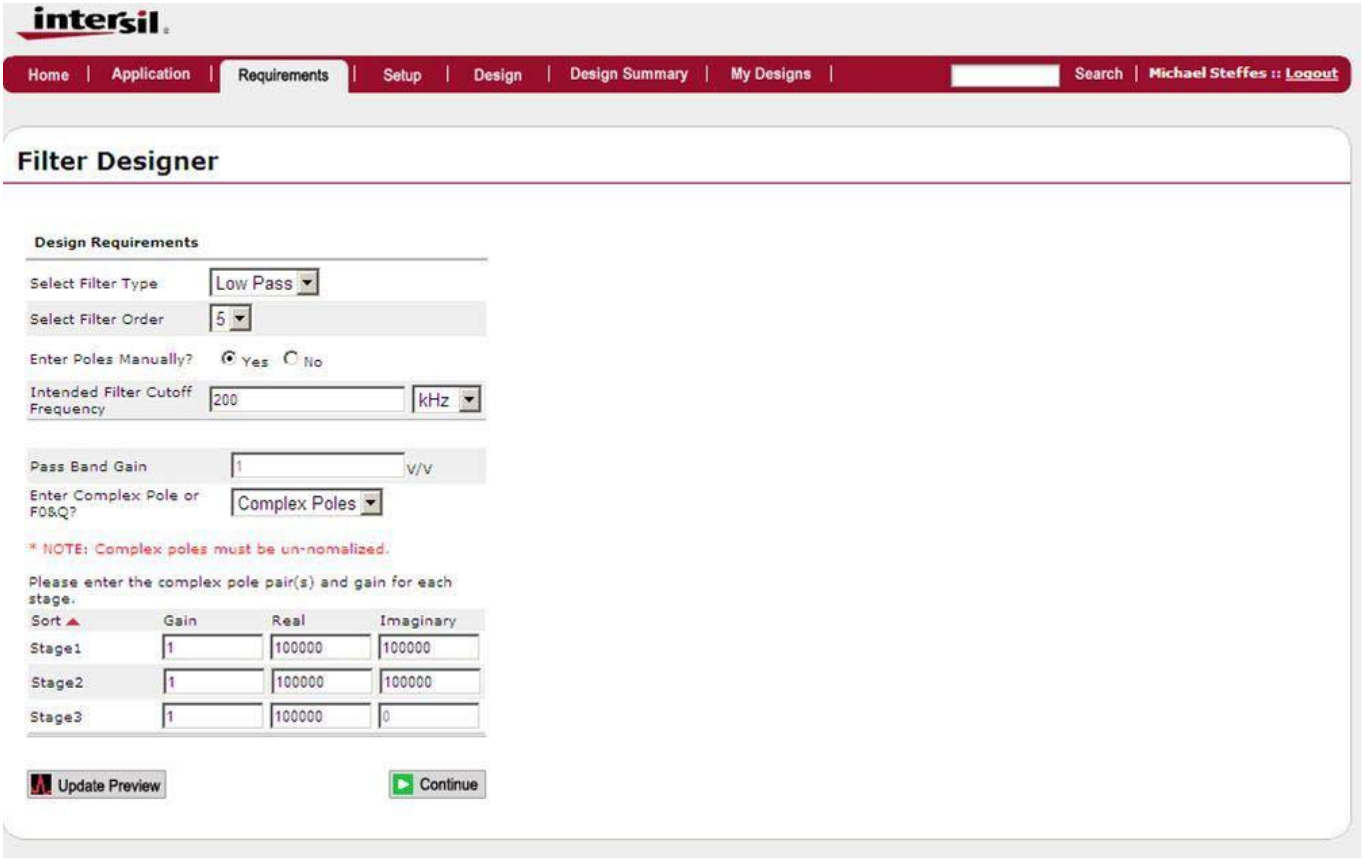


FIGURE 26.

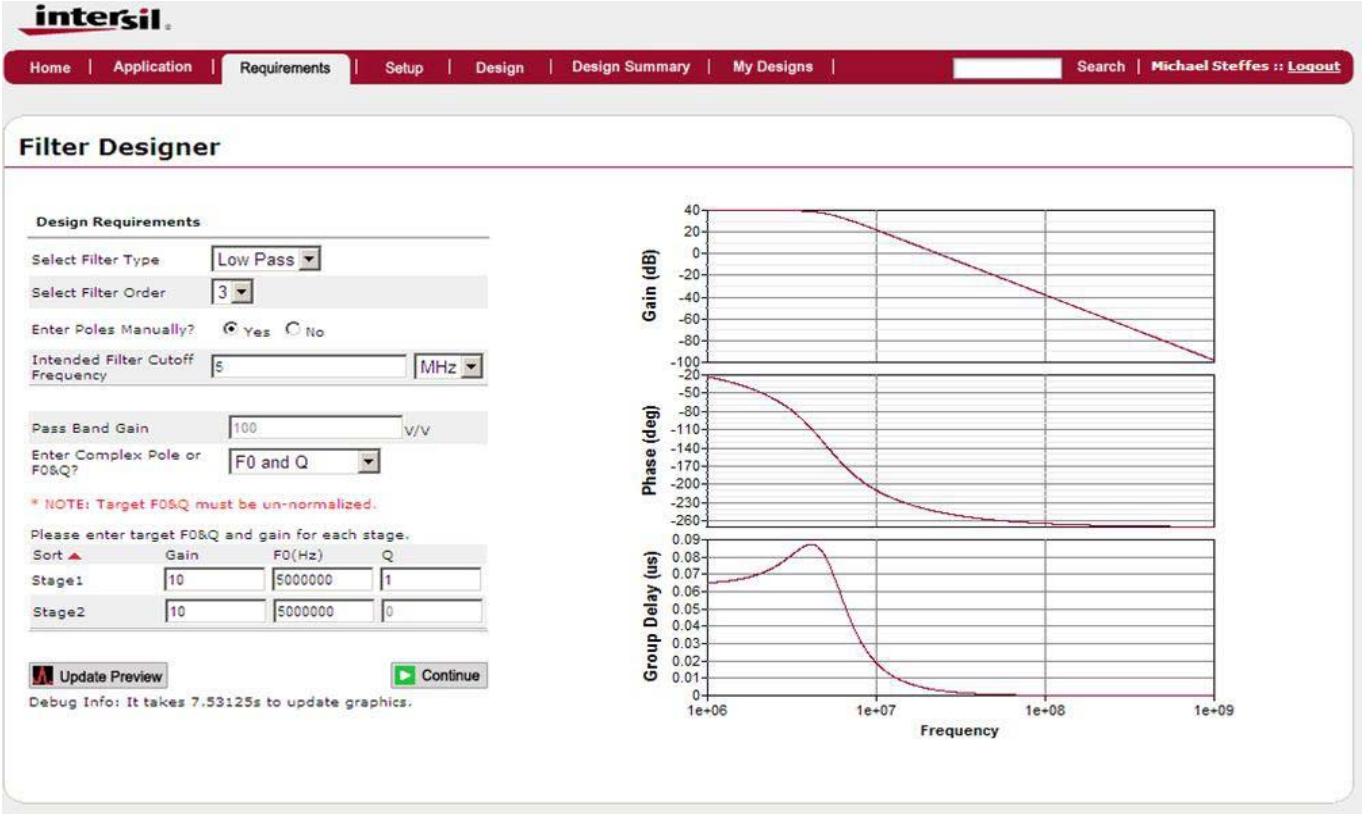


FIGURE 27.

Changing to a 3rd order design in Fo and Q format and targeting a 3rd order Butterworth gives the screen displayed in Figure 27. Here we have also set each stage up for a gain of 10 getting a total filter gain of 100 and hit the "Update Preview" key.

Now, hitting continue and changing the total supply to 10V with a 6V step output in the final stage will give the screen displayed in Figure 28 – where this has been left on the first stage requirements showing the fastest CFA has been selected for implementation.

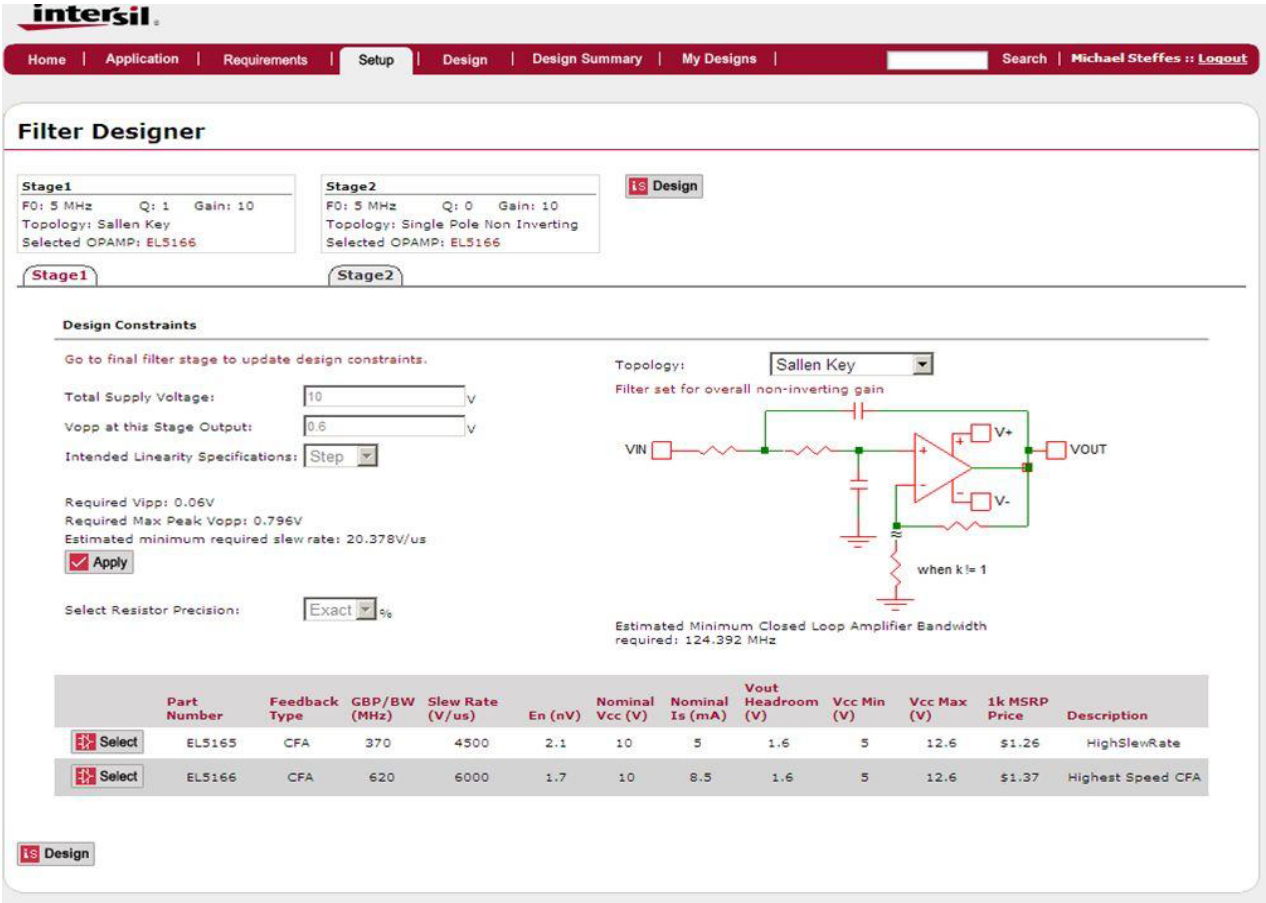


FIGURE 28.

Then hitting the design key will give a proposed design and then hitting the Transient key will get the resulting step response. Note the input is only ±60mV to get this ±6V output. Also, the overshoot and ringing is typical of the Butterworth filter used as an example in Figure 29.

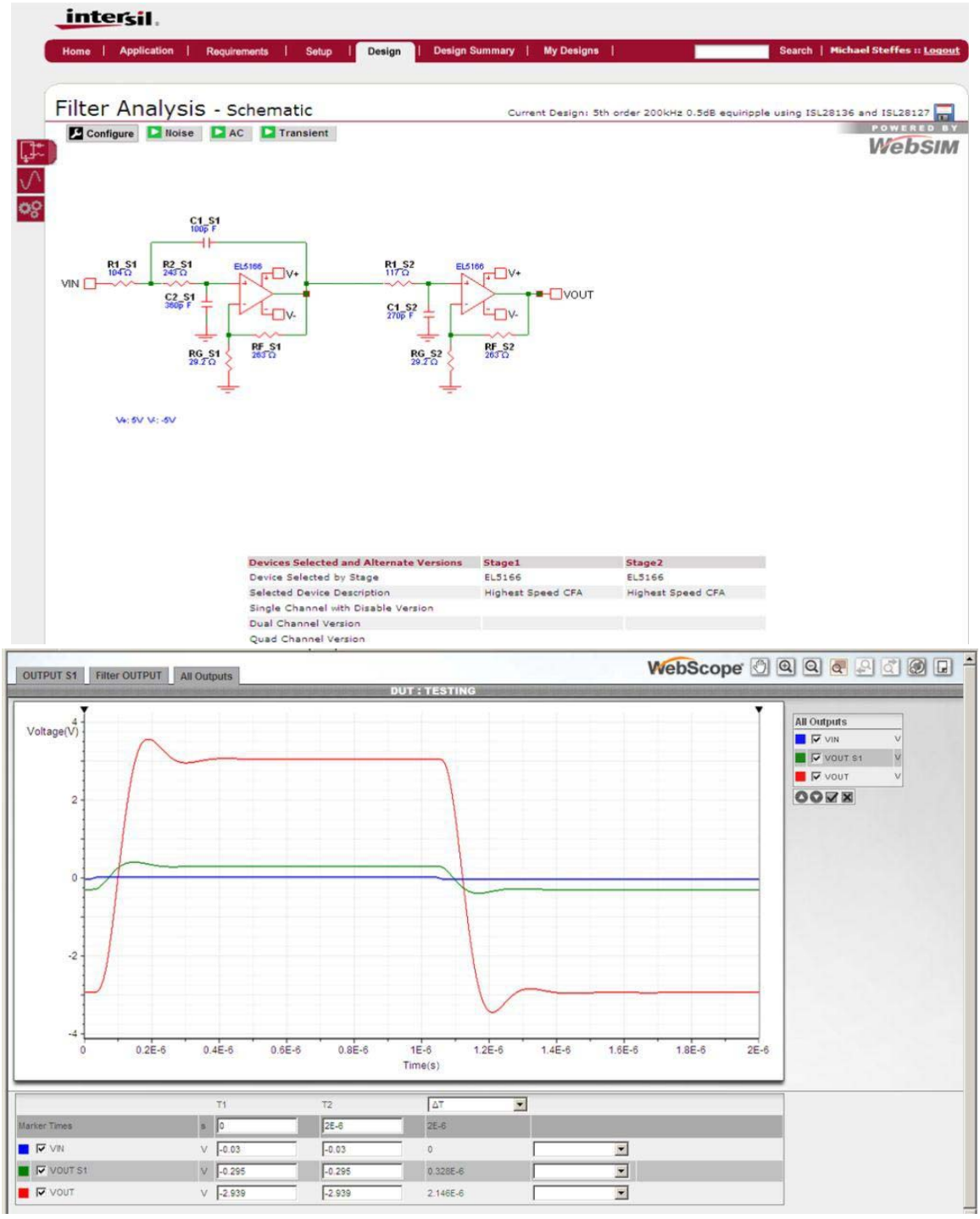

intersil
Home | Application | Requirements | Setup | Design | Design Summary | My Designs | Search | Michael Steffes :: Logout
Filter Analysis - Schematic
Current Design: 5th order 200kHz 0.5dB equiripple using ISL28136 and ISL28127
Configure
Noise
AC
Transient
POWERED BY WebSIM
C1_S1
100p F
R1_S1
104Ω
R2_S1
243Ω
EL5166
V+
V-
VIN
C2_S1
360p F
RG_S1
29.2Ω
RF_S1
263Ω
R1_S2
117Ω
C1_S2
270p F
RG_S2
29.2Ω
RF_S2
263Ω
VOUT
V+: 5V V-: -5V
Devices Selected and Alternate Versions
Stage1
Stage2
Device Selected by Stage
EL5166
EL5166
Selected Device Description
Highest Speed CFA
Highest Speed CFA
Single Channel with Disable Version
Dual Channel Version
Quad Channel Version
OUTPUT S1
Filter OUTPUT
All Outputs
WebScope
DUT : TESTING
Voltage(V)
Time(s)
All Outputs
VIN
VOUT S1
VOUT
T1
T2
ΔT
Marker Times
VIN
VOUT S1
VOUT

FIGURE 29.

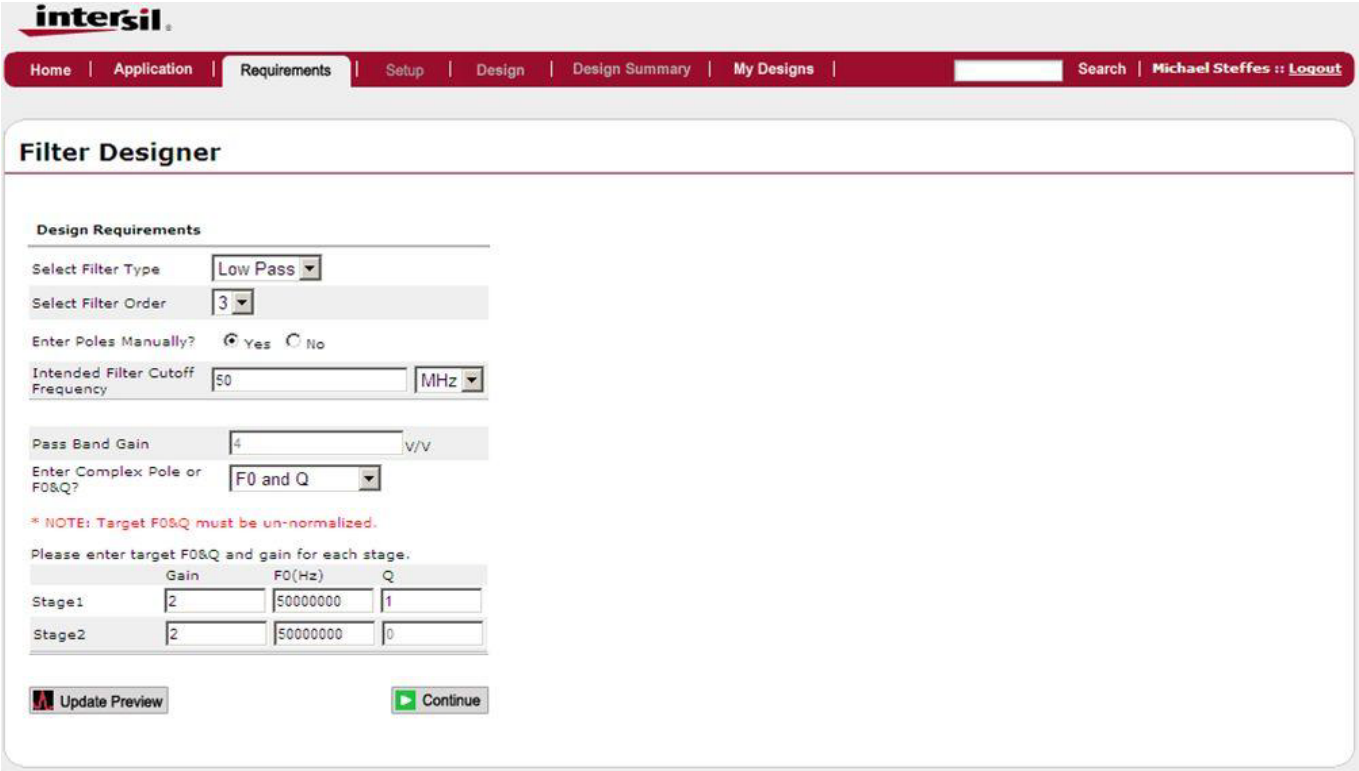


FIGURE 30.

Out of Range Requirements

When the inputs are set for very high Fo, Q, and/or gain, the tool might find that the required amplifier bandwidth exceeds that in the available op amp part set. As an example, try a 3rd order Butterworth design at 50Mhz where each stage is set up for a gain of 2. The manual pole selection page is shown in Figure 30 (the automatic flow is limited to 20Mhz maximum Fcutoff – so these higher frequency designs are only available in the manual pole entry option).

Hitting "Continue" will give the next page displayed in Figure 31 where it is reporting that the requirements exceed what is available (lower left). This page is sitting on the output stage where it reports we need 300Mhz Bandwidth for this gain of 2 stage. Part of the issue here is the 5V total supply – changing that to 10V will bring in some faster parts. Only CFA is offered as the 600Mhz GBP required of a VFA solution in this stage is not currently available but it does find suitable CFA devices. However, switching this last stage to an inverting single pole circuit will force the VFA implementation option and allow you to select the best possible part for that type of stage.

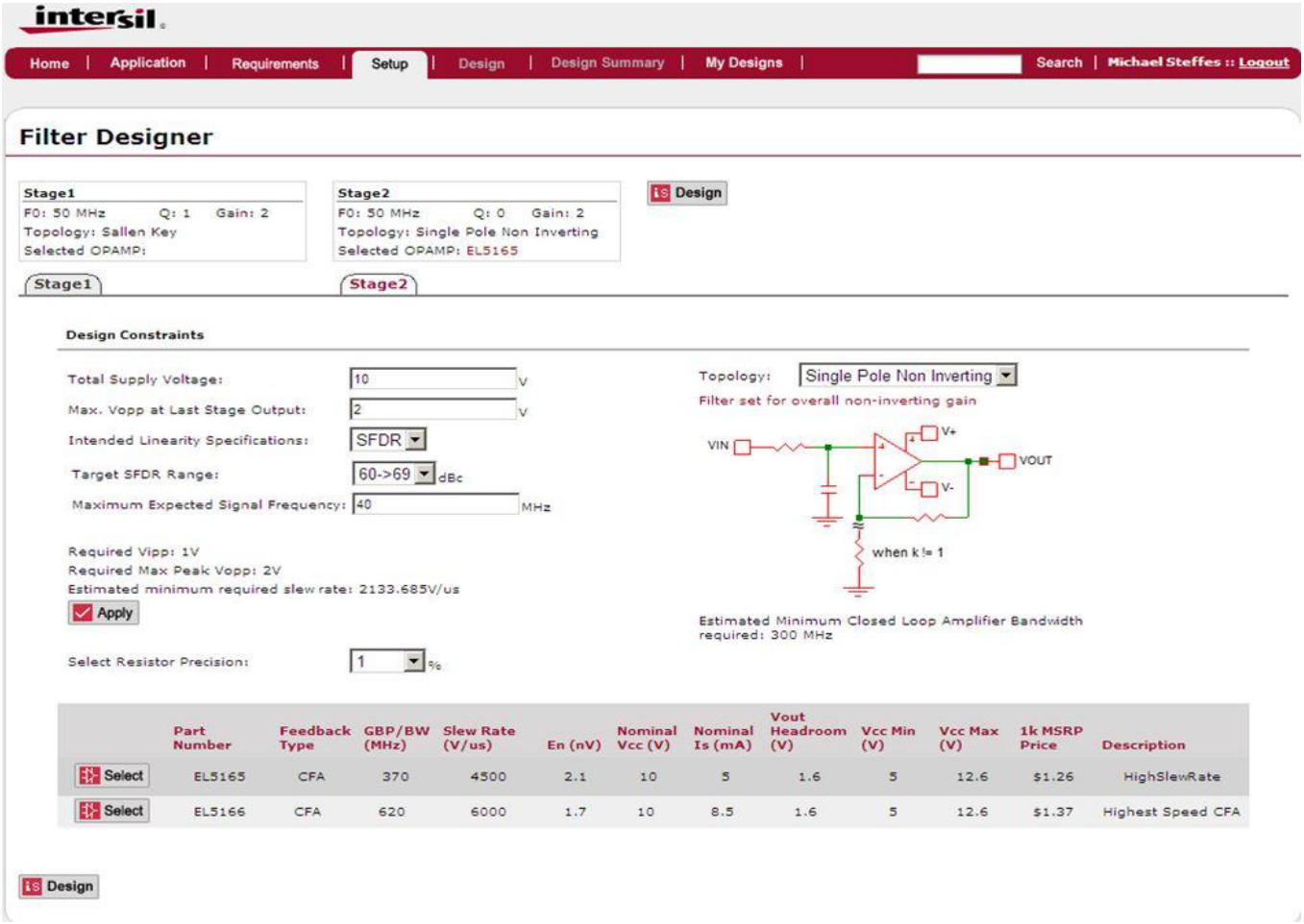


FIGURE 31.

Changing over to an inverting single pole output stage at 10V supply will initially give the screen displayed in Figure 31. Note here that it has not yet updated the reported bandwidth requirements – it is still showing the 300Mhz estimated for the non-inverting stage (which is a closed loop Bandwidth – going inverting in any stage will force a VFA solution and this note changes to report required gain bandwidth product).

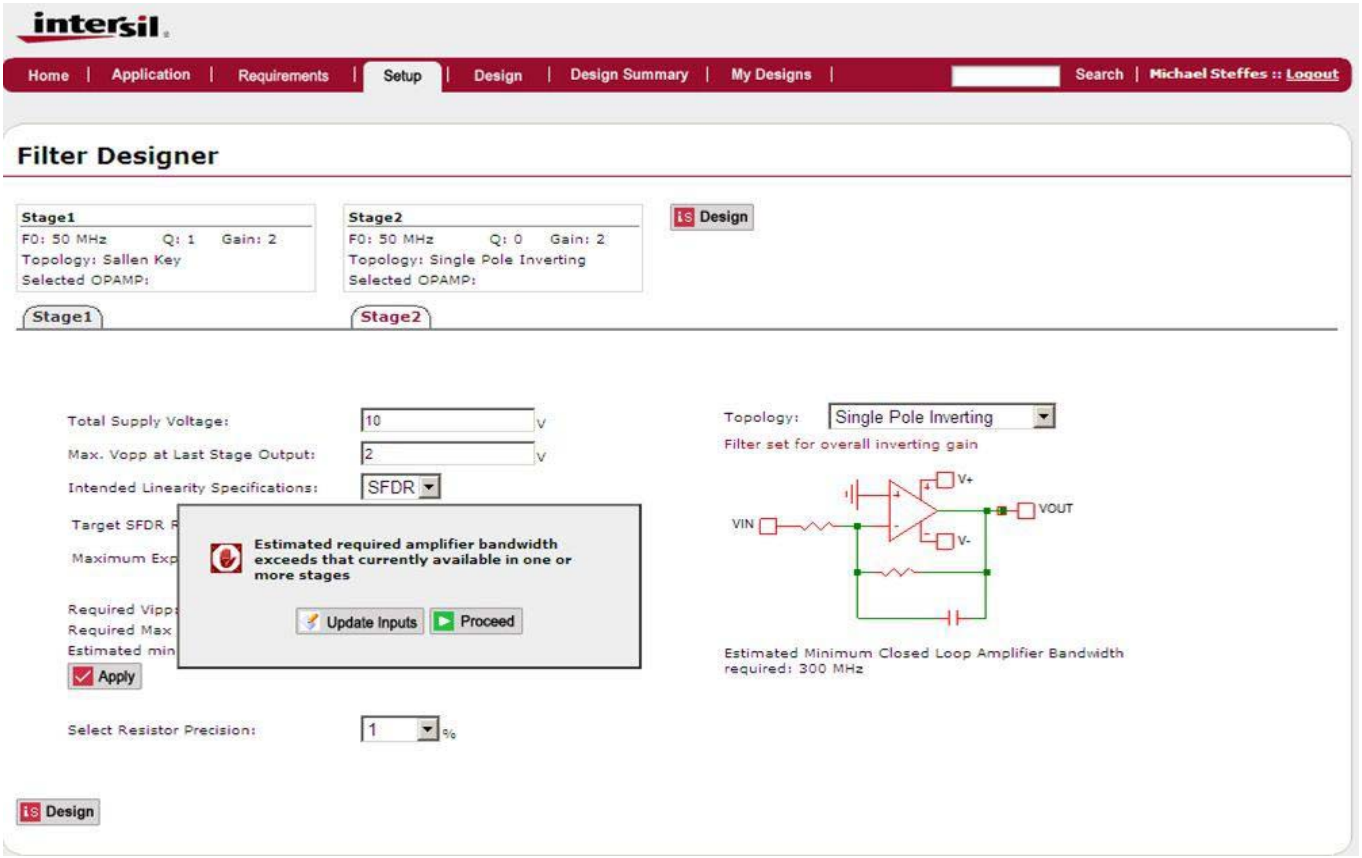


FIGURE 32.

Hitting "Proceed" here (Figure 32) will complete the calculation for the required gain bandwidth product and warn you again that the result (750Mhz below) exceeds that available in the current op amps loaded into the tool.

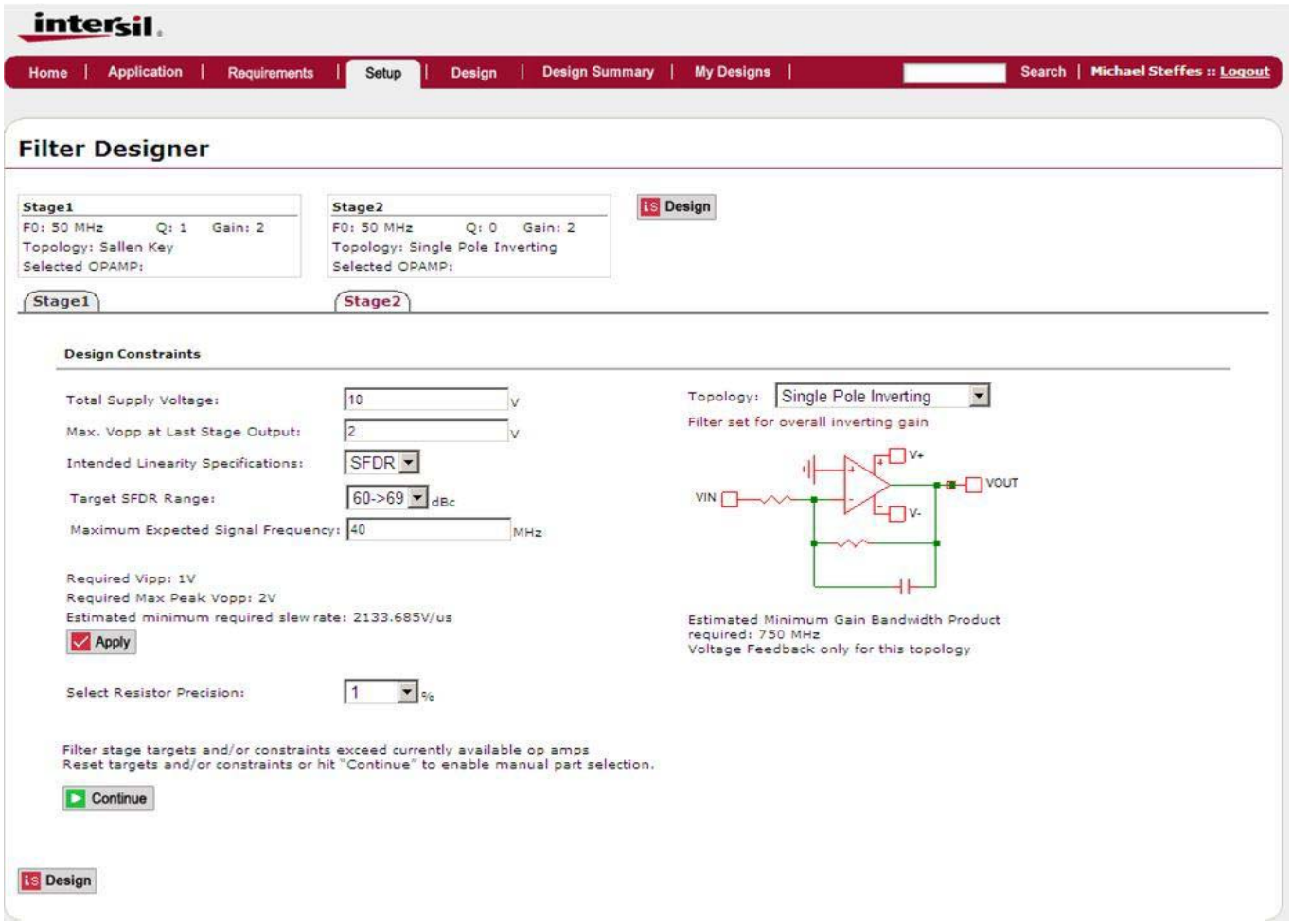


FIGURE 33.

Continuing through this warning will list the VFA parts that will work at the specified supply voltage in descending GBP order. Doing that and selecting the fastest device will display the screen shown in Figure 34.

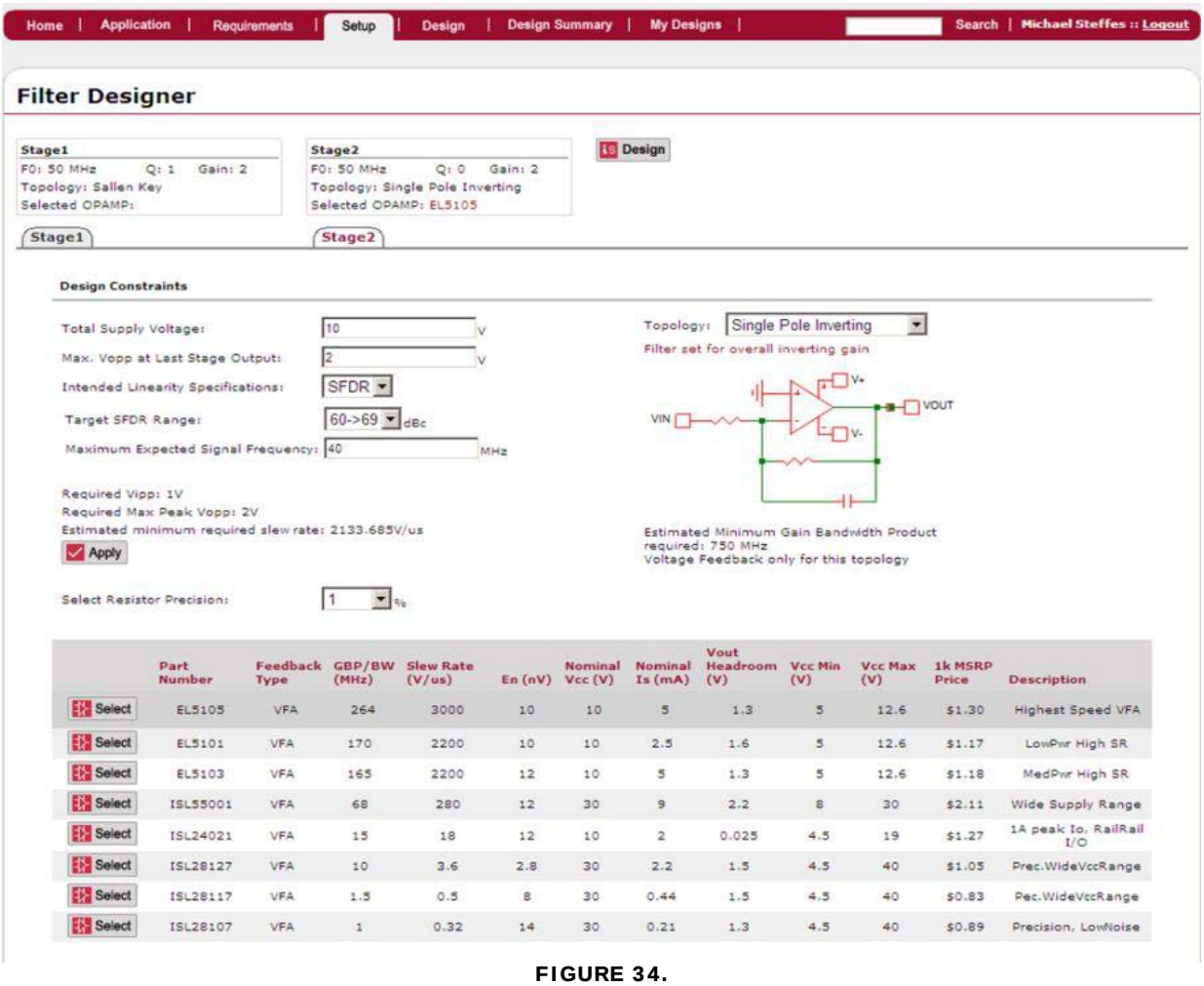


FIGURE 34.

In Figure 34, the EL5105 has been selected for the last stage. The tool will attempt a design adjusting the R&C values to hit the desired 50Mhz pole even though a 750Mhz GBP part is suggested – much higher than the available 264Mhz GBP in the EL5105. Note that in this design the non-inverting output circuit can be implemented at 50Mhz using a CFA op amp. That would be the preferred approach in this case, but for illustration purposes we will continue with this example.

Going now to the first stage, we see again that the tool is warning the requirements exceed the available op amps. It is asking for 997MHz at a gain of 2 in this stage. Hitting "Continue" will again list the parts that will work at this supply voltage in descending order of BW/GBP. The highest (at a gain of 2) will be the CFA parts and the screen shown in Figure 35 displays the fastest device selected.

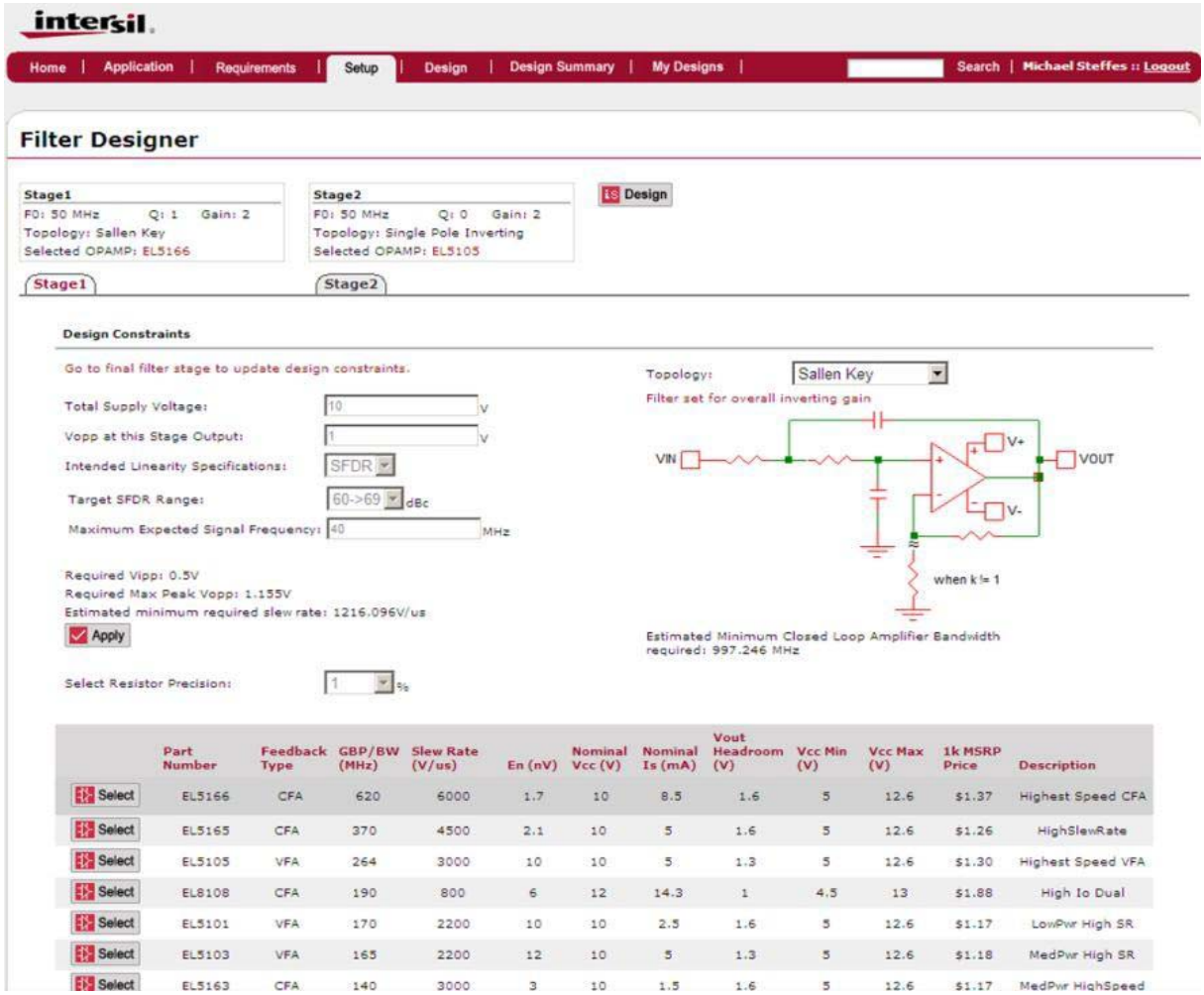


FIGURE 35.

Hitting "Design" will send the tool off to do the best it can to hit the desired poles and gain adjusting for the relatively low amplifier bandwidths. Doing that, will give the screen shown in Figure 36.

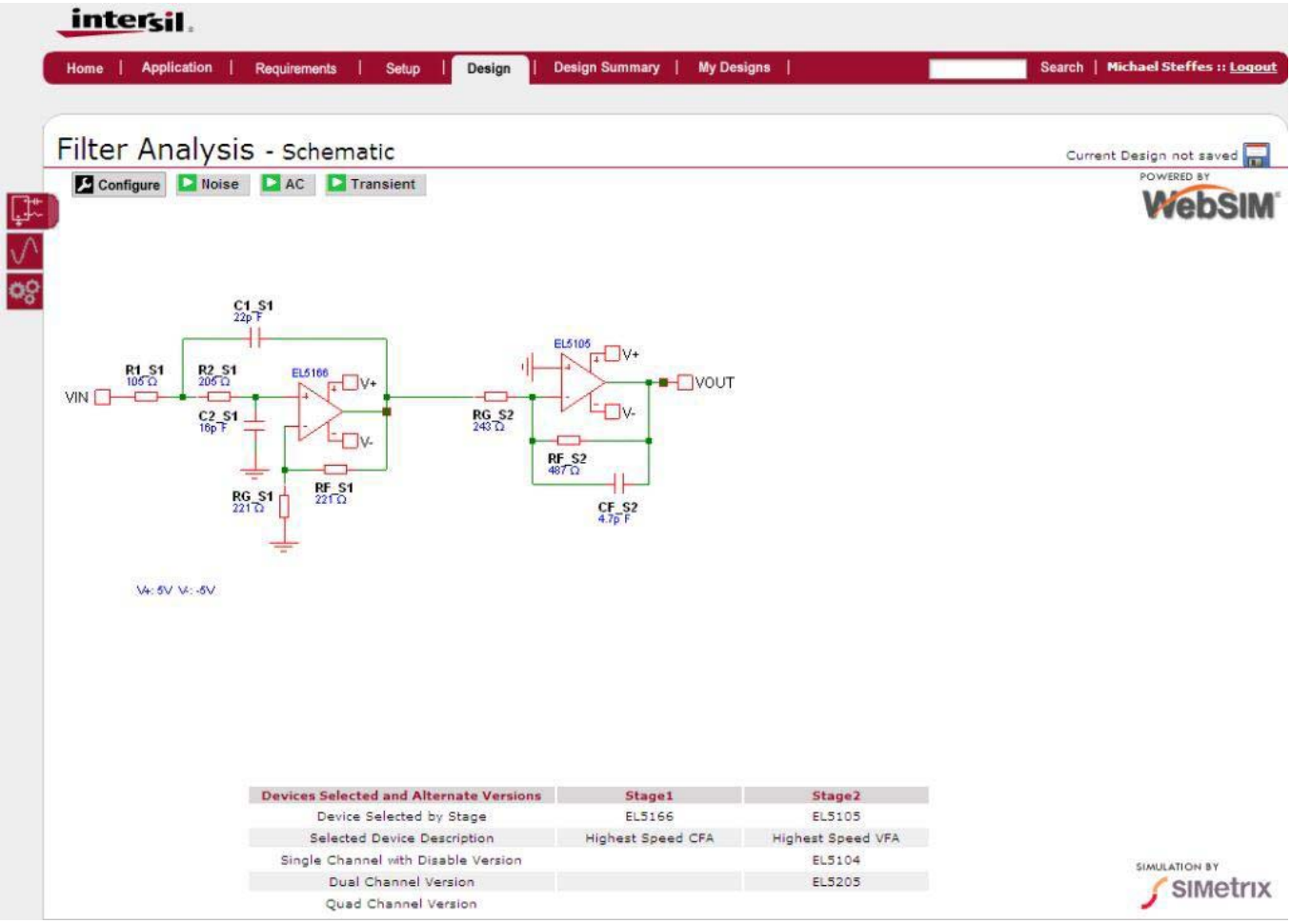


FIGURE 36.

Running the AC simulation and placing the ideal gain on top of the simulated output will show how closely this somewhat extreme design matched the desired shape. Zooming in on the 50Mhz region and moving the F2 marker to 50Mhz, shows the screen displayed in Figure 37.

FIGURE 37.

In Figure 37, we see the actual filter is rolled off to 8.7dB at 50MHz vs. an ideal of 9dB (3dB down from the DC gain of 4V/V or 12dB). Therefore, it is in error by 0.3dB.

This example is doing pretty good, but a similar design at 50MHz at higher Q or gain will start to deviate considerably from ideal. It is a good idea for Fo > 20Mhz to limit the desired gain and/or Q in each stage to reach successful implementation. In any case, the tool will attempt a design but the results may not be satisfactory.

These are just a few examples – a vast range of possible end designs are possible using the capabilities offered by this tool – go explore the ones of interest to you.

Appendix 1

Implementation Failure Modes

The design flows in the tool are attempting to deliver each individual stage tuned up to hit that stage Fo, Q and Gain considering numerous 2nd order effects within each stage. However, it is possible to see a multi-stage design deviate considerably from the expected response (in simulation) due to interstage coupling and cascading effects. Since numerous combinations of amplifier types are allowed in each design, it was not possible "a priori" to predict invalid combinations – however if the completed design has some of these issues, the simulations will show those then.

The algorithms setting the filter resistor values are attempting to limit their noise contribution vs. the op amps intrinsic noise. This would suggest ever decreasing resistor values but those have been limited to minimum settings for each topology. However, it is possible to end up with a design using relatively low R values. Normally, this is desirable. However, if a 2nd or 3rd stage using low R values is being driven from a prior stage that is a rail-to-rail output device, those often have considerable load sensitivity to bandwidth built into their simulation model. It is then possible to see a lower amplifier bandwidth in that earlier stage than the design algorithm is expecting due to this next stage loading effect. If this is a Sallen Key stage, lower amplifier bandwidth than expected will give a higher Q and lower Fo which will show up as a response that is peaking more but rolling off earlier. In an MFB stage, lower op amp bandwidth than expected will decrease the Fo at almost constant Q – so the total response might be rolled off a bit earlier than expected. An easy test for this issue is to re-design the stage following the RR output stage using lower C values forcing the R values up. This is supported in the redesign feature of the tool.

Each stage is designed checking for output clipping through either frequency response peaking or step response overshoot. This is done stage by stage working backwards from the nominally desired final output V_{P-P} towards the input stage. This does not account for cascaded peaking or overshoot in the completed design. The simulations will show this issue as a clipped output swing in the step response. Using

the semi-automatic design when the overall gain is >1in the filter limits the possibility of this happening by stepping the gains up from first stage to last stage. Of course if the overall filter gain is 1, this issue is still there and a step response simulation will show it most clearly. One of the tougher design points for multi-stage designs for this clipping issue is an overall gain of 1 condition. If that becomes an issue, asking for a bit gain in each stage will help this.

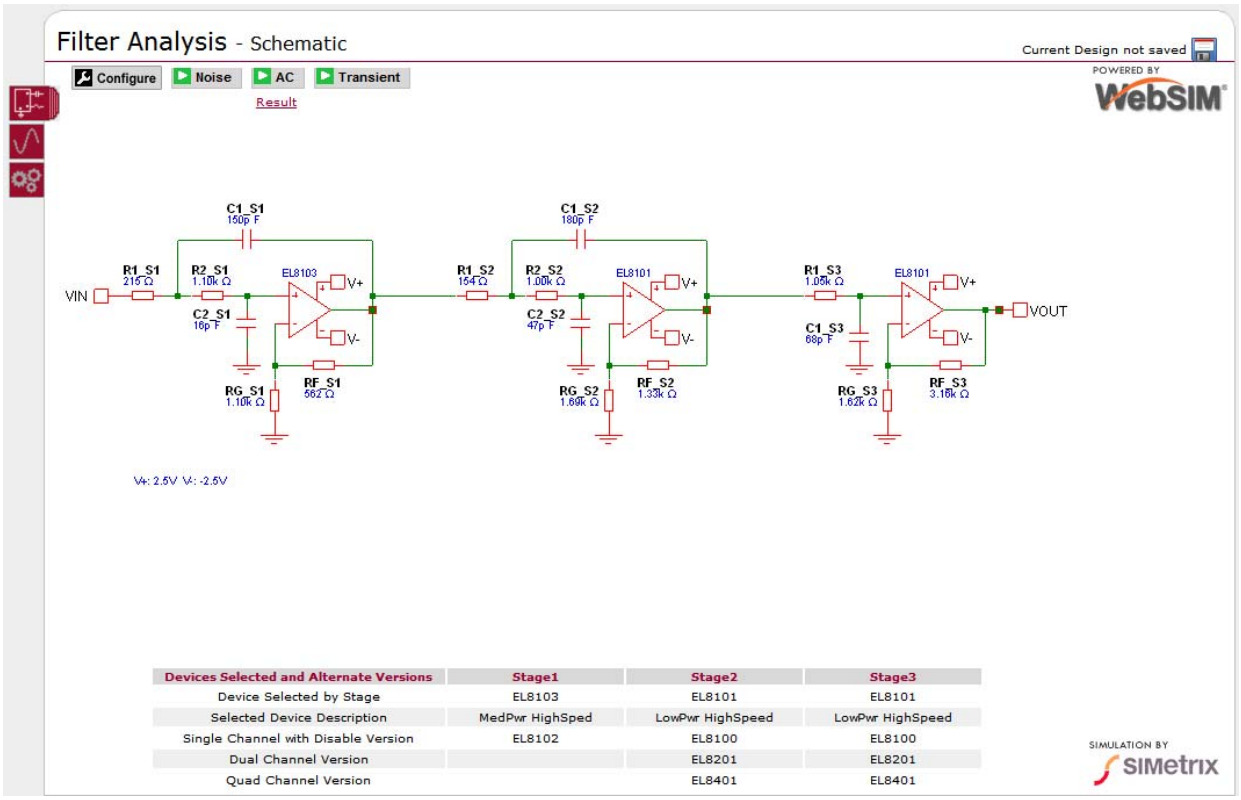
Appendix 2

Using Monte Carlo Analysis in iSim: PE to Evaluate Component Tolerance Impact in an iSim Active Filter Design

Monte Carlo simulation is a method of analysis that uses random sampling techniques to obtain a probabilistic approximation to the solution of a mathematical equation or model. Using this same approach applied to the filter R's and C's will show the effect of parameter variations, (such as the tolerance or aging of components), on an active filter design.

Implementing a Monte Carlo analysis in iSim:PE is quick to set up and easy to analyze. This appendix will step through setting device tolerances in a schematic and running a Monte Carlo simulation; then analyzing the results.

For this example, we allowed the tool to design a 5th order 0.25 dB Chebyshev Low Pass filter with a 6MHz cutoff frequency and a gain of 8V/V. As seen in Figure 38, this is a 3 stage 5V design using the EL8101 and EL8103 high speed rail-to-rail operational amplifiers. The R's and C's have been snapped to 2% and 5% step values (respectively) in the filter design tool. Their purchase tolerance from the standard value can be specified separately in the iSim:PE Monte Carlo simulation.



Devices Selected and Alternate Versions	Stage1	Stage2	Stage3
Device Selected by Stage	EL8103	EL8101	EL8101
Selected Device Description	MedPwr HighSped	LowPwr HighSpeed	LowPwr HighSpeed
Single Channel with Disable Version	EL8102	EL8100	EL8100
Dual Channel Version		EL8201	EL8201
Quad Channel Version		EL8401	EL8401

FIGURE 38. 5TH ORDER CHEBYSHEV LOW PASS FILTER

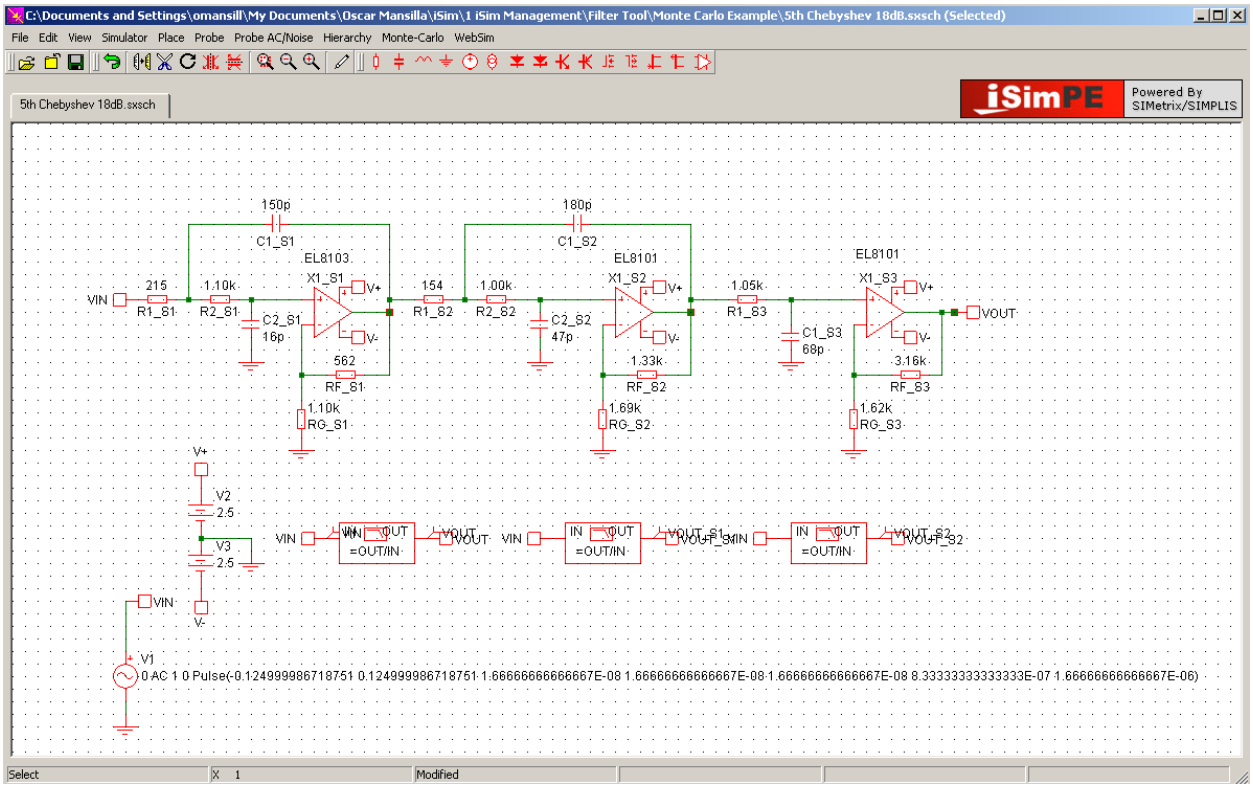


FIGURE 39. 5TH ORDER CHEBYSHEV LOW PASS FILTER ON ISIM:PE

The next step is to port the schematic to iSim:PE. Save the design, using the "Download Schematic" link on the "Design Summary" page of the tool, to a directory in your PC and open it on iSim:PE as shown in Figure 39.

First we will set the tolerance on the resistors and capacitors, the procedure for doing this is as follows:

1. On the Menu header select "Monte-Carlo" and then "Set All Resistor Tolerances."
2. An input box will pop up (Figure 40), enter the tolerance of the resistor in this case it would be 2% (must include the '%' sign). You will see a "2%" over the resistors when you are done.
3. Similar to the setting the tolerance on the resistors, select "Monte-Carlo" and then "Set All Capacitor Tolerances."
4. An input box will appear, enter 5% (must include the '%' sign) for the tolerance of the capacitor. You will see a "5%" over the capacitors when you are done.

One thing to note is that the distribution for the device tolerances is Gaussian with the tolerance representing a ±3σ spread.

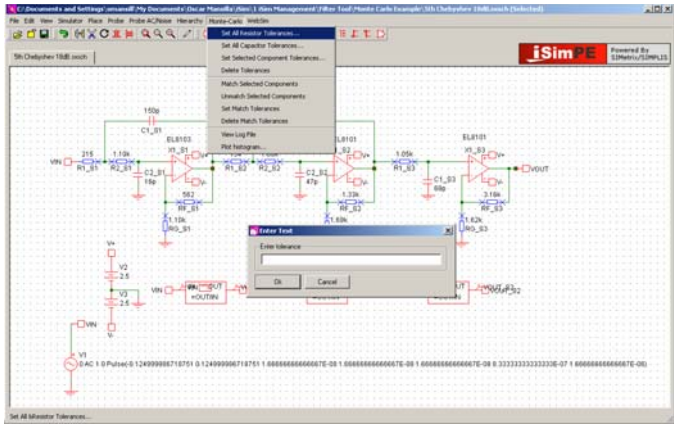


FIGURE 40. ENTER TOLERANCE WINDOW

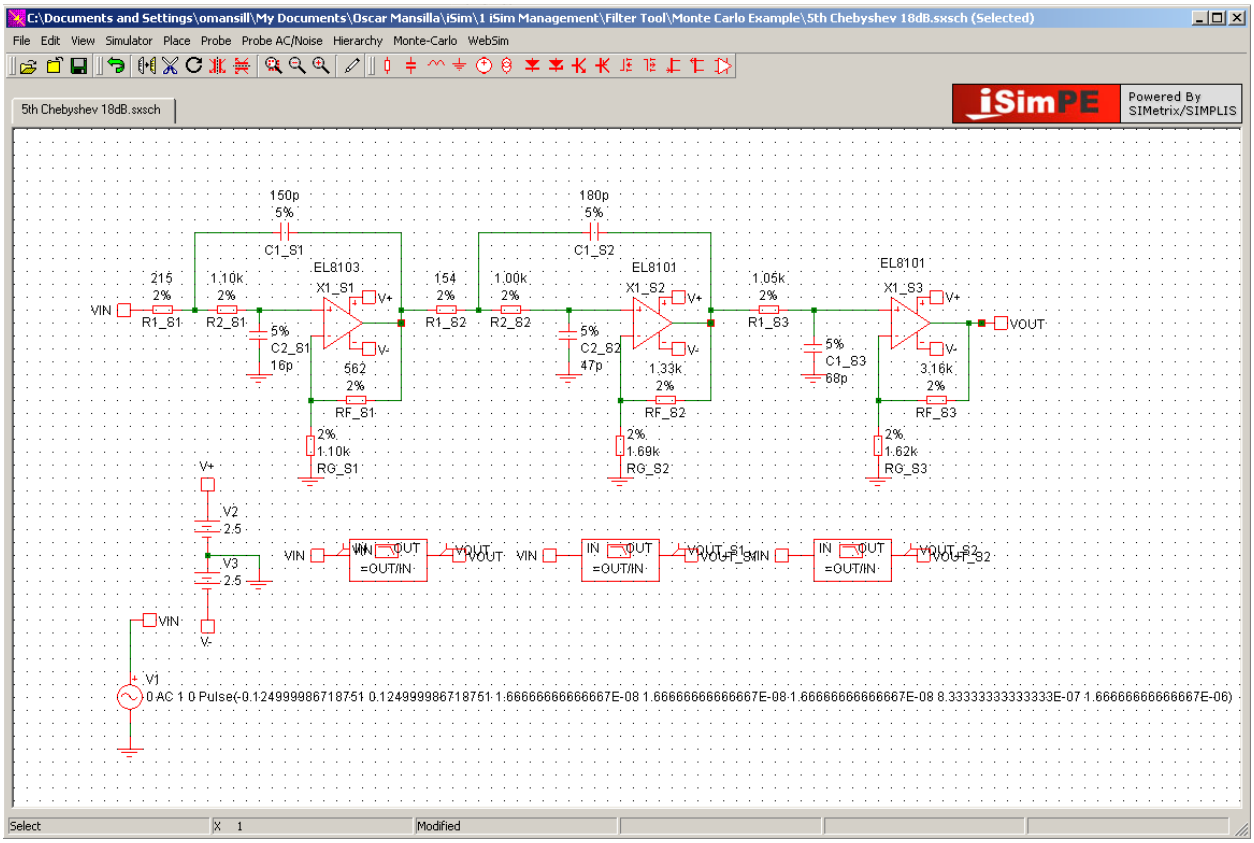


FIGURE 41. ISIM:PE SCHEMATIC WITH SET TOLERANCES

Once all component tolerances are set, it's time to enable Monte Carlo simulation:

1. On Menu header select "Simulator" then click "Choose Analysis."
2. The "Choose Analysis" window will appear notice the tabs on the top, clicking the tabs you can view the set parameters for the types of analysis that will be simulated. On the right side of the window you can view which analysis types are enabled, for the filter tool the schematic is automatically enabled for AC, Transient, and Noise.
3. To enable Monte Carlo simulation on the Transient Analysis, check the box next to "Enable multi step" in the Monte Carl and Multi-step Analysis section of the window
4. Press the "Define" button
5. In the "Sweep Mode" section you will see Monte Carlo is selected and in the "Step Parameters" section enter the number of steps to simulate. In this example we have set it to 50 steps (Figure 42).
6. By switching to the AC and Noise tabs Monte Carlo simulation can be enabled as described is Steps 3-5 above.

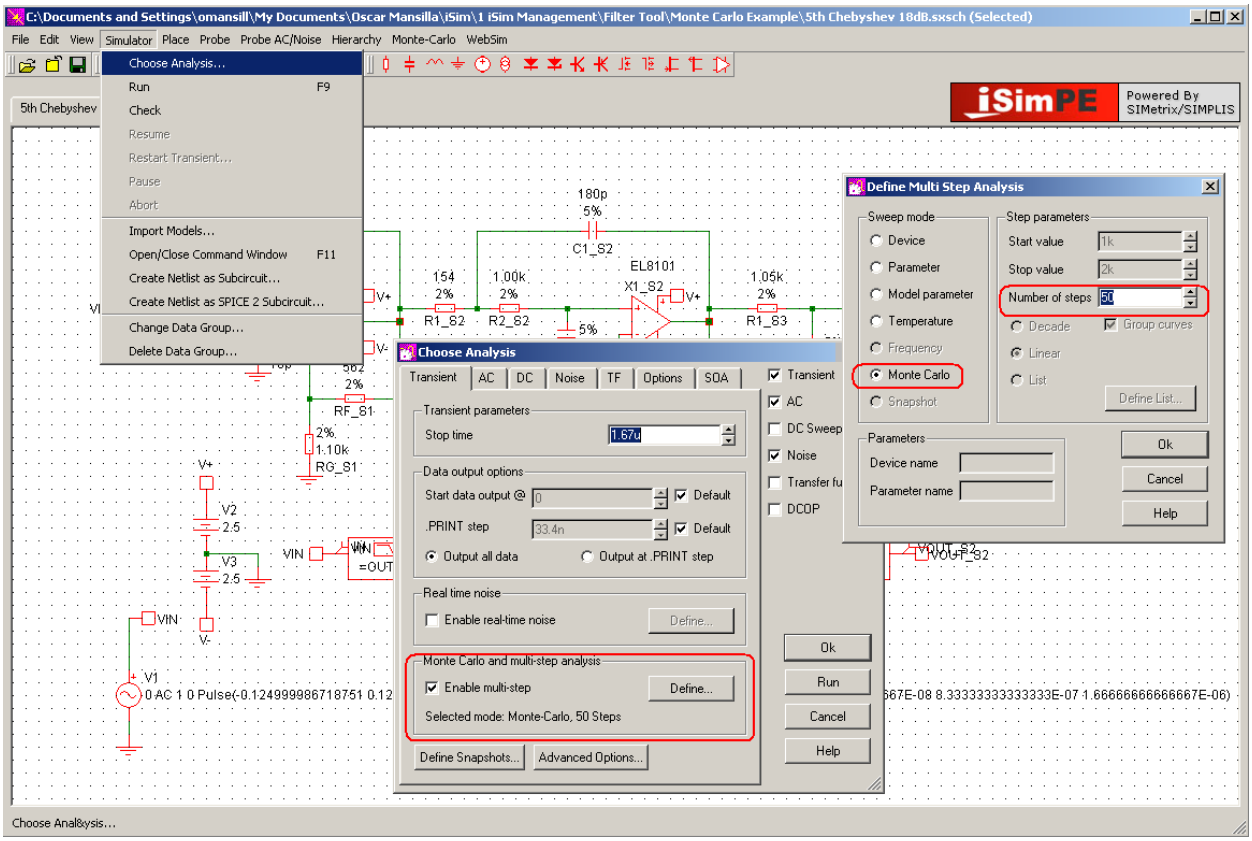


FIGURE 42. ENABLING MONTE CARLO ANALYSIS

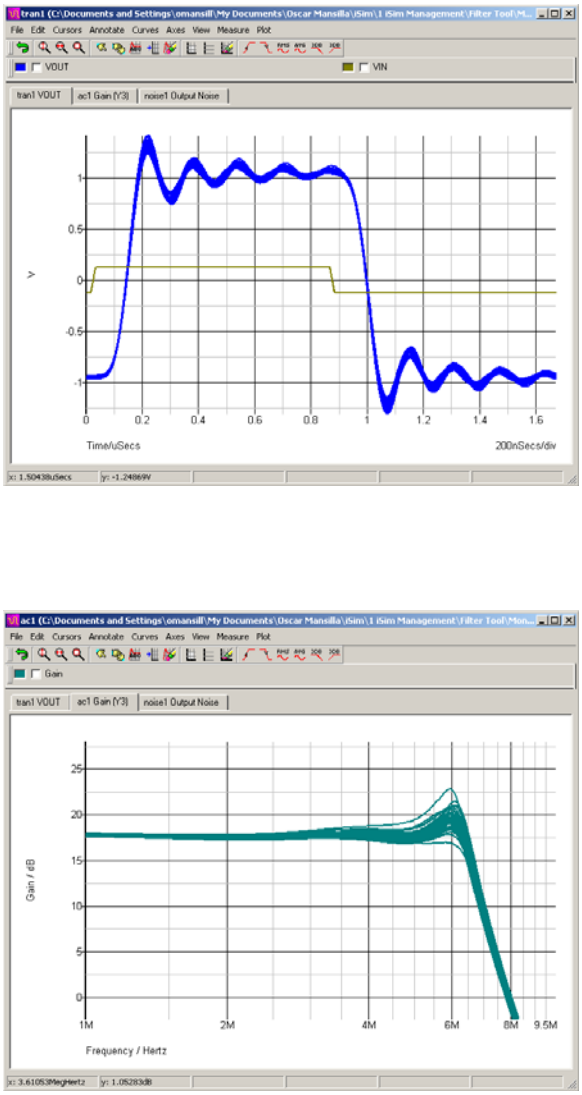


FIGURE 43. MONTE CARLO RESULTS OF TRANSIENT AND AC GAIN SIMULATIONS

Looking at the Figure 43, you can see the envelope of the Monte Carlo simulation with the component tolerances specified as in Figure 42. A sense of the impact of the component variation can be studied on key design parameters such as the overshoot, settling time, and delay of the filter. Similarly, AC plots can be studied for pass band ripple and cut off frequency variation due to the component tolerance. If these results indicate too much performance spread, a tighter tolerance on the R's and C's can be selected and the Monte Carlo analysis rerun. The op amp simulation models do not currently support parameter variation through Monte Carlo techniques. However, the SmartFilter design tool attempts to design in enough performance margin to each stage that the amplifier BW variations should be a minor effect.

Using iSim:PE allows more flexibility in analyzing an active filter design, Monte Carlo simulation is one of the many features that allows a designer to further study key design targets with the added effect of component variation.

Appendix 3

Using iSim PE to Test Alternate Stage Sequencing for Output Noise

The iSim Active Filter Designer delivers designs where the real pole (if there is one) appears as the final stage. There is little consensus in academia, or among the vendors, on the proper stage sequencing for multi-stage active filters. An easy way to see the impact of different stage sequencing is to use the schematic editing tools in iSim PE to re-order the stages for a filter delivered from the tool.

This discussion will step through the procedures to move the last stage to the first and show the difference this might have on the output noise. We will start with an example low pass design that is a 5^{th} order 6MHz Legendre Papoulis filter running on ±2.5V supplies and using very fast, but relative noisy, VFA op amps in the design (EL8101's). The circuit designed with the Active Filter Designer and then ported into iSim PE is shown in Figure 44.

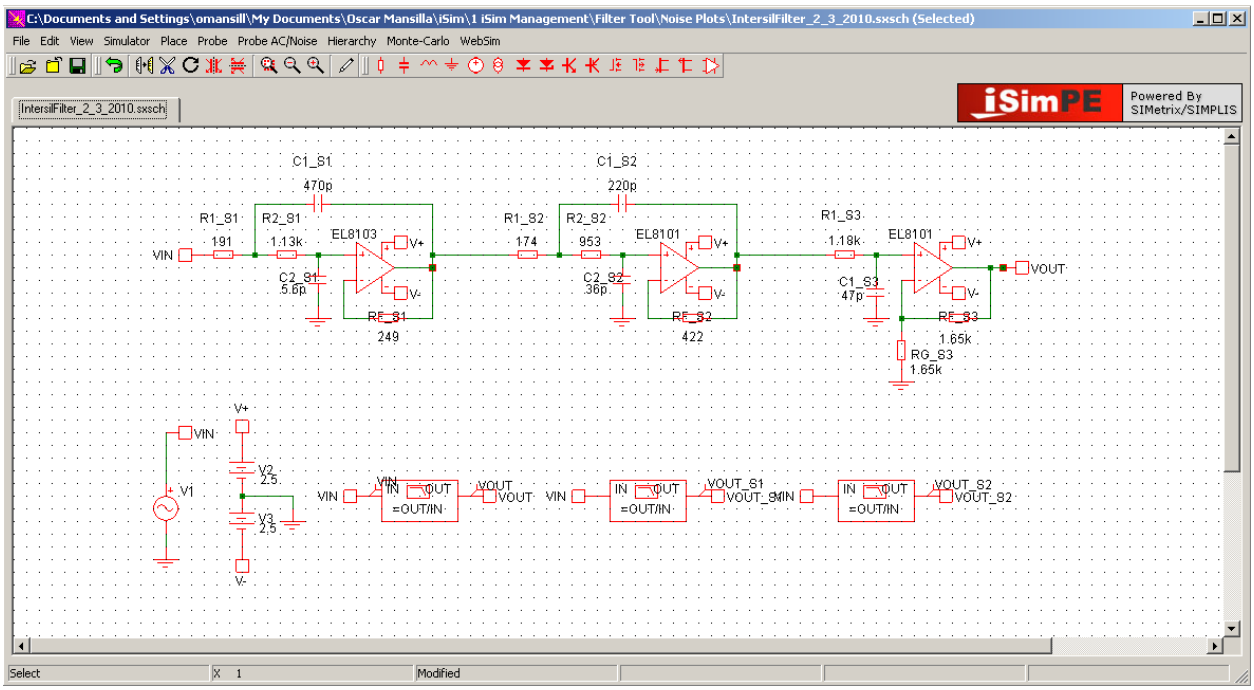


FIGURE 44. 5TH ORDER FILTER ON ISIM:PE

To start the schematic editing, there are four terminals that need to stay in place when moving the stages. These are the VOUT and VIN large terminals and the small terminals on the output of first and last stage. These terminals have coordinating names with AC and transient probes; if these terminals are moved along with the amplifier you will get erroneous results.

The first step is to remove the connections from the terminals on the last stage. Figure 45A is a zoomed in shot of the last stage. Circled in blue are the small and large terminals that must be disconnected. Also highlighted in blue are the three wire connections that should be deleted. Simply clicking the over the wire on iSim:PE highlights the connection in blue, then just hit the 'Delete' key on your keyboard to delete the connection. Figure 45B shows the same schematic with the wires deleted and the last stage isolated from the previous stage and the terminals.

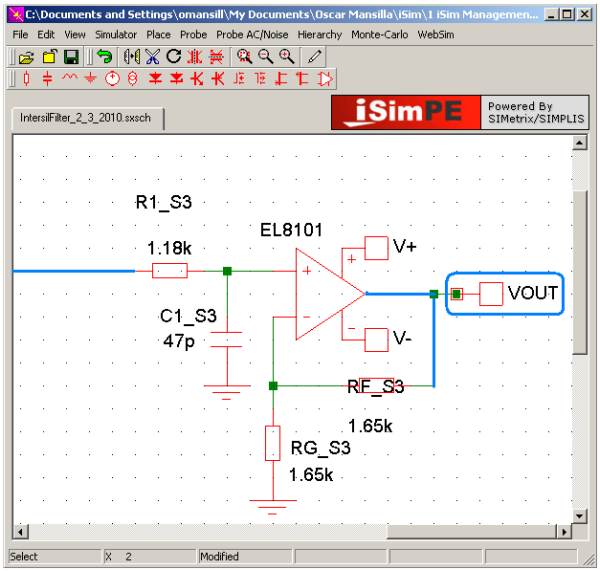


FIGURE 45A. LAST STAGE WITH CONNECTIONS HIGHLIGHTED

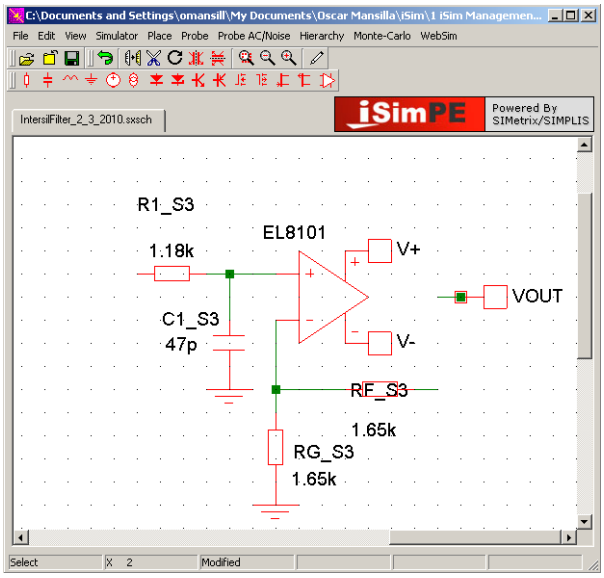


FIGURE 45B. LAST STAGE WITH DISCONNECTED WIRES

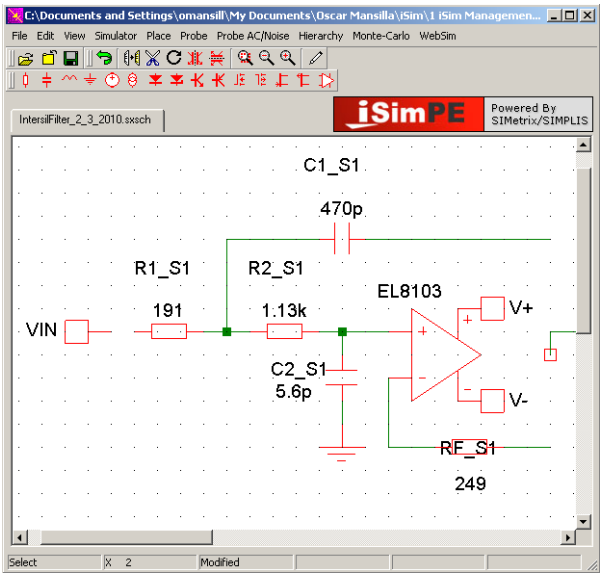


FIGURE 46B. FIRST STAGE ISOLATED FROM

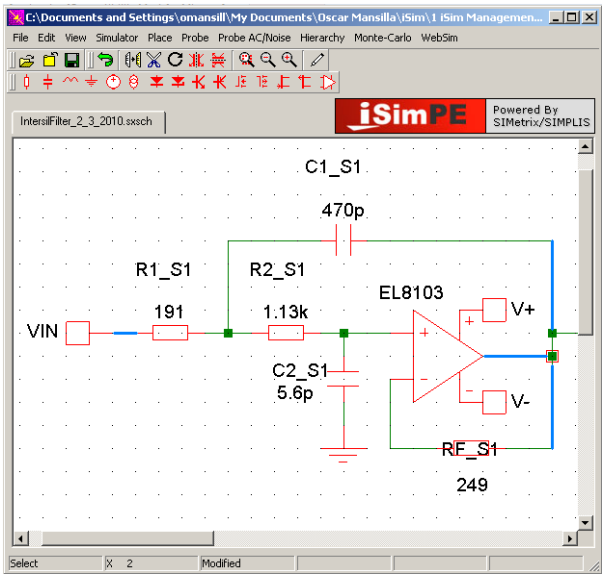


FIGURE 46A. FIRST STAGE WITH CONNECTIONS HIGHLIGHTED

The same process can be done for the first stage. Figure 46A highlights the recommended wires that should be deleted in blue. Occasionally the VIN terminal will be connected directly to the R1_S1 resistor, in this case simply click on the terminal and drag it to the left in order to isolate the first stage from its input.

With the stages isolated, the last step is to move the last stage to the first and vice versa. You can draw a box around the first stage and it will select all the components. Figure 47 shows the last and first stage isolated and all components for each individual stage selected. By simply dragging one of the stages away from the main schematic, you can make room for the other stage to be dropped in that place. The other stage you placed away from the schematic can now be moved to vacant stage. All that is left to do is redraw the wires. The wiring option is on the menu bar and indicated by a pen symbol. Figure 47 has a green box pointing out where to find the wiring button. Figure 5 is the complete schematic where the stage orders are changed.

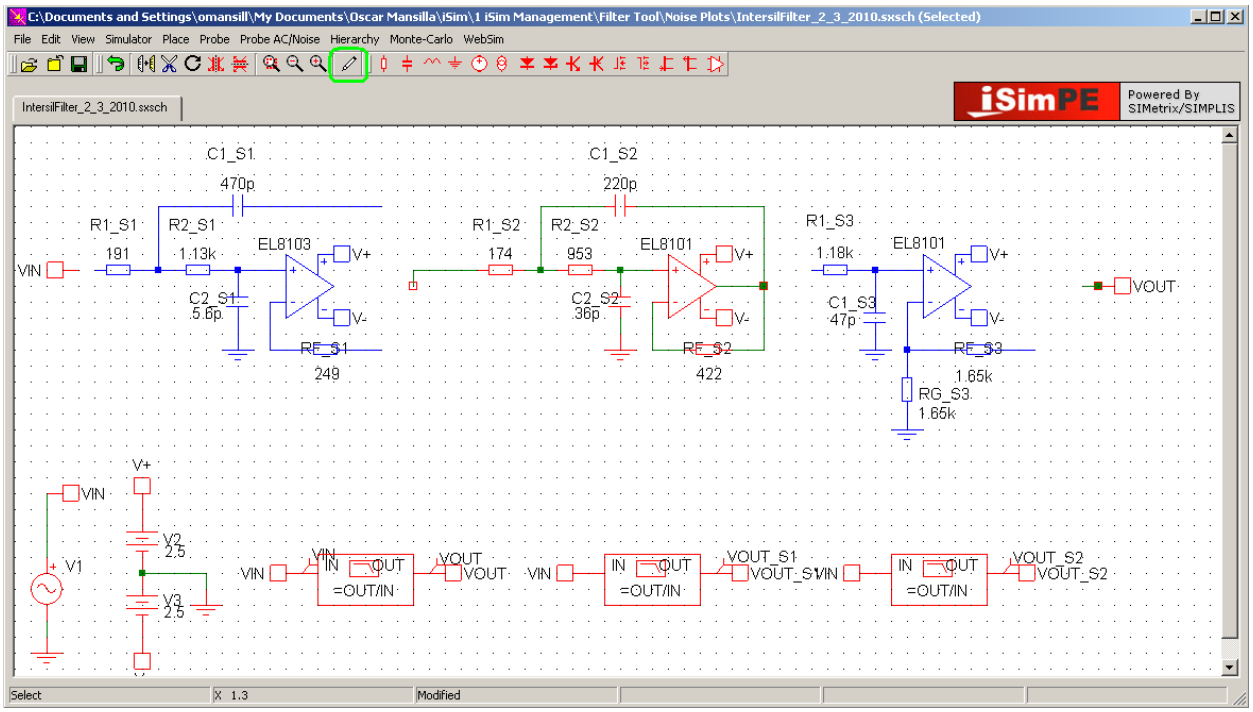


FIGURE 47. FIRST AND LAST STAGE ISOLATED

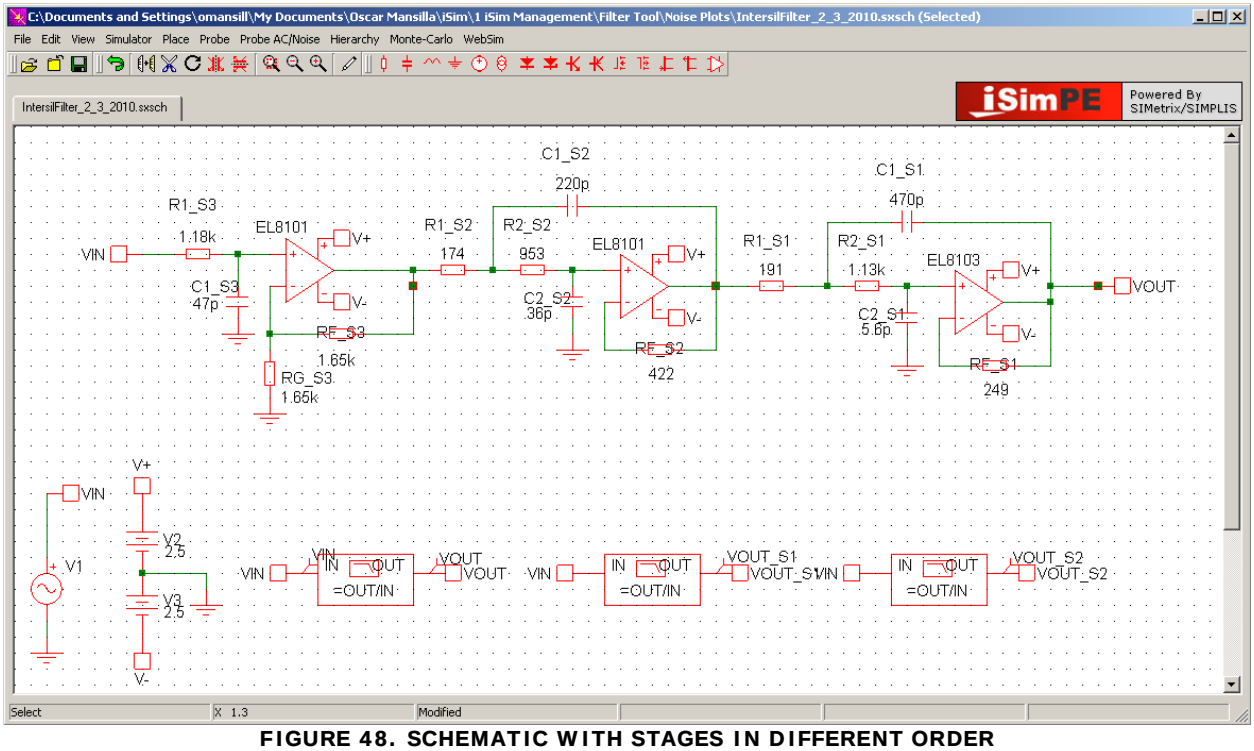


FIGURE 48. SCHEMATIC WITH STAGES IN DIFFERENT ORDER

To plot the Output Noise after running a simulation, on the menu toolbar go to "Probe AC/Noise" and select "Plot Output Noise." One thing to note here is that if the current waveform you are viewing is for the Transient simulation, the output noise plot will show up on a new graph. However if the current plot you are viewing is the AC plot, the noise plot will show up on the same graph with a different Y – axis.

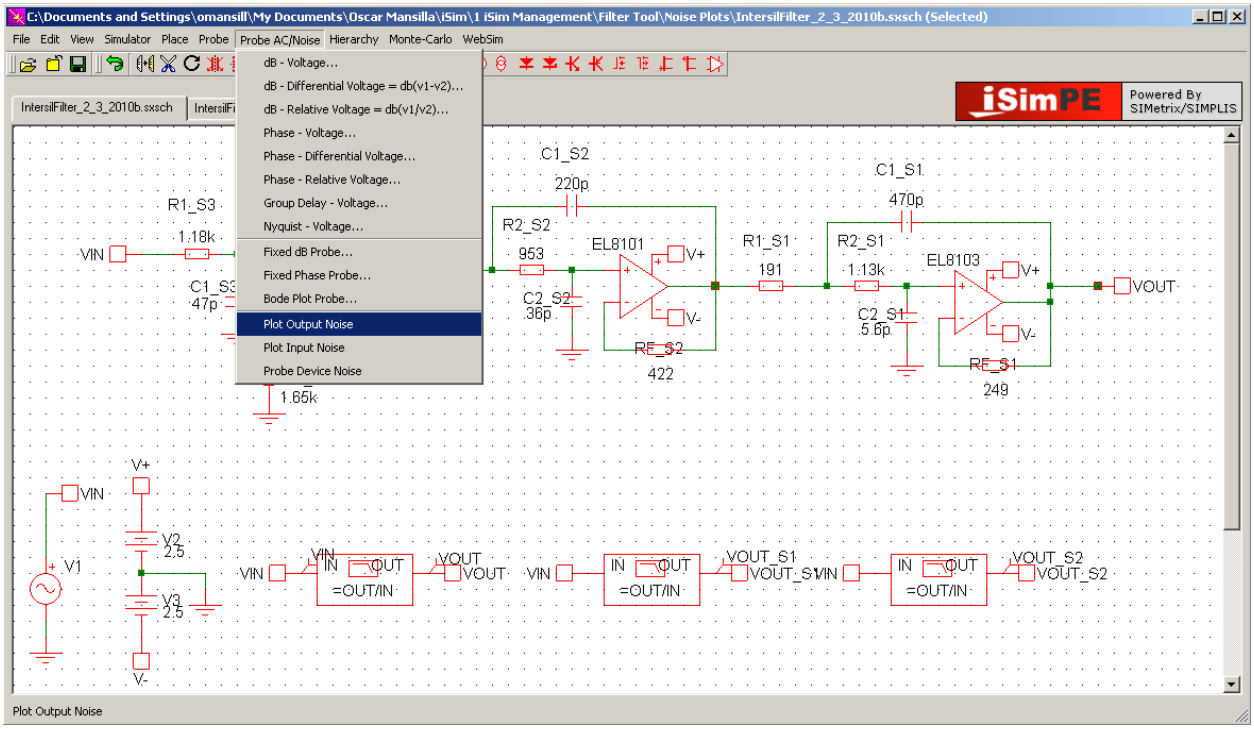


FIGURE 49. PLOTTING THE OUTPUT NOISE

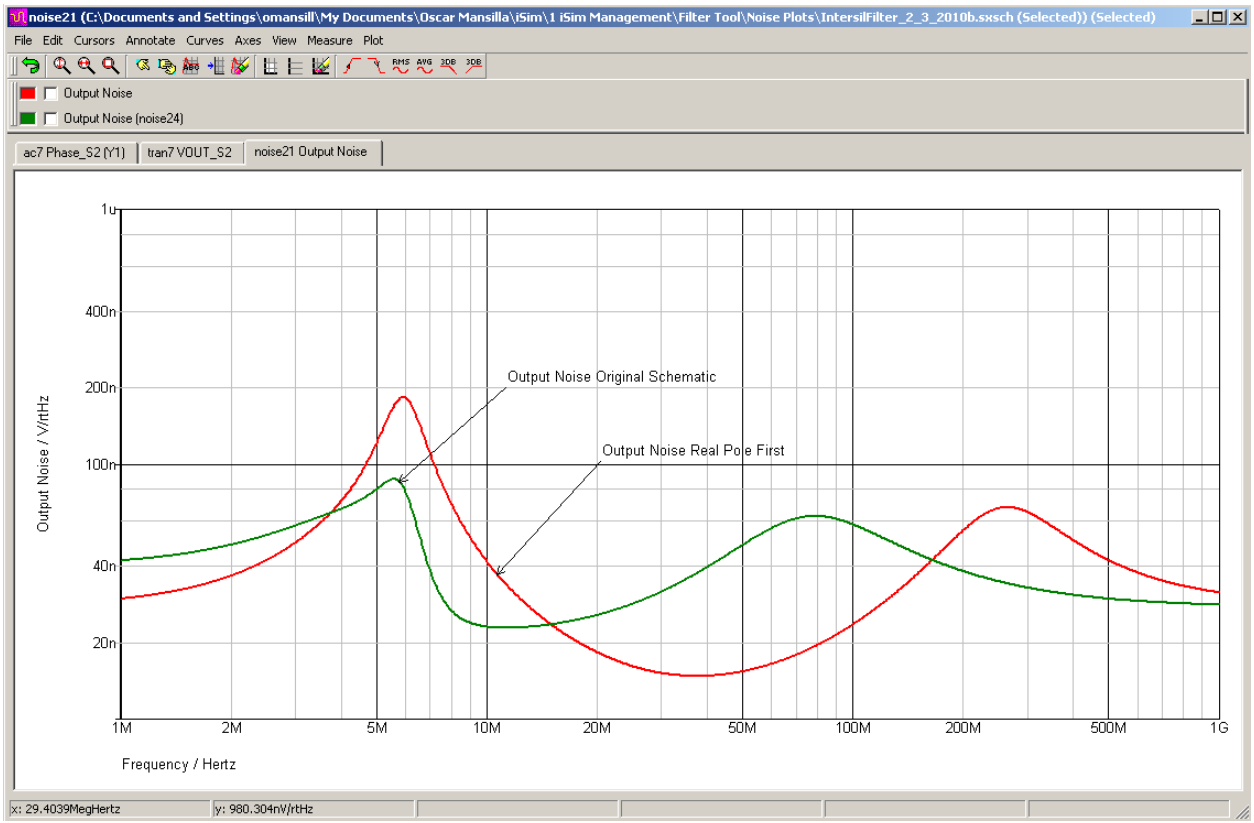


FIGURE 50. NOISE PLOTS BEFORE AND AFTER STAGE CONVERSION

Figure 50 shows the output noise for the original schematic and the modified version with the real pole as the first stage. As would be expected, the low frequency noise with the Gain of 2 real pole first shows lower spot noise (this is one common argument for putting it and most of the gain first). However, having the complex poles come later in the filter shows a higher peak in the final output spot noise. If the "integrated" noise is of most interest (commonly the case for low pass filters), the more peaked output noise will integrate to higher total noise vs. the original design where the low frequency noise is higher, but the peaking considerably lower.

It is certainly not always clear which pole sequencing will give the best results, but once the design is in iSim PE, it is easy to try alternative approaches. The most flexible approach to testing different poles sequencing and stage gains would be to use the manual pole entry feature of the Active Filter Designer to spread that gain as desired, sequence the 2nd order poles as desired, accept the last stage as a real pole if the order is 3 or 5, and then re-order the stages using the approach shown here testing either noise, clipping, etc. The semi-automatic flow built into the Active Filter Designer seems to give good results but it is not possible to claim that they are "optimum" solutions.

Appendix 4

Showing All Available Op Amps in the Tool

The Setup step analyzes the requirements in each stage to remove op amps from the "Recommended Op Amps for this Stage" list of devices and then sorts them in approximate ascending order of design margin. There can be situations where the designer would like to see the devices that have been screened out in this step. At the bottom of the "Recommended" device list, there is another tab to display "Alternate Op Amps". Hitting this tab will list all remaining op amps currently supported by the tool in ascending order of GBW/BW with the following constraints -

1. The device is not already listed in the Recommended set of parts
2. If the stage is inverting, only the remaining VFA devices are listed as CFA devices cannot be applied.

Showing these "excluded" devices will allow the designer to override the selection algorithms in the tool and choose any of the available devices for the design. This should be done with extreme caution - particularly with respect to desired total supply voltage across the op amps vs. the Min/Max operating supply voltage range for the device chosen. It would be very easy using this approach to select an op amp that only operates up to say 5.5V maximum supply voltage where the final design is intended for say ±5V operation. The simulation macromodels for the op amps do not include parameter adjustment vs. supply voltage nor do they sense an out of range condition on the power supplies. So the simulations here might show valid performance in the just mentioned examples whereas the board implementation will fail.

In other situations, it might be very useful to manually override the selection algorithms to push a design a bit further than the somewhat conservative assumptions used in the built-in selection criteria.

As an example of using this feature, go to the highest limit on Fo and design a 3rd order Butterworth using the manual pole entry feature where each stage is giving a gain of 5. This will report that the required amplifier speeds are not currently supported as shown in Figure 51.

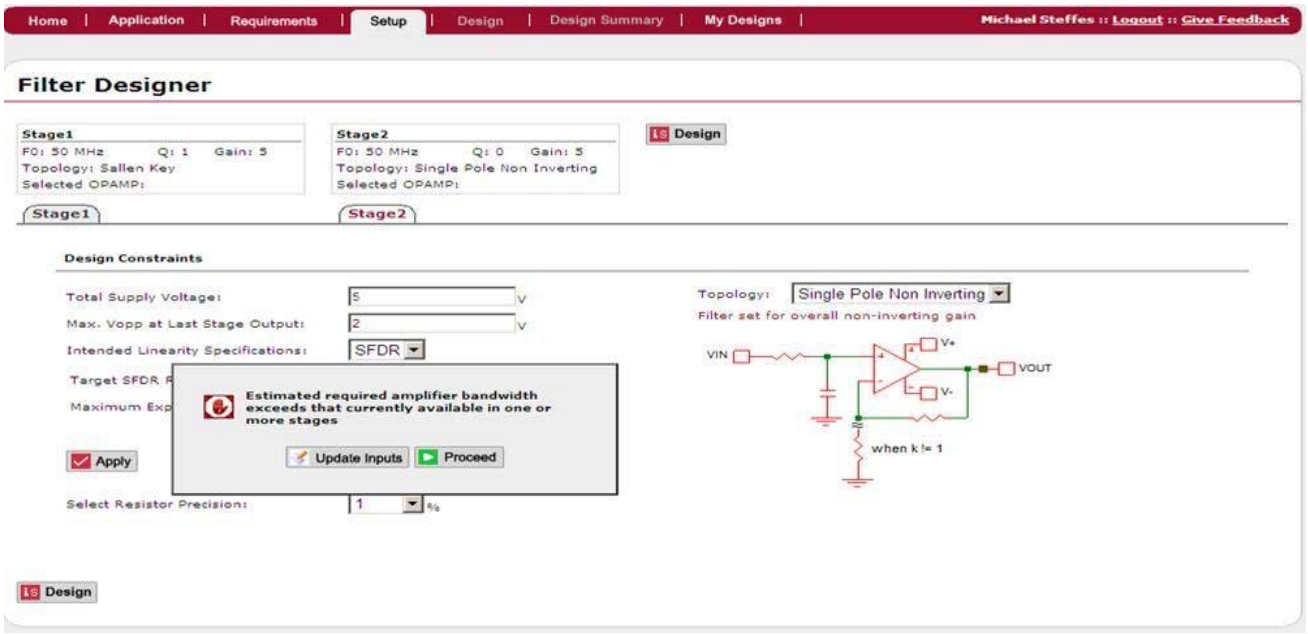


FIGURE 51. GLOBAL WARNING MESSAGE

In Figure 51 we see the first stage is set to a 2nd order Fo = 50MHz with Q = 1 and Gain = 5V/V while the 2nd stage is a single real pole at 50Mhz. This first warning is a global test of the requirements where some, but perhaps not all, of the stages are asking for too much speed. The next step will look only at the current "active" stage and give the warning shown in Figure 52.

Part of the issue in this warning is that the 5V total supply voltage with $2V_{P-P}$ output is excluding all the CFA op amps from consideration due to output headroom considerations in this output stage. Changing the supply voltage to 10V with a $4V_{P-P}$ output swing then hitting apply will generate the global error message (since the first stage is still beyond the available devices). Proceeding through that warning again will get the screen displayed in Figure 53 where the tool is now saying it can find parts for the output stage.

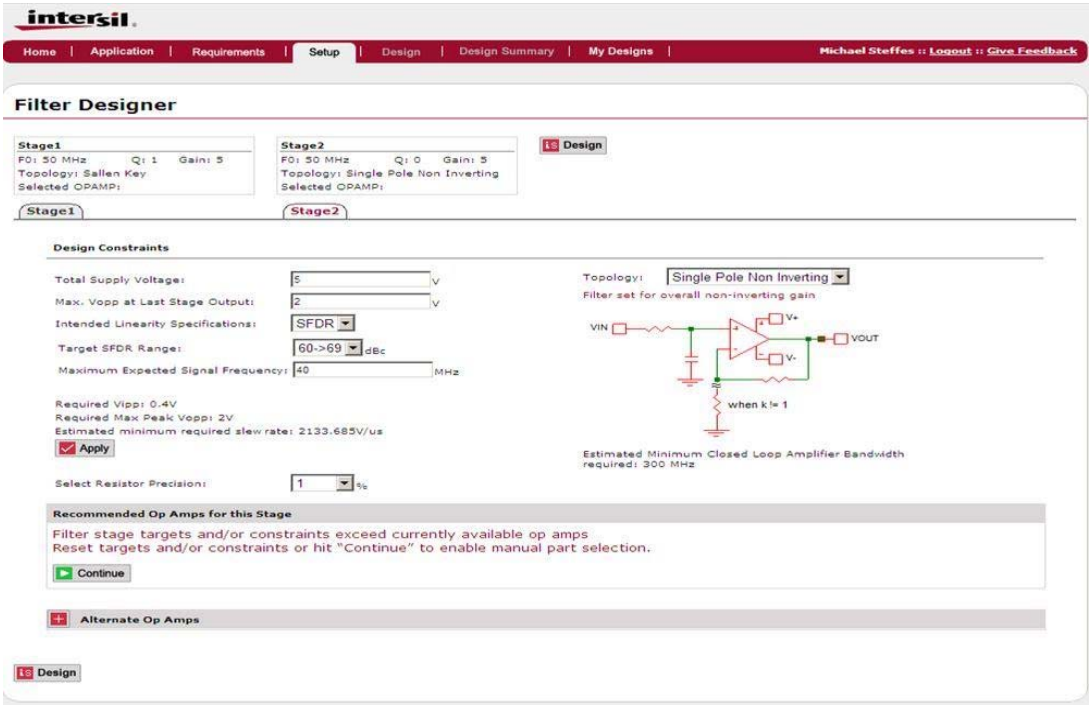


FIGURE 52. STAGE WARNING MESSAGE FOR STAGE 2

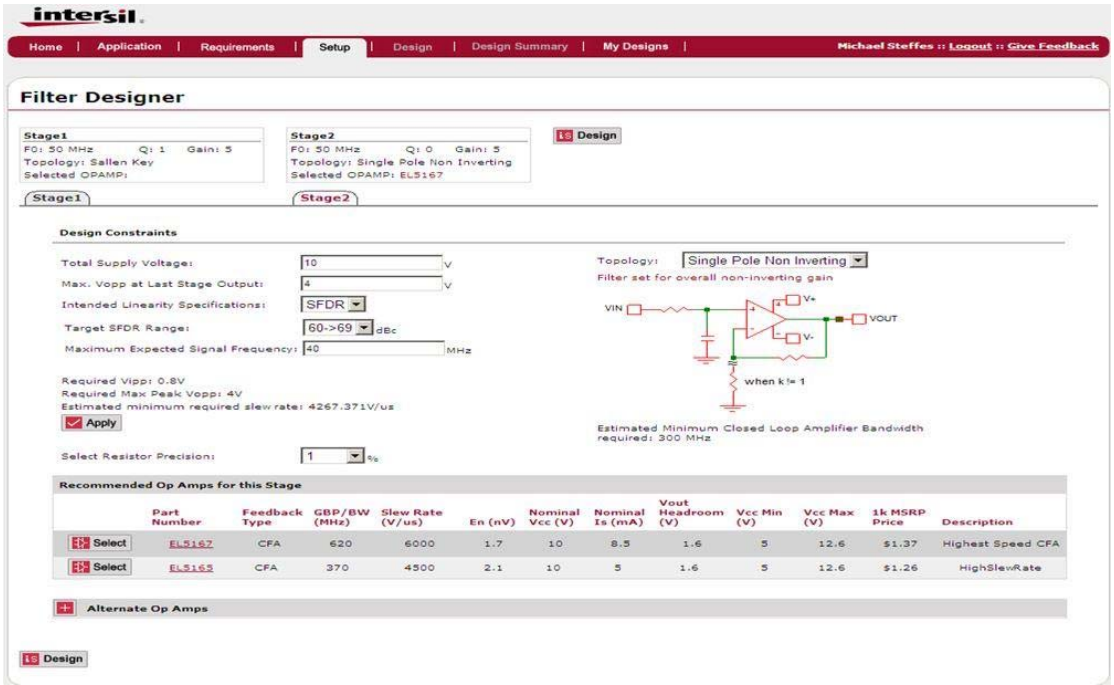


FIGURE 53. VALID SOLUTION FOR OUTPUT STAGE

Note this stage is says it needs 300MHz Bandwidth at a gain of 5. The CFA devices are listing their nominal BW over a range of gains. The tool will adjust the feedback resistor in its solutions to hold that bandwidth up through a maximum gain in the 3 to 4V/V region. As the required gain increases, the bandwidth is held constant by reducing the feedback resistor value. However, that eventually leads to such low values that the added loading of the feedback network will start to bandlimit physical implementations. Each CFA device has a built-in limit on this adjustment that will start to increase the feedback R from optimum (for BW) as the loading considerations become dominant. This will start to bandlimit CFA based circuits and that is considered in the tool when proposing devices and executing the design.

The tool has picked the EL5167 for this output stage as the most suitable device. This is because the 370MHz shown for the EL5165 will actually be <300Mhz at the required gain of 5. Note the first stage shows no device selected by the tool. This indicates the estimated requirements in this stage exceed all devices currently loaded into the tool.

Expanding the "Alternate Op Amps" selection by clicking on the "+" key will simply list the remaining devices available in the tool. Doing this and scrolling down will show the 2 - Recommended op amps at the top then all of the VFA devices listed in ascending GBP/BW then all the CFA devices listed in ascending GBP/BW order. These are shown in Figure 54 (as devices are added to the tool this list with change accordingly).

Select	EL5167	CFA	620	6000	1.7	10	8.5	1.6	5	12.6	$1.37	Highest Speed CFA
Select	EL5165	CFA	370	4500	2.1	10	5	1.6	5	12.6	$1.26	HighSlewRate

Alternate Op Amps — These parts do not satisfy one or several of the necessary design targets and/or constraints – select cautiously

	Part Number	Feedback Type	GBP/BW (MHz)	Slew Rate (V/us)	En (nV)	Nominal Vcc (V)	Nominal Is (mA)	Vout Headroom (V)	Vcc Min (V)	Vcc Max (V)	1k MSRP Price	Description
Select	ISL28194	VFA	0.0035	0.0012	265	5	0.00033	0.009	1.8	5.5	$0.79	µPwr RailRail I/O
Select	ISL28195	VFA	0.01	0.0042	150	5	0.001	0.009	1.8	5.5	$0.73	µPwr RailRail I/O
Select	ISL28158	VFA	0.2	0.1	64	5	0.034	0.015	2.4	5.5	$0.89	µPwr RailRail I/O
Select	ISL28156	VFA	0.25	0.05	46	5	0.039	0.13	2.4	5.5	$1.00	µPwr RailRail I/O
Select	ISL28133	VFA	0.4	0.1	65	5	0.018	0.04	2	5.5	$0.90	Prec.Chopper
Select	EL8176	VFA	0.4	0.13	28	5	0.055	0.13	2.4	5.5	$0.76	µPwr RailRail I/O
Select	ISL28107	VFA	1	0.32	14	30	0.21	1.3	4.5	40	$0.89	Precision, LowNoise
Select	ISL28117	VFA	1.5	0.5	8	30	0.44	1.5	4.5	40	$0.83	Pec.WideVccRange
Select	ISL28113	VFA	2	1	22	5	0.09	0.01	1.8	5.5	$0.45	uPwr RR I/O
Select	ISL28136	VFA	5.1	1.9	15	5	0.9	0.07	2.4	5.5	$1.00	Prec.RailRail I/O
Select	ISL28114	VFA	7.7	2.8	11.8	5	0.4	0.05	1.8	5.5	$0.45	LowPwrRailRail I/O
Select	ISL28127	VFA	10	3.6	2.8	30	2.2	1.5	4.5	40	$1.05	Prec.WideVccRange
Select	ISL24021	VFA	15	18	12	10	2	0.025	4.5	19	$1.27	1A peak Io, RailRail I/O
Select	ISL28191	VFA	61	17	1.7	5	2.6	0.02	3	5.5	$1.32	Prec. Low Noise
Select	ISL55001	VFA	68	280	12	30	9	2.2	8	30	$2.11	Wide Supply Range
Select	EL5101	VFA	170	2200	10	10	2.5	1.6	5	12.6	$1.17	LowPwr High SR
Select	EL8102	VFA	198	600	12	5	5.6	0.3	4	5.5	$1.35	MedPwr HighSped
Select	ISL28190	VFA	83.3	50	1	5	8.5	0.02	3	5.5	$1.58	Prec. Low Noise
Select	EL8101	VFA	106	200	10	5	2	0.3	3	5.5	$1.09	LowPwr HighSpeed
Select	EL5103	VFA	165	2200	12	10	5	1.3	5	12.6	$1.18	MedPwr High SR
Select	EL5105	VFA	264	3000	10	10	5	1.3	5	12.6	$1.30	Highest Speed VFA
Select	EL5161	CFA	95	1500	4	10	0.75	1.6	5	12.6	$0.58	LowPwr HighSpeed
Select	EL5163	CFA	140	3000	3	10	1.5	1.6	5	12.6	$1.17	MedPwr HighSpeed
Select	EL8108	CFA	190	800	6	12	14.3	1	4.5	13	$1.88	Dual, High Output Current

FIGURE 54. ALTERNATE OP AMPS LIST IN THIS STAGE

Since only two parts are showing up as Recommended, the alternate list is showing everything else available in the tool at this time (March 2010). Selecting the EL5163 from this list will force the design to attempt to use this somewhat slower device. Doing that and going to the first stage shows the screen displayed in Figure 55.

Here, the tool is reporting that no parts satisfy the 2.96GHz speed requirement of this stage (at a gain of 5). There are actually two ways to proceed from this screen. Hitting the Continue button when no parts are available will simply list the top 10 devices in descending order of speed, while hitting the "Alternate Op Amps" + sign will list all op amps in the tool excluding none as there is nothing listed in the Recommended table at this point. Hitting the Continue button and picking the fastest part will display the screen shown in Figure 56.

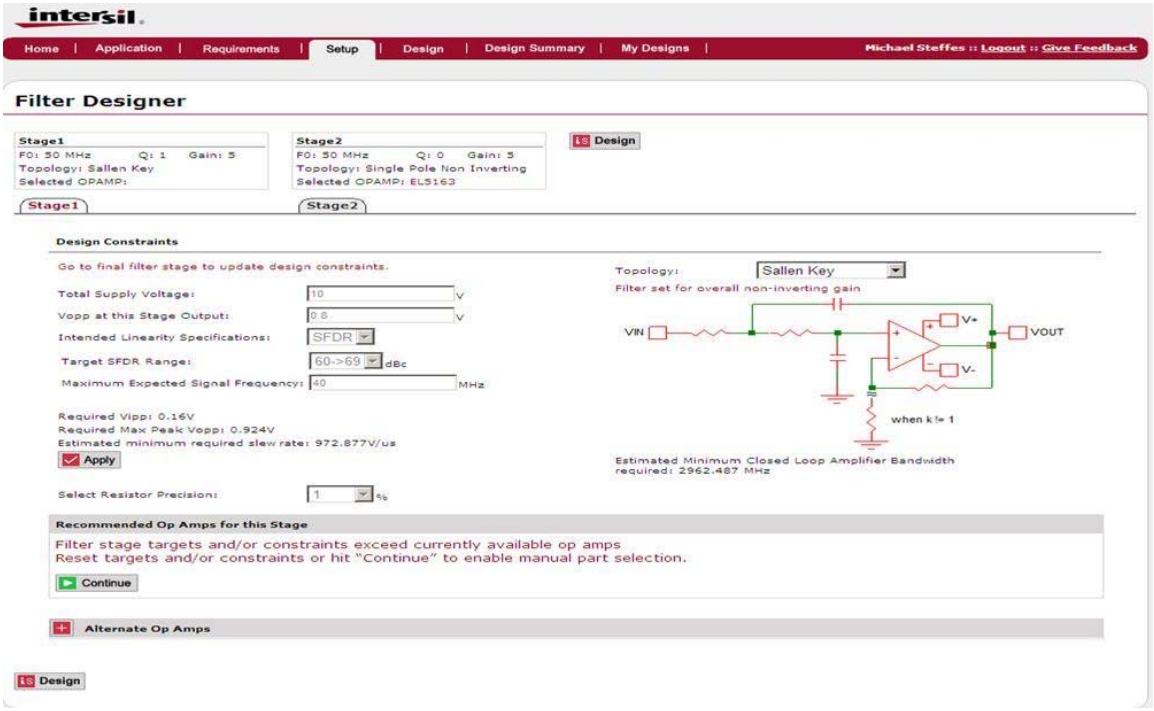


FIGURE 55. FIRST STAGE FOR 50MHz DESIGN

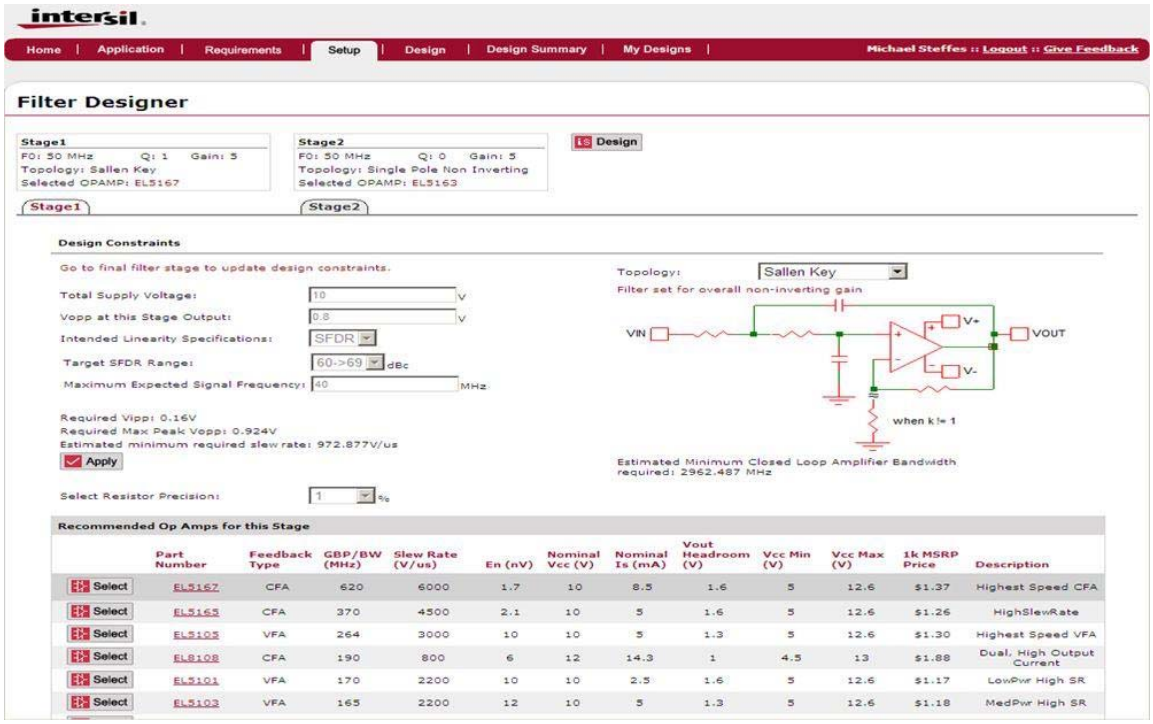


FIGURE 56. HITTING THE CONTINUE KEY TO JUST GET THE FASTEST PARTS

Now executing the design will do the best it can delivering the following simulation schematic shown in Figure 57.

Hitting the AC simulation key then expanding the Filter AC output plot into the WebScope waveform viewer and comparing the simulated magnitude response vs. the ideal response will display the screen shown in Figure 58.

The completed design gives a slightly more peaked response than an ideal 50Mhz 3rd order Butterworth response. This is coming from the Sallen-Key input stage where it is typically the case that inadequate speed in the amplifier stage will give an actual pole location that is slightly higher Q (more peaked) than expected.

There are numerous other ways to take advantage of the "Alternate Op Amps" feature but always remember there are usually good reasons that these parts do not appear on the "Recommended Op Amps" list.

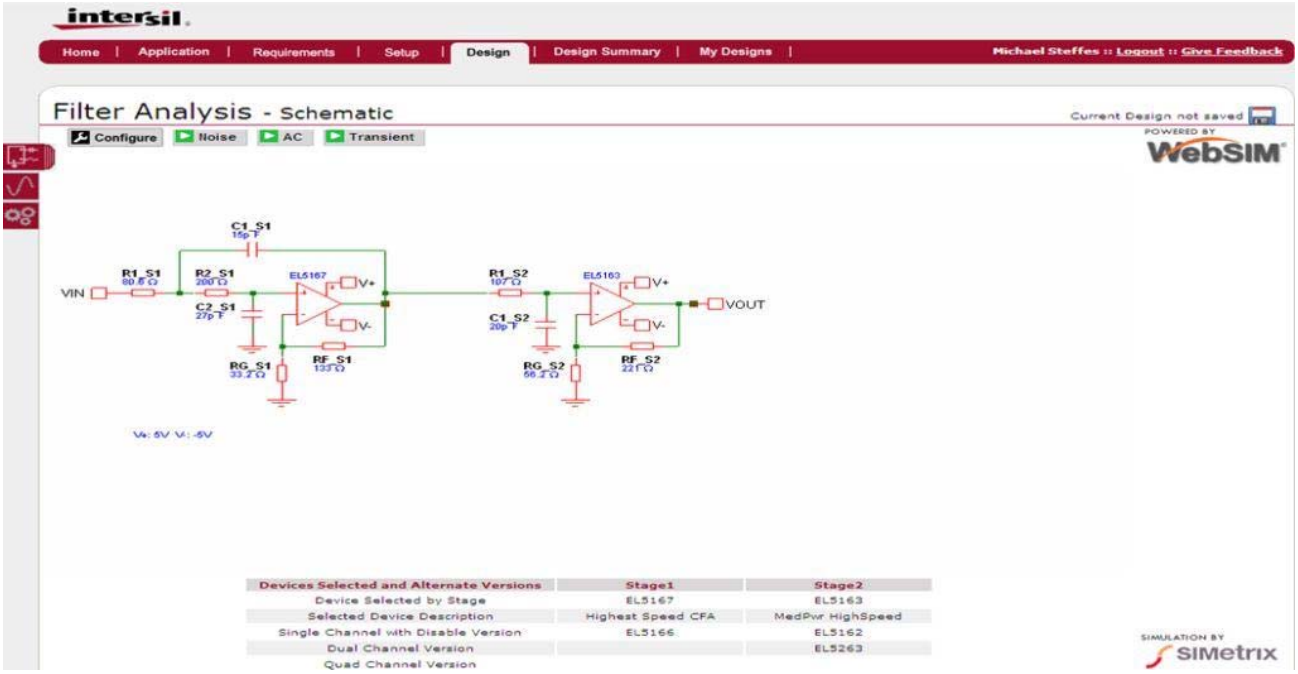


FIGURE 57. COMPLETED 50MHZ, 3RD ORDER BUTTERWORTH, GAIN OF 25V/V SCHEMATIC

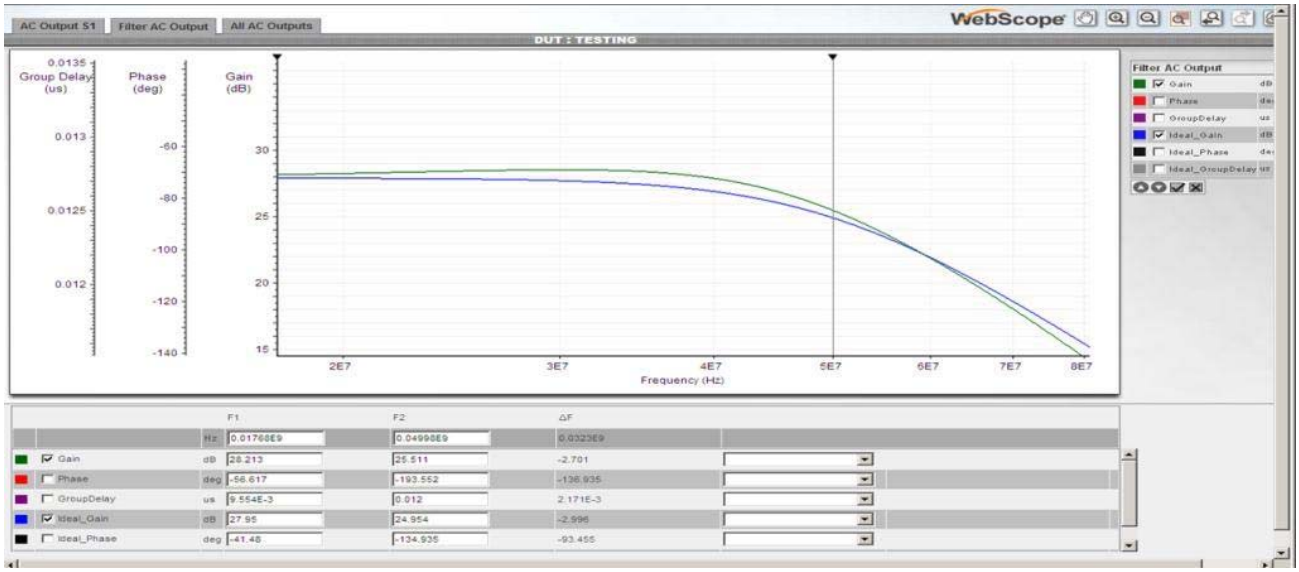


FIGURE 58. COMPARISON OF SIMULATED TO IDEAL GAIN RESPONSE