User's Manual

RX62T Motor Control Evaluation Kit

User Manual: Hardware

RX Family / RX600 Series / RX62T Group

Renesas Electronics
www.renesas.com

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the xxx/xx Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	RX62T Group Hardware Manual	R01UH0034EJ0100
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	Motor Control Evaluation Kit User's manual for Hardware	This User's manual
User's manual for Software	Description of CPU instruction set	xxx/xx Series User's manual for Software	R01USxxxxEJxxxx
Application Note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

Notation of Numbers and Symbols

Register Notation

List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Abbreviation	Full Form

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1. Overview

1.1. Purpose

This manual describes the technical details of the kit hardware. The Quick Start Guide provides details on the software installation and debugging environment.

1.2. Features

The RX62T Motor Control Kit is an evaluation tool for Renesas microcontrollers and incorporates the following features:

- Single board that consists of MCU and inverter stage
- Capability to drive two motors:
    - 24V up to 5A 3-phase Brushless DC motor with hall sensors, encoder and sensor-less with on-board hardware
    - Any 3-phase Brushless DC or AC Induction motor with user-supplied power stage
- Support for dual operation mode:
    - GUI mode : controlled by GUI from a personal computer through USB connection
    - Standalone mode: controlled by on-board potentiometer, pushbuttons and LCD
- Ease-of-use:
    - User code debugging
    - User interface such as: switches, potentiometer, LED, LCD
    - Sample application code
    - Sample peripheral initialization code
- Multiple sensor and sensor-less motor control algorithms
    - Three-shunt and single-shunt current measurement support
    - External amplifier and internal PGA support
- On-board USB isolator for E1 emulator

1.3. Applications

Home appliances, industrial automation, office equipment, audio equipment, consumer products etc.

1.4. Specifications

Tables 1.1 and 1.2 list the Specifications.

Table 1.1 Specifications (1)

Item	Function	Specification
CPU	Central processing unit	Rx600 CPU core • Number of fundamental instructions: 73 • Minimum instruction execution time: 10 ns (f(XIN) = 100 MHz, VCC = 2.7 V to 5.5 V) • Multiplier: 32 bits × 32 bits → 64 bits • Divider: 32 bits / 32 bits → 32 bits • Barrel shifter: 32 bits • Operating mode: Single-chip mode (address space: 4 Gbyte linear)
Memory	ROM, RAM, data flash	See Table 1.3 Products List.
Reset sources		• Hardware reset by RESET# • Power-on reset • Reset from two Watchdog timers • Software reset • Reset by voltage detection
Voltage detection	Voltage detection circuit	When voltage on detection When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Watchdog timer		• 8 bits x 1 channel • Select from among eight counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072) • Switchable between watchdog timer mode and interval timer mode
Independent Watchdog timer (IWDT)		• 14 bits x 1 channel • Counter-input clock: low-speed on-chip oscillator dedicated to IWDT
Clock	Clock generation circuits	• One circuit: Main clock oscillator • Internal oscillator: Low-speed on-chip oscillator dedicated to IWDT • Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency • Oscillation stoppage detection • Independent frequency-division and multiplication settings for the system clock (ICLK) and peripheral module clock (PCLK) • The CPU and system sections such as other bus masters, MTU3, and GPT run in synchronization with the system clock (ICLK): 8 to 100 MHz. • Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz
Power control		• Standard operating mode • Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode

Interrupts		• Peripheral function interrupts: 101 sources • External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) • Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt) • 16 levels specifiable for the order of priority
I/O ports	Programmable I/O ports	I/O port pins for devices in the 112-pin LQFP/100-pin LQFP/80-pin LQFP/64-pin LQFP • I/O: 61/55/44/37 • Input only: 21/21/13/9 • Open-drain outputs: 2/2/2/2 (I2C bus interface pins) • Large-current outputs: 12/12/6/6(0) (MTU3 and GPT pins) • The 5-V version of the 64-pin product does not have large-current outputs. • Reading out the states of pins is always possible.

Timer	Multi-function timer pulse unit 3 (MTU3)	• 16 bits x 8 channels • Up to 24 pulse inputs/outputs and three pulse inputs • Select from among six to eight counter-input clock signals for each channel (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • 24 output compare or input capture registers • Counter clearing (clearing can be synchronized with compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) input and output from all registers in synchronization with counter operation • Buffered operation • Cascade-connected operation • 38 kinds of interrupt source • Automatic transfer of register data • Pulse output modes • Toggled, PWM, complementary PWM, and reset synchronous PWM • Complementary PWM output mode • Outputs non-overlapping waveforms for controlling 3-phase inverters • Automatic specification of dead times • PWM duty cycle: Selectable as any value from 0% to 100% • Delay can be applied to requests for A/D conversion. • Non-generation of interrupt requests at peak or trough values of counters can be selected. • Double buffering • Reset-synchronous PWM mode • Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion

	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins • 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 • Initiation on detection of short-circuited outputs (detection of simultaneous switching of large-current pins to the active level) • Initiation by comparator-detection of analog level input to the 12-bit A/D converter • Initiation by oscillation-stoppage detection • Initiation by software • Selection of which output pins should be placed in the high-impedance state at the time of each POE input or comparator detection
Timer	General PWM timer (GPT)	• 16 bits x 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Operation of the several counters may be synchronized • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the low-speed on-chip oscillator clock signal dedicated to IWDT (to detect abnormal oscillation).
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)

Communications	Serial communications interface (SCIB)	• 3 channels Serial communications modes: • Asynchronous, clock synchronous, and smart-card interface • Multiprocessor communications • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer Noise cancellation (only available in asynchronous mode)
	I2C bus interface (RIIC)	• 1 channel Communications formats: • I2C bus format/SMBus format • Master/slave selectable
	CAN module (CAN) (as an optional function)	• 1 channel • 32 mailboxes
Communications	Serial peripheral interface (RSPI)	• 1 unit RSPI transfer facility • Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave Data formats • Switching between MSB first and LSB first • The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. • 128-bit buffers for transmission and reception • Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Buffered structure • Double buffers for both transmission and reception
	LIN module (LIN)	• 1 channel (LIN master) • Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol

2. Power Supply

2.1. Requirements

The main power source for the kit is a 24V DC external power supply that can be connected to J3 2.5 mm barrel type connector. An additional power connector J4 is provided for use with a bench type power supply. From this main power source multiple voltages are derived and are shown in Table 1 below. When the board is connected to a personal computer, a secondary isolated 3.3VDC is derived from the USB bus voltage.

Supply Voltages	Purpose	Schematic Symbol	Circuit	Source
24V DC	DC Bus	VBUS	external power supply	J3 or J4
12V DC	MOSFET driver	VDRV-12V	U9 12V DC regulator	24V DC bus
5V DC	Logic	VCC-5V	U8 5V DC regulator	24V DC bus
5V DC	Analog	ANVCC-5V	L5,C48	VCC-5V
4.25V DC	Analog reference	REF 4.25V	U11 shunt regulator	ANVCC-5V
3.3V DC	LCD	3V3_LCD	U23 DC regulator	VCC-5V
3.3V DC	H8S USB Isolator	VCC3V3-M1	U2 DC regulator	VUSB5V

Table 1 Power supplies

2.2. Protection

2.2.1. Short Circuit

Short circuit protection for the main 24V DC power source is provided by a fast acting 5A fuse FU1. In addition both the 12V DC and 5V DC regulators have built in short circuit protection. The USB power source is protected by a resettable fuse F1 as well as by 3.3V regulator internal short circuit protection.

2.2.2. Reverse Polarity

Protection against accidental polarity reversal at the main 24V DC connector terminals is provided by the circuit shown in Figure 1 below. When the right polarity is applied, Q1 is turned on by the positive voltage provided at the gate by R35 and the negative terminal –VBUS is connected to VBUS ground reference. When the reverse polarity is applied, Q1 is off and –VBUS is not connected.

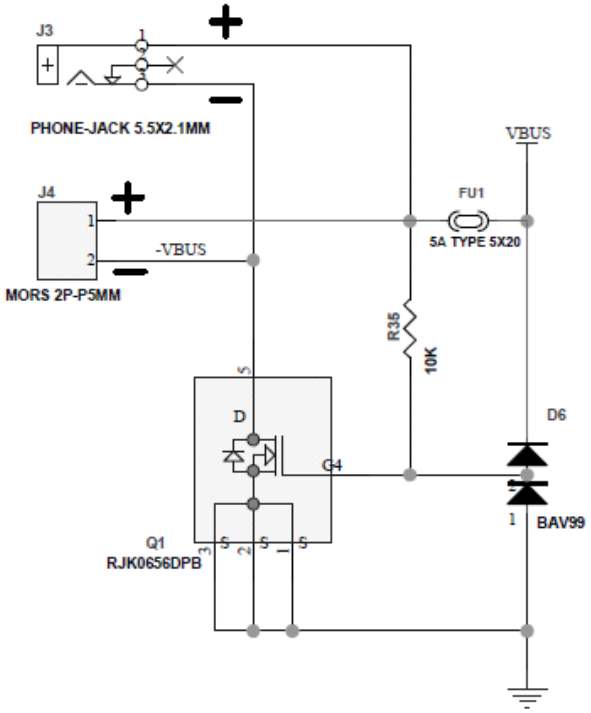

Figure 1 Reverse polarity protection

3. Board Layout

3.1. Functional Description

The board layout with the main functional features is shown in Figure 2. Several connectors are provided for the power supply, motor, sensors, external power module, debugging tools, personal computer GUI and user SPI port. Push buttons and potentiometer are provided for standalone operation control. A 96x64 dot graphic LCD is used to display motor parameter data such as RPM, Current, Voltage, etc.

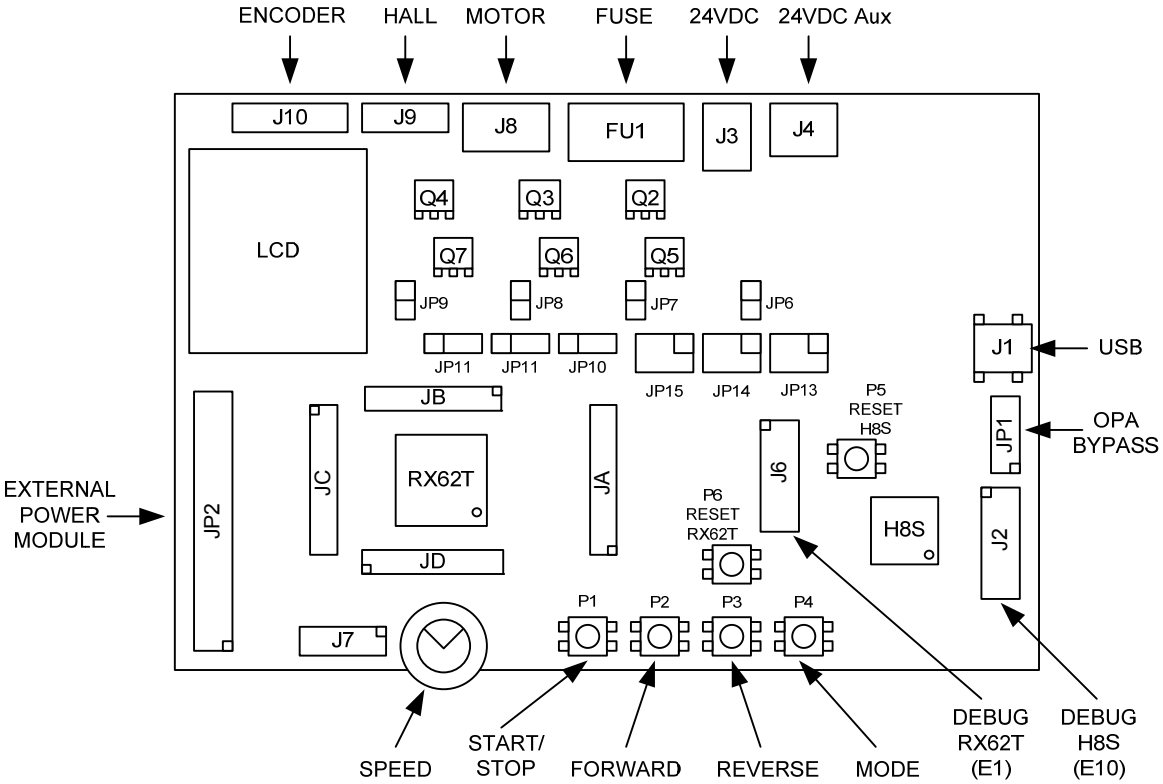

Figure 2 Board functional layout

The kit uses the Renesas Rx62T as the main microcontroller to control up to two 3-phase motors. A second Renesas H8S microcontroller is used to provide UART to USB translation for the GUI as well as galvanic isolation from the high-voltage motor drives. The isolated power supply for the H8S is derived from the USB bus voltage.

3.2. Board Configuration

The Rx62T has special peripherals built in to support various motor control algorithms and the evaluation board hardware has to be reconfigured to match the algorithm present in the flash memory. The board hardware supports both 180˚ sinusoidal and 120˚ trapezoidal drive topologies in sensor-less and sensor modes. However the sample software provided with the kit supports only 180˚sinusoidal drive method in sensor-less mode by 3-shunt or single shunt current measurement and sensor mode by encoder feedback. The encoder based algorithm is used for position control. The Rx62T has the resources and capability to support two 3-phase motor drives simultaneously. The board has all the necessary hardware including the power stage for one 24V BLDC motor and has a connector to interface with an external power module to drive the second motor. The sample software provided with the kit supports only the onboard power stage to drive one motor.

3.2.1. 180˚ Sinusoidal Drive Support

The sample software package provided with the kit is comprised of five distinct codes samples to support FPU based control algorithms. For each algorithm the hardware must be reconfigured by jumper settings shown in Table 2. The sample code algorithms are divided in two major groups based on the current measurement method as 3-shunt and 1-shunt.

- 3-Shunt FPU based Vector Control
    - 1) - Sensor-less with External Op. Amp. (Default)
    - 2) - Sensor-less Internal PGA and comparators
    - 3) - Encoder based speed and position control
- 1-Shunt FPU based sensor-less Vector Control
    - 4) - Sensor-less with External Op. Amp.
    - 5) - Sensor-less Internal PGA and comparators

The jumper setting for various sensor-less algorithms are shown in Table 2 below:

Operation		JP6	JP7	JP8	JP9	JP10	JP11	JP12	JP13	JP14	JP15
External OPA	3 - Shunt	1 - 2	–	–	1 - 2	1 - 2	1 - 2	1 - 2	1 - 2	1 - 2	1 - 2
	1 - Shunt	–	1 - 2	1 - 2	–						
Internal PGA	3 - Shunt	1 - 2	–	–	1 - 2	2 - 3	2 - 3	2 - 3	3 - 4	3 - 4	3 - 4
	1 - Shunt	–	1 - 2	1 - 2	–						

Table 2 Configuration jumper setting

The only sensor based algorithm supported by the sample software package is the encoder based position control. The hardware configuration for encoder operation is the same as for the 3-Shunt with external OPA. The position control provides precise rotation angle movement configurable by the user from the control GUI.

3.2.2. 120˚ Trapezoidal Drive Support

The hardware supports both sensor and sensor-less 120˚ trapezoidal mode operation, but there is no sample code supplied with the kit. However the motor included in the kit is fitted with Hall sensors and connector J9 is provided for interfacing.

For sensor-less trapezoidal control the hardware supports BEMF detection by ADC and internal comparators. The jumper configurations are shown in Table 3.

Operation		JP6	JP7	JP8	JP9	JP10	JP11	JP12	JP13	JP14	JP15
BEMF Detection	ADC	–	1 - 2	1 - 2	–	1 – 2	1 – 2	1 – 2	5 - 6	5 - 6	5 - 6
	Internal Comparator	–	1 - 2	1 - 2	–						

Table 3 Jumper configuration for BEMF detection

4. RX62T Peripheral Resources

4.1. Resources for Motor 1 Support

4.1.1. Motor 1

The on-board hardware is capable of driving a BLDC motor with a 24VDC and up to 5A external power supply. The Rx62T timers used are MTU3_6 and MTU3_7. The motor supplied with the kit is an Anaheim Automation , 3-Phase BLDC motor, PN# BLY171D-24V-4000-1000SI-05 or equivalent equipped with hall sensors and a 1000 line per revolution quadratic encoder with index. Figure 3 shows the BLY171D-24V-4000-1000SI-05.

Figure 3 BLDC motor BLY171D-24V-4000-1000SI-05

The RX62T peripheral resources used to drive Motor 1 are shown in Table 4

Control Function		Rx62T Peripherals		I/O Function	Pin#
Motor 1	PWM UH1	MTU3	MTU3_6 MTU3_7	MTIOC6B	45
	PWM VH1			MTIOC7A	46
	PWM WH1			MTIOC7B	47
	PWM UL1			MTIOC6D	48
	PWM VL1			MTIOC7C	49
	PWM WL1			MTIOC7D	50
	HALL1 A		MTU3_0	MTIOC0A	32
	HALL1 B			MTIOC0B	33
	HALL1 C			MTIOC0C	34
	ENCODER1 A		MTU3_1	MTCLKA	67
	ENCODER1 B			MTCLKB	68

	ENCODER1 Z	ICU		IRQ0-B	1
	VB1	S12ADA	S12ADA0	AN003	88
	IU1			AN002	89
	IV1			AN001	90
	IW1			AN000	91
	VREF 4.25V	ADA	Ch-0	AN0	77
	Speed Pot		Ch-1	AN1	76
	IV1		Ch-3	AN3	74
	OUT U,V,W common		Ch-4	AN4	70
	P1 (START / STOP)	IO		P53	80
	P4 (FORWARD)			P52	81
	P3 (REVERSE)			P51	82
	P2 (MODE)			P50	83
	POE4# (Over-current)			POE#4	43
	DL1 (LED)			P30	58
	DL2 (LED)			P31	59
	DL3 (LED)			P32	61
	DL4 (LED)			P33	63
	LCD - /RS			PE3	9
	LCD-/RESET			PA0	41
	LCD - SDA	RSPI	Ch-B	MOSI-B	35
	LCD - SCKL			RSPCK-B	37

Table 4 Motor 1 resources

4.1.2. H-Bridge Drive

To drive Motor 1, timer channels MTU3-6 and MTU3-7 are used to produce three sets of complementary PWM outputs with dead-time: PWM_UH1/PWM_UL1, PWM_UV1/PWM_VL1, PWM_WU1/PWM_WL1. These signals drive the six MOSFET H-bridge shown in Figure 4.

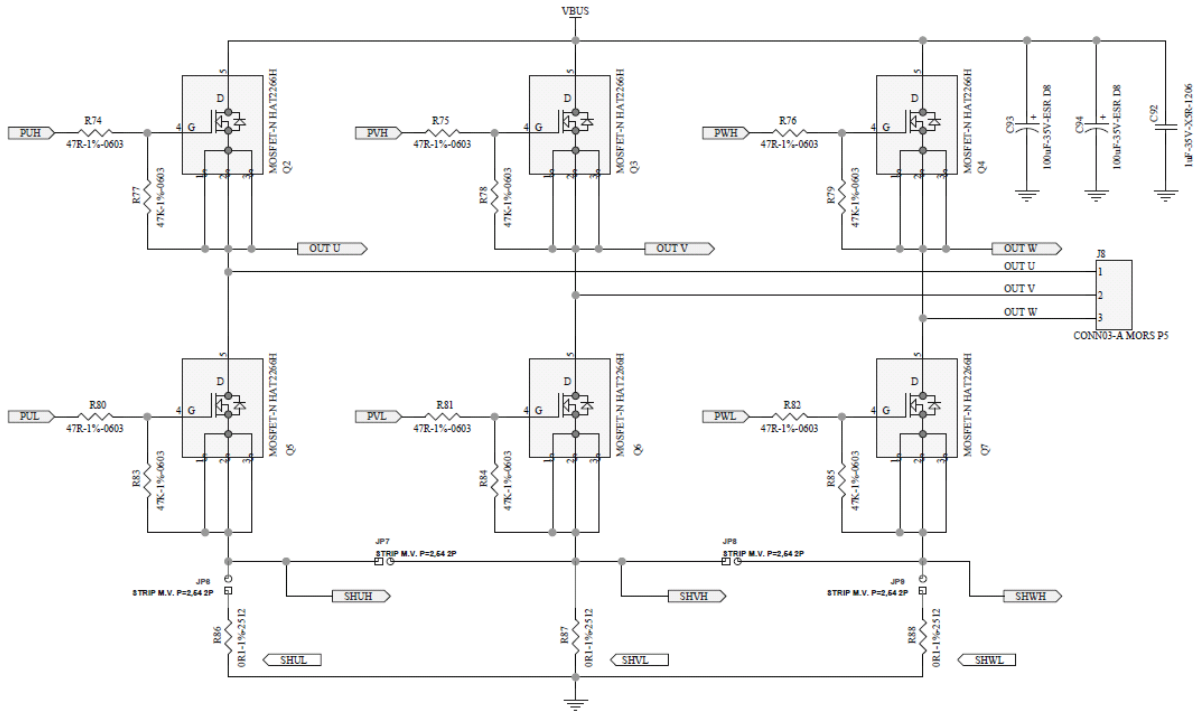

Figure 4 H-Bridge

4.1.3. Current and Voltage Sensing

For sensor-less control, the motor phase currents IU1, IV1, IW1 and DC bus voltage VB1 are sampled and measured simultaneously by the 4 inputs of the 12-Bit analog to digital converter unit S12ADA.

4.1.4. Hall Sensor Interfacing

For hall sensor support three input capture pins MTIOC0A, MTIOC0B and MTOIC0C of timer channel MTU3-0 are used and the interface connector J9 shown in Figure 5 below.

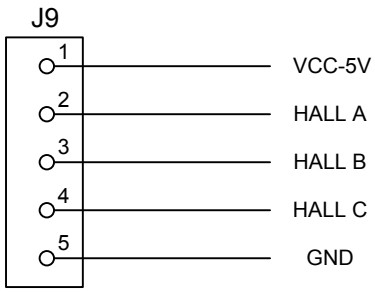

Figure 5 Hall sensor connector

4.1.5. Encoder Interfacing

To interface the three wire encoder of Motor 1, signals A and B are connected to the external clock inputs MTCLKA and MTCLKB of timer channel MTU3-1are used. Signal Z is connected to external interrupt pin IRQ0-B. Connector J10 shown in Figure 6 below is provided for the encoder interfacing.

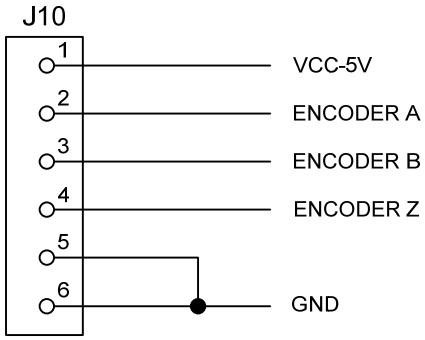

Figure 6 Encoder connector

4.1.6. Standalone Operation Support

For standalone operation manual control functions START/STOP, FORWAED, REVERSE, MODE and motor SPEED are provided by pushbuttons P1, P2, P3, P4 connecter to port P50, P51, P52, P53 and a potentiometer connected to the channel 1 of the 10-bit analog to digital converter ADA. Figure 7 shows these controls.

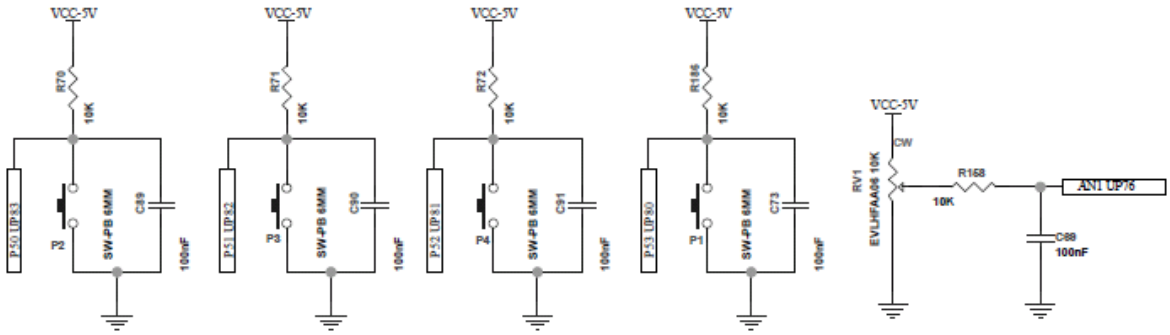

Figure 7 Standalone controls

4.1.7. Over-current Detection

Protection against an over-current and undercurrent situations of Motor 1 is implemented by summing all phase currents and comparing it with two thresholds of a window comparator as shown in Figure 8.

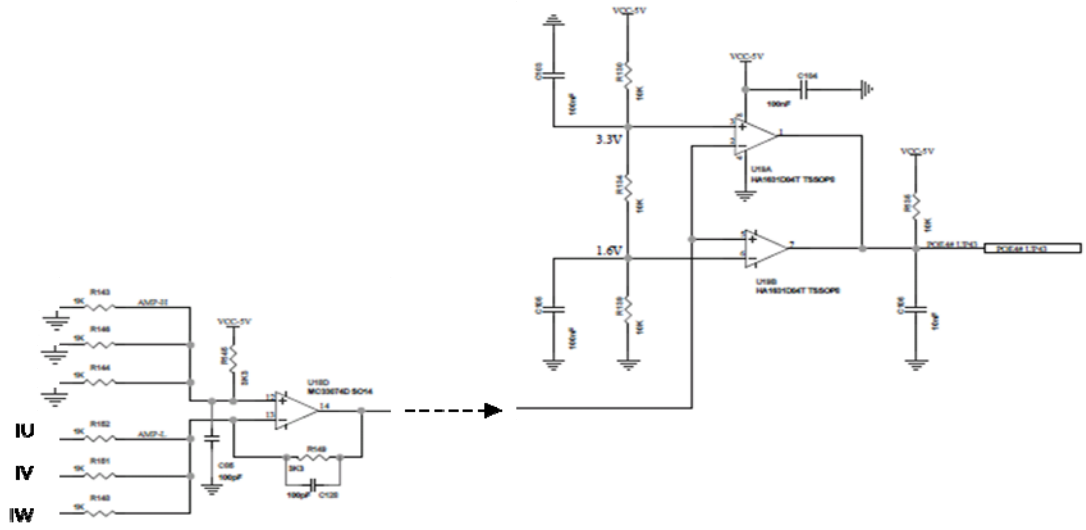

Figure 8 Over-current, under-current protection

The comparator output signal is connected to POE4# pin of the RX62T. When this pin is triggered, the PWM outputs to the motor drive will be placed in high-impedance mode.

4.2. Resources for Motor 2 Support

The RX62T peripheral resources to support Motor 2 are listed in Table 5

Control Function		Rx62T Peripherals		I/O Function	Pin#
Motor 2	PWM UH2	MTU3	MTU3_3 MTU3_4	MTIOC3B	56
	PWM VH2			MTIOC4A	55
	PWM WH2			MTIOC4B	54
	PWM UL2			MTIOC3D	53
	PWM VL2			MTIOC4C	52
	PWM WL2			MTIOC4D	51
	HALL2 A		MTU3_5	MTIC5U	96
	HALL2 B			MTIC5V	97
	HALL2 C			MTIC5W	98
	ENCODER2 A		MTU3_2	MTCLKC	99
	ENCODER2 B			MTCLKD	100
	ENCODER2 Z	ICU		IRQ1-B	8
	VB2	S12ADA	S12ADA1	AN103	84
	IU2			AN102	85
	IV2			AN101	86
	IW2			AN100	87
	TEMP2	ADA	Ch-2	AN2	75
	FAULT2	IO		POE0#	57

Table 5 Motor 2 resources

Figure 9 shows the external power stage connector JP2.

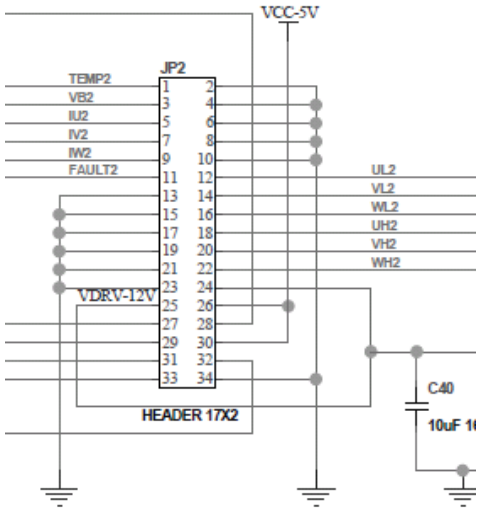

Figure 9 External power stage connector

This connector provides an interface to an external power module to drive a second 3-phase motor.

4.3. Miscellanies functions

4.3.1. Communication

The Rx62 resources to support various communication needs are shown in Table 6.

	Peripheral Function		I/O Function	Rx62T Pin#
Communication	H8S/2212 Communication	SCI	TXD2	28
			RXD2	27
	EEPROM	RIIC	EEPSCL	16
			EEPSDA	17
	TDO	RSPI	RSPCK-A	64
	MDI		MOSI-A	65
	TMS		MISO-A	66

Table 6 Communication support

TXD2/RXD2 pins are used for UART communication with the motor control GUI through USB bridge implemented with H8S/2212 microcontroller. The RSPI port is a spare communication port and can be accessed on connector J7.

4.3.2. E1 Debugger

Table 7 shows the Rx62T pins reserved for the E1 debugger and the corresponding J5 connector pins.

	I/O Function	J5	Rx62T Pin#
E1 Debugger	MDE	4	2
	EMLE	6	4
	TCK	1	21
	TRST	3	18
	TDO	5	22
	MDI	7	6
	TMS	9	19
	TDI	11	20
	RESET	13	10
	MDO	10	7

Table 7 E1 Debugger interface

4.3.3. Debug Support

The board has various built in functionality to support firmware debugging.

4.3.3.1. Timer PWM outputs

To support debugging and troubleshooting of various motor control variables, six timer outputs are available for PWM duty cycle monitoring. The variables can be translated into PWM duty cycles and monitored on the low-pass filters terminated outputs of timers: GPT2, GPT3, MTU3-1 and MTU3-2. The circuits and the pins are shown in Figure 10 and Table 8.

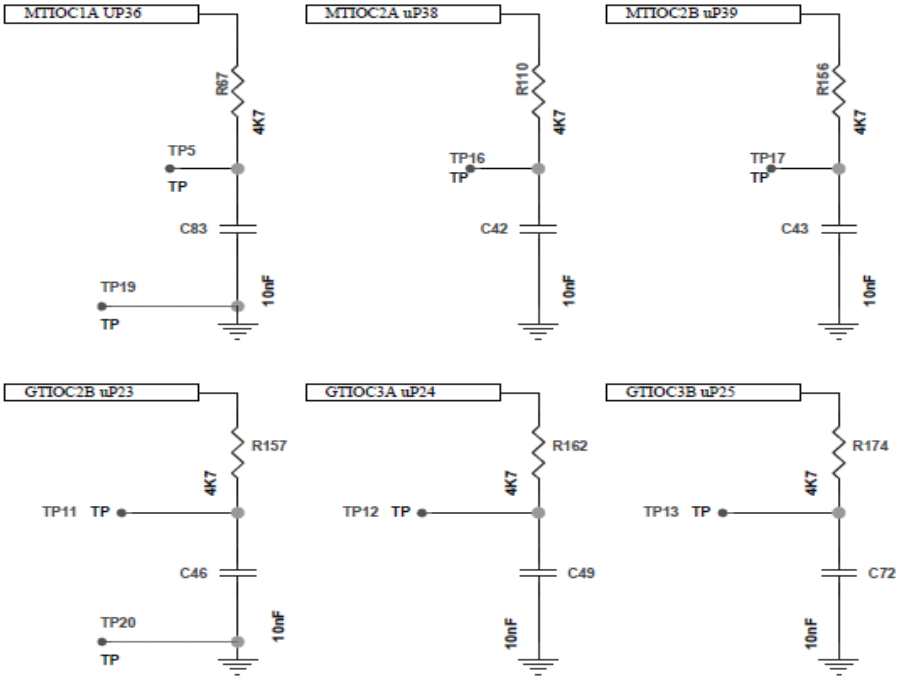

Figure 10 Debug PWM outputs

	Peripheral Function	I/O Function	Rx62T Pin#
Debug PWM Outputs	GPT2, GPT3	GTIOC2B	23
		GTIOC3A	24
		GTIOC3B	25
	MTU3-1, MTU3-2	MTIOC1A	36
		MTIOC2A	38
		MTIOC2B	39

Table 8 Debug PWM output support

4.3.3.2. Unused Pins

Table 9 shows all the unused pins of the Rx62T MCU. These pins can be configured by the user for their various I/O peripheral needs.

	I/O Function	Rx62T Pin#
Spare Pins	PB7/SCK2-A/TRDATA1	26
	PB4/GTERG/IRQ3/POE8#	30
	P65/AN4	69
	P55/AN11	78
	P54/AN10	79

Table 9 Unused Pins

4.3.4. Rx62T Pin Probing Connectors

To allow easy access to the Rx62T pins, probing connectors JA, JB, JC, JD are provided as shown in Figure 11. Note that the connectors are not mounted.

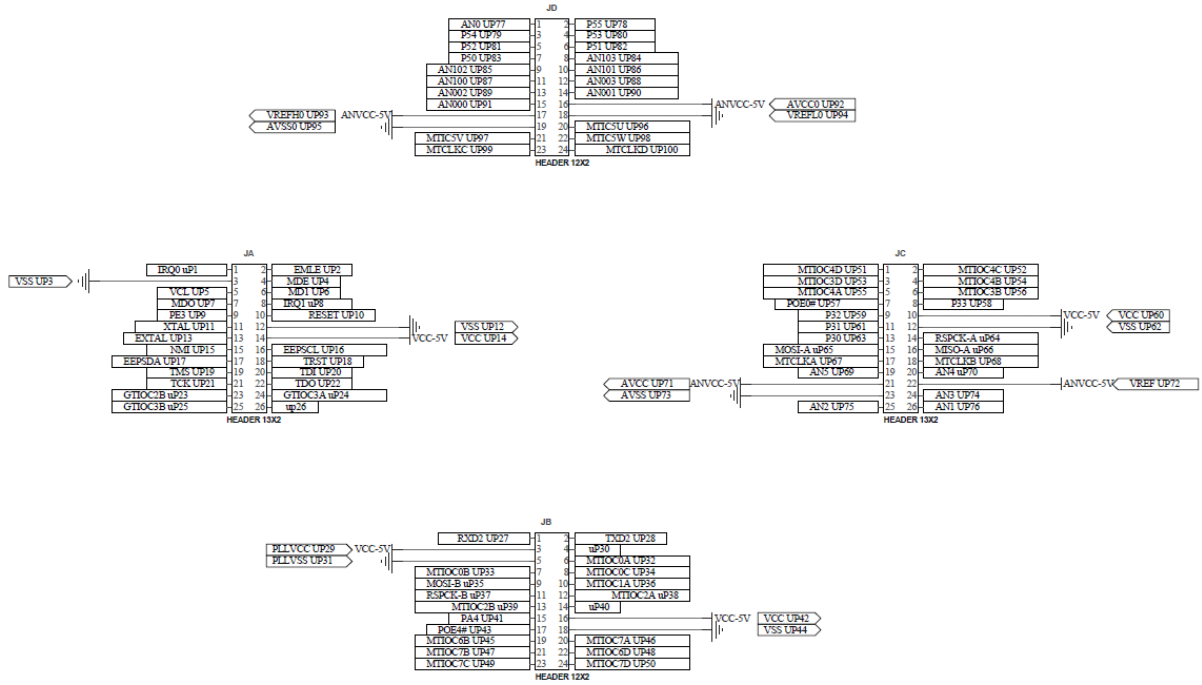

Figure 11 Rx62T pin probing connectors

5. PC GUI Support

To support the GUI operation an H8S/2212 Renesas microcontroller is used. The communication with the PC is through the USB interface with the Rx62T UART and a galvanic isolator is provided as shown in Figure 12. The isolation IC is a barrier between the high voltages present on the motor power stages and the PC.

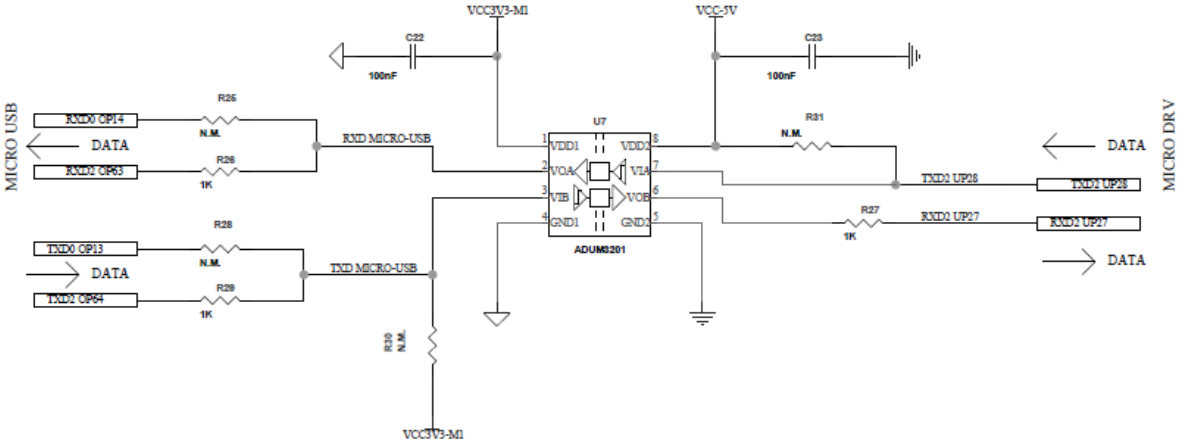

Figure 12 Galvanic Isolation Barrier

6. Further Reading

To further explore the features and capabilities of this kit please consult the following documents, they are located on the CD and can be reached using the Manual navigator (or Explore the CD):

Rx62T Motor Kit Quick Start Guide – Document: D011033_11_V0100

Three Shunt Sensor-less Vector Control of PMSM Motors – Document: R01AN0903EU

Single Shunt Sensor-less Vector Control of PMSM Motors – Document: R01AN0901EU

Three Shunt Sensor-less Vector Control of PMSM Motor with Internal Programmable Gain Amplifier (PGA) – Document: R01AN0902EU

Single Shunt Sensor-less Vector Control of PMSM Motor with Internal Programmable Gain Amplifier (PGA) – Document: R01AN0900EU

Position Control of PMSM Motors with Encoder – Document: R01AN0899EU

Plus:

RX62T Group User's Manual: Hardware – Document: R01UH0034EJ

RX Compiler Package User’s Manual – Document: R20UT0570EJ

High-performance Embedded Workshop IDE user’s Manual – Document: R20UT0372EJ

RX62T Group datasheet – Document: R01DS0096EJ

RJK0656DPB Silicon N Channel Power MOS FET Datasheet – Document: REJ03G1882

YMCRPRX62T_Schematic.pdf – Board Schematic for YMCRPRX62T

Motor_BLY171D-24V-4000-05.pdf – Motor specifications