Introduction

Power supply sequencing is a method of staging two or more power supply output voltages. Sequencing makes the timing between power supplies turning on and off very deterministic. This document describes the application of the ZL2005 in an Autonomous Sequencing application.

Autonomous Sequencing technology is a feature of the ZL2005 where the relationship between each output is configured by pin-strap settings. An Autonomous Sequencing group is defined as a set of ZL2005 devices that are configured to sequence relative to each other without the intervention of a host controller. A common two wire bus provides the means for all devices to communicate their requirement to turn on or turn off relative to each other within the group. This type of sequencing that includes inter-device communication allows for a very robust, easy to implement and intelligent sequencing method.

Each ZL2005 device is pin-strap configured for its own output voltage, softstart ramp, power-up delay, clock configuration, and bus address. A device's group position is determined by the pin-strap setting of its address. The first ZL2005 device in an Autonomous Sequencing group is defined by being set to the lowest address within the group and the setting of the CFG pin. The last ZL2005 device in an Autonomous Sequencing group is defined by the highest consecutive address within the group and the setting of the CFG pin. All of the ZL2005 ENABLE pins are connected together and driven by a single logic source. The first device initiates the power up of the sequencing group following assertion of ENABLE. The last device initiates the power down of the sequencing group following de-assertion of ENABLE. In the event of a fault within the group, shut down will be communicated within the group and an immediate power down of all devices within the group will begin. Each sequencing communication in the group is the result of an event within the group. The ability to communicate faults within the group is termed "fault spreading."

Autonomous Sequencing Example

This section describes an example of Autonomous Sequencing technology using two ZL2005 devices mounted on two ZL2005EV1 evaluation boards. The sequencing scenario will include a 3.3V rail and a 1.5V rail that are configured to sequence in a preset manner.

A ZL2005 device that is used for Autonomous Sequencing capabilities is expected to be pin-strap configured from the factory default state with no parameters stored in either USER_STORE or DEFAULT_STORE. Stored configurations should be erased from all devices. A new ZL2005EV1 EVB will have a configuration stored in the DEFAULT_STORE. To erase all stored configurations perform the following steps:
1. Invoke the ZL2005 Evaluation Software
2. Select the "PMBus: Advanced" page.
3. Click "RESTORE_FACTORY"
4. Click "STORE_DEFAULT_ALL"
5. Click "OK"
6. Click "STORE_USER_ALL"
7. Click "OK".

Then select the address for the next board (0x21) and repeat the configuration erase for that board's device. This procedure will erase all stored configurations and place each device in the factory default state.

The configuration pin (CFG) is used to set the relative position of a ZL2005 device within an Autonomous Sequencing group. A resistor from ground applied to this pin sets the device to be either first, in the middle or last in the group. The lowest addressed device in the group must be set as the first device of the group. The consecutively addressed devices must be set as middle devices. The highest consecutively addressed device must be set as the last device.

The ZL2005 address pins set the absolute position of the device within an Autonomous Sequencing group. The addresses must be set in conjunction with the CFG pin setting and must be set in a consecutive order. The ZL2005 pin-strap addressing is settable from address 0x20 to 0x27 with combinations of high, open and low on pins SA1 and SA0. Refer to the data sheet for the address settings. Other address ranges can be selected through resistor settings on the SA1 and SA0 pins, but the addresses must be limited to groups of eight such as 0x40 through 0x 47, or 0x58 through 0x5F, or 0x60 through 0x67, for example.

Table 1. ZL2005 Device Settings

Pin	Device on EVB #1	Device on EVB #2
SA1, SA0	low, low (address x20)	low, open (address x21)
V1, V0	high, low (2.5V)	open, low (1.2V)
SYNC	open (auto detect)	open (auto detect)
CFG	low (SYNC pin is input)	low (SYNC pin is input)
DLY1, DLY0	open, open (10 ms delay)	open, open (10 ms delay)
SS1, SS0	open, high (20 ms ramp time & PG delay)	open, open (10 ms ramp time & PG delay)
ILIM1, ILIM0	open, high (70 mV/2.7 mΩ = 25.9A)	open, high (70 mV/2.7 mΩ = 25.9A)
FC1, FC0	open, high (stable for power train)	open, high (stable for power train)
UVLO	open (4.5V min)	open (4.5V min)

ZL2005 Device Settings

Table 1 describes the pin-strap values applied to each ZL2005EV1 to prepare the device on each EVB for autonomous sequencing activities.

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ZL2005EV1 EVB Connections

1. Connect the evaluation boards together using J13 of board #1 (address x20) and J12 of board #2 (address x21). The inter-device bus, ENABLE and SYNC pins are connected together via these connectors.
2. Place the ENABLE jumper to the "MSTR EN" position on both boards.
3. Set the ENABLE switch of board #2 to the middle position (MONITOR).
4. Connect USB cable from PC to USB jack[1]
5. Connect RTN of EVB#1 to RTN of EVB#2.
6. Connect VIN of EVB#1 to VIN of EVB#2.
7. Connect the power source GND to RTN and V+ to VIN.
8. Turn the input power supply on.
9. Enable outputs by the ENABLE switch on board #1

NOTE 1: These EVBs are configured to work in a group mode with inter-device communication. The USB from a PC must be connected to the USB jack in order to power the onboard microcontrollers. If the onboard microcontrollers are not powered they apply an improper load to the inter-device bus which disables the communication between ZL2005s.
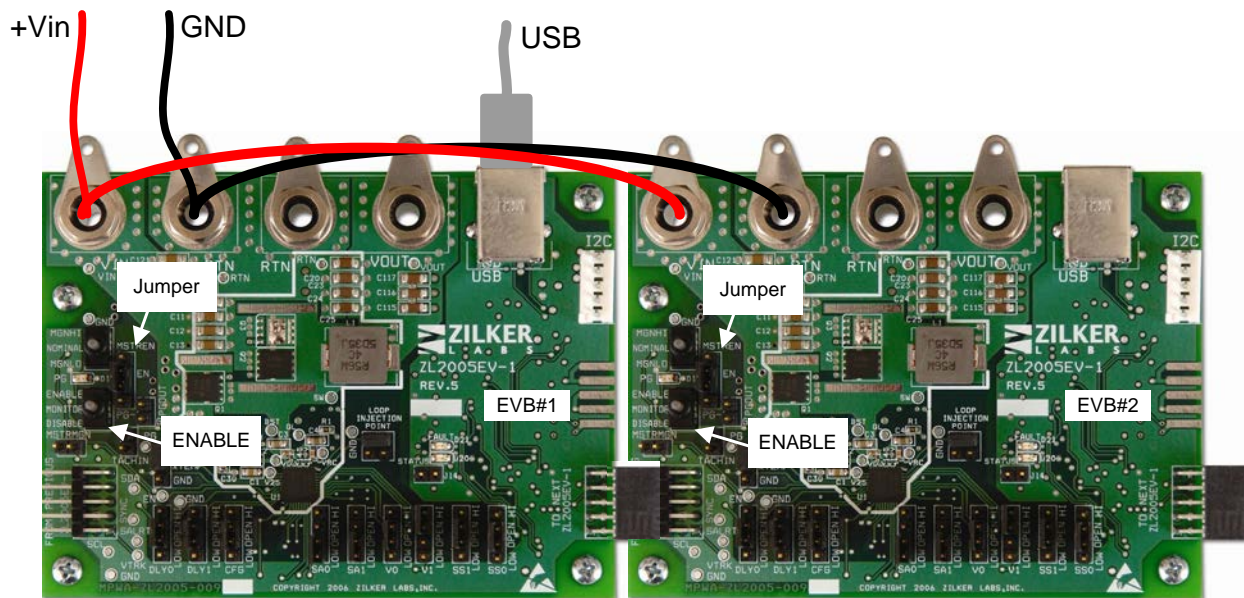
Figure 1. EVB Connections for Autonomous Sequencing

Autonomous Sequencing Example: Enable Sequence
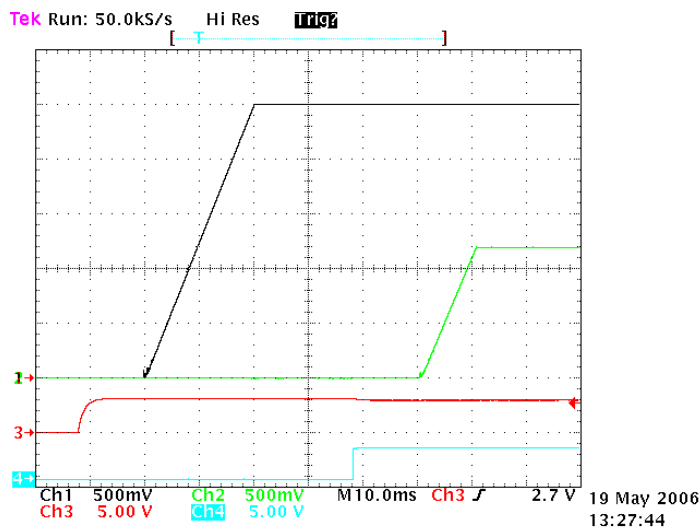
Figure 2. Enable Sequence

Channel 1 = VOUT1, board #1
Channel 2 = VOUT2, board #2
Channel 3 = ENABLE
Channel 4 = Power Good, board #1

In Figure 2, the scope is set to trigger on the ENABLE event. The ENABLE signal is the first to go high. The next signal to change is the turn-on ramp of VOUT1 since it has been configured to be the first device in the group. It occurs 10 ms after ENABLE (DLY1:DLY0 set to 10 ms). The time of the VOUT1 ramp is 20 ms (SS1:SS0 set to 20ms). Power Good 1 then goes high 20 ms after VOUT1 is above power good threshold (power good delay = softstart = 20 ms). At the time of Power Good 1 going high, device #1 communicates over the inter-device bus that the next device in the group can begin its enable procedure (not shown). The delay for VOUT2 to begin its turn on is set to 10ms. The ramp time for VOUT2 is 10 ms (SS1:SS0 set to 10 ms).

Autonomous Sequencing Example: Disable Sequence
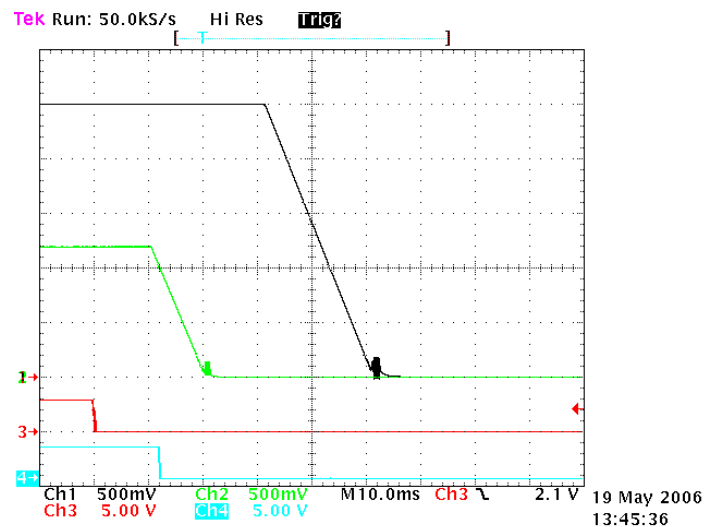
Figure 3. Disable Sequence

Channel 1 = VOUT1, board #1
Channel 2 = VOUT2, board #2
Channel 3 = ENABLE
Channel 4 = Power Good, board #2

In Figure 3, the scope is set to trigger on the ENABLE event. The ENABLE signal is the first to go low. The next signal to change is the VOUT2 turn off ramp since it has been configured to be the last device in the group. It occurs 10 ms after ENABLE going low (DLY1:DLY0 set to 10 ms). The time of the VOUT2 ramp is 10 ms (SS1:SS0 set to 10ms). The next signal to change is the Power Good 2 which goes low after VOUT2 drops below the power good threshold. At the time VOUT2 ramps to zero volts, device #2 communicates over the inter-device bus that the next device in the group can begin its disable procedure (not shown). The delay for VOUT1 to begin its turn off is set to 10 ms. The ramp time for VOUT1 is 20 ms (SS1:SS0 to 20 ms).

References

[1] *ZL2005 Data Sheet*, Zilker Labs, Inc., 2006.

[2] AN2013 – *ZL2005 and PMBus™*, Zilker Labs, Inc., 2006.

Revision History

Date	Rev. #	
July 10, 2006	1.0	Initial Release
October 3, 2006	2.2	Updated EVB picture on Page 3
May 4, 2009	AN2022.0	Assigned file number AN2022 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read "Intersil and it's subsidiaries including Zilker Labs, Inc." No changes to app note content.

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